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EDN

Shielding

Use NAPLPS to ease graphics transmission

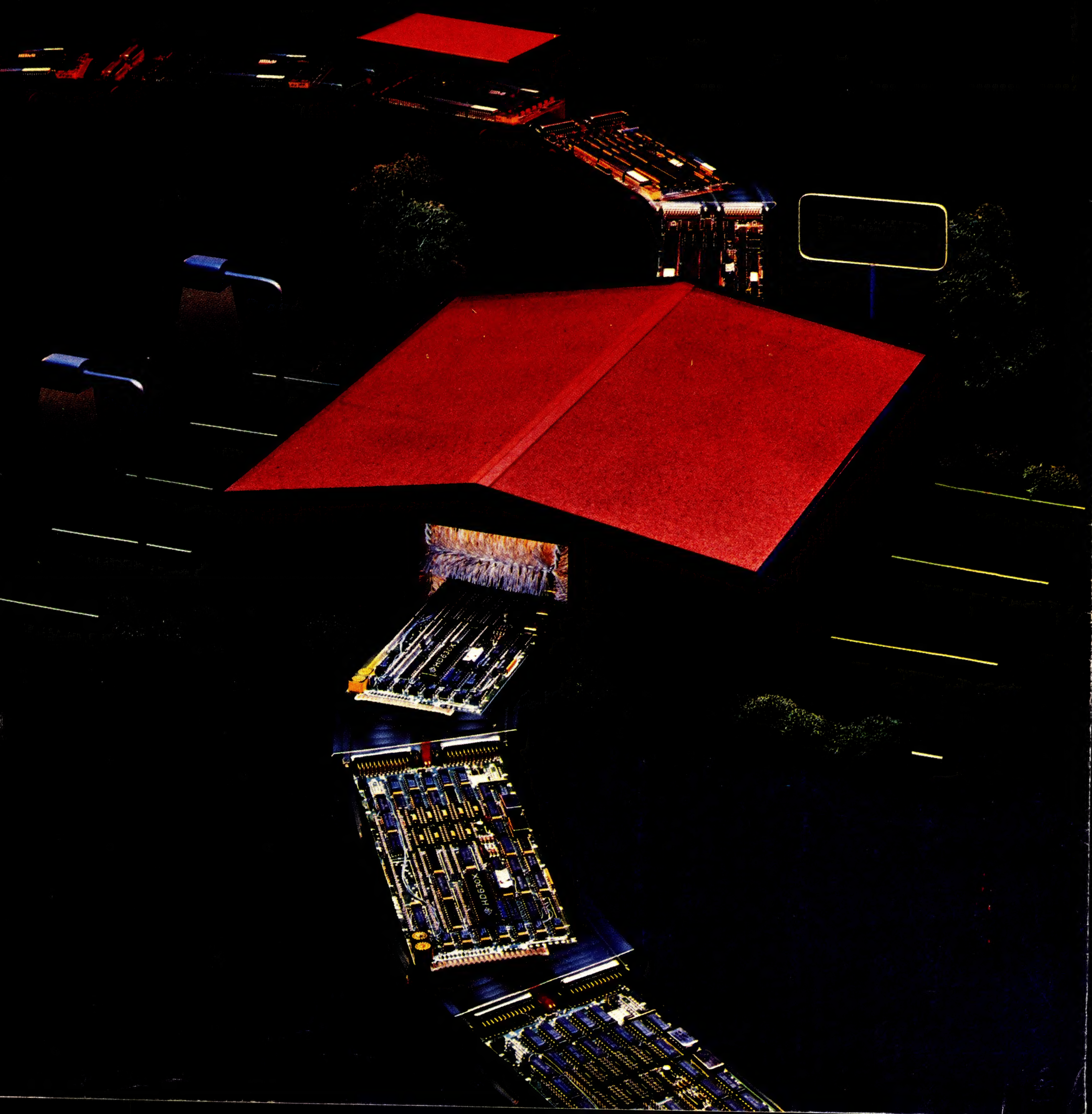
Designer's Guide to: Programmable logic—Part 1

EEPROM standardization

Article database

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Enhanced μPs clean up board designs



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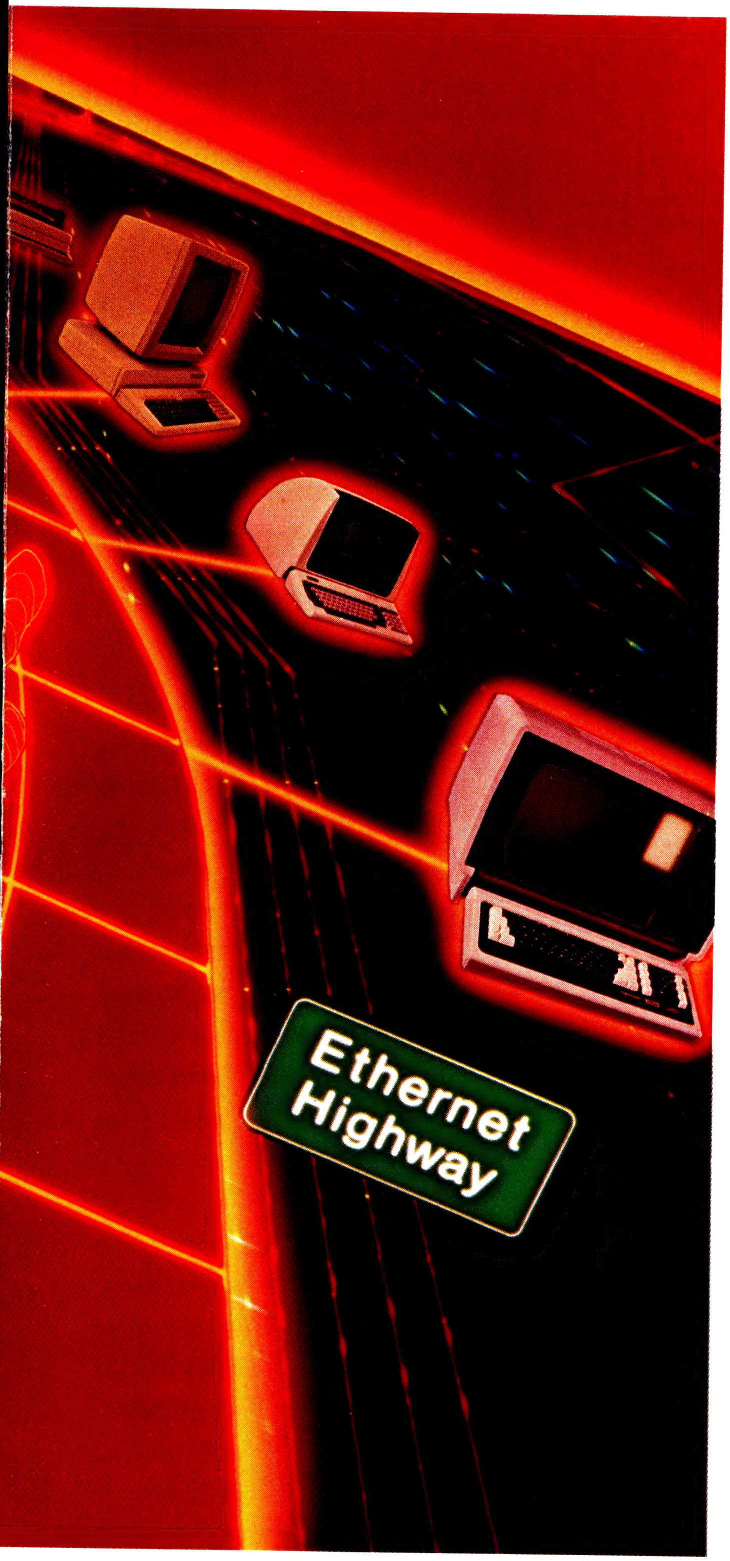

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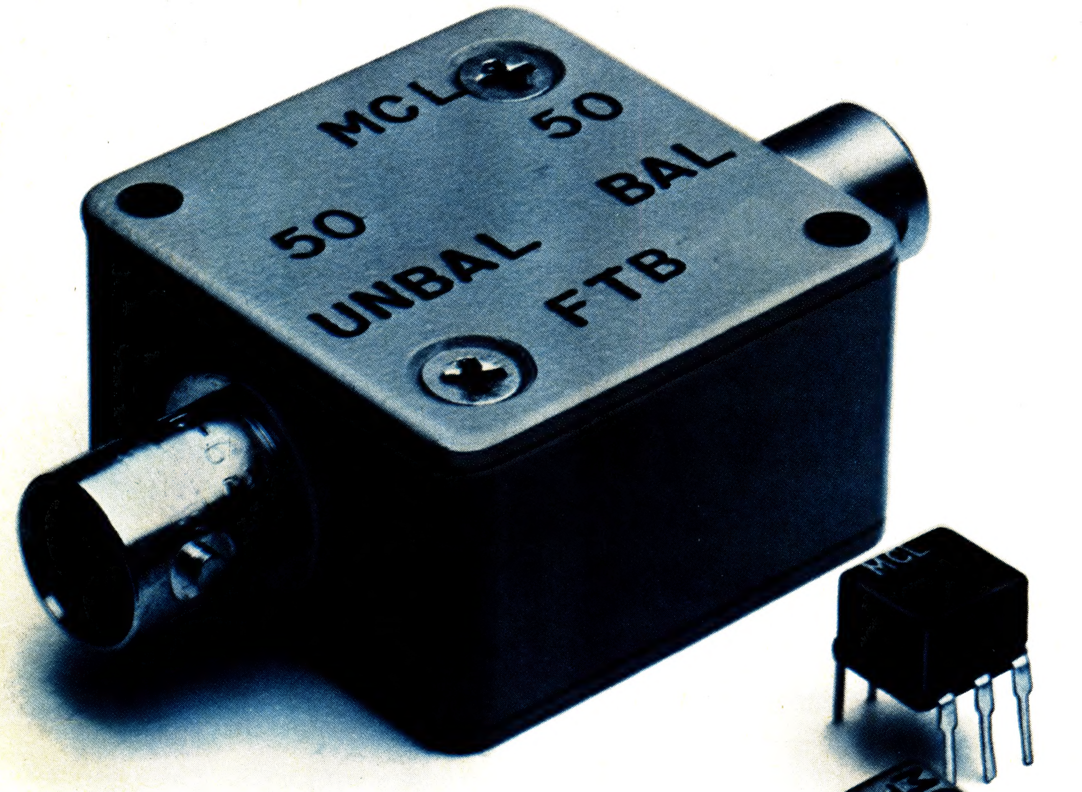

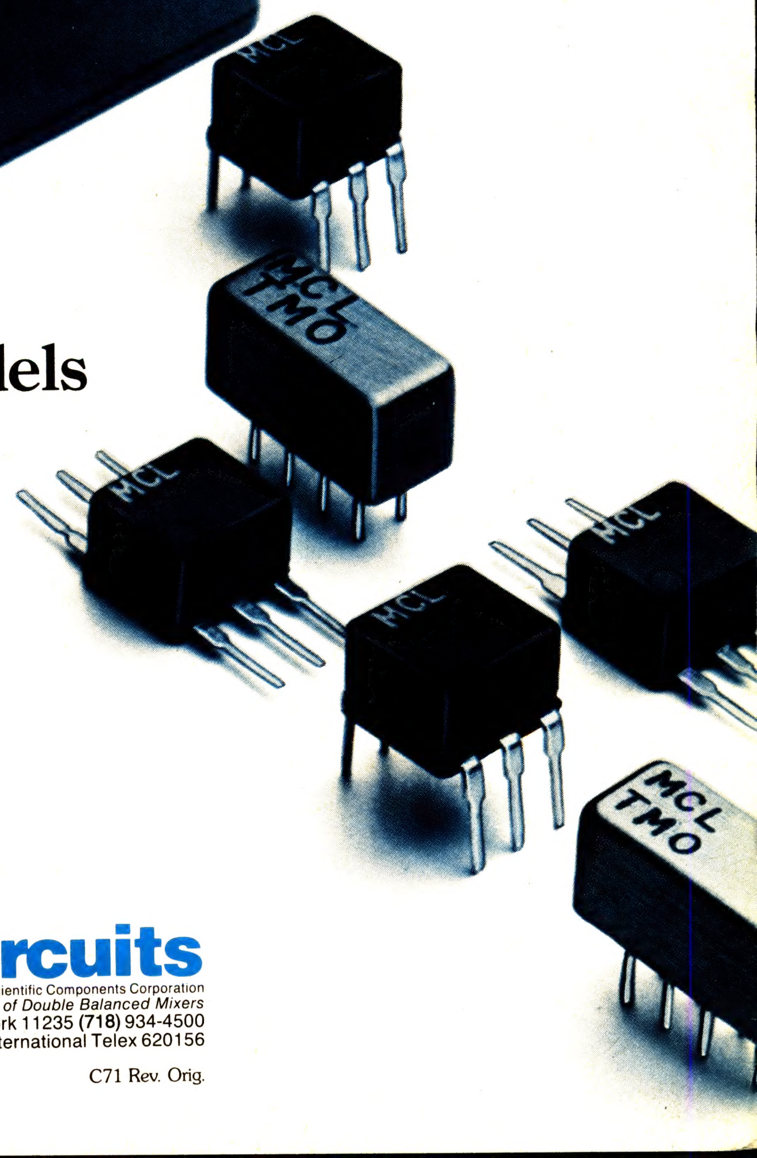

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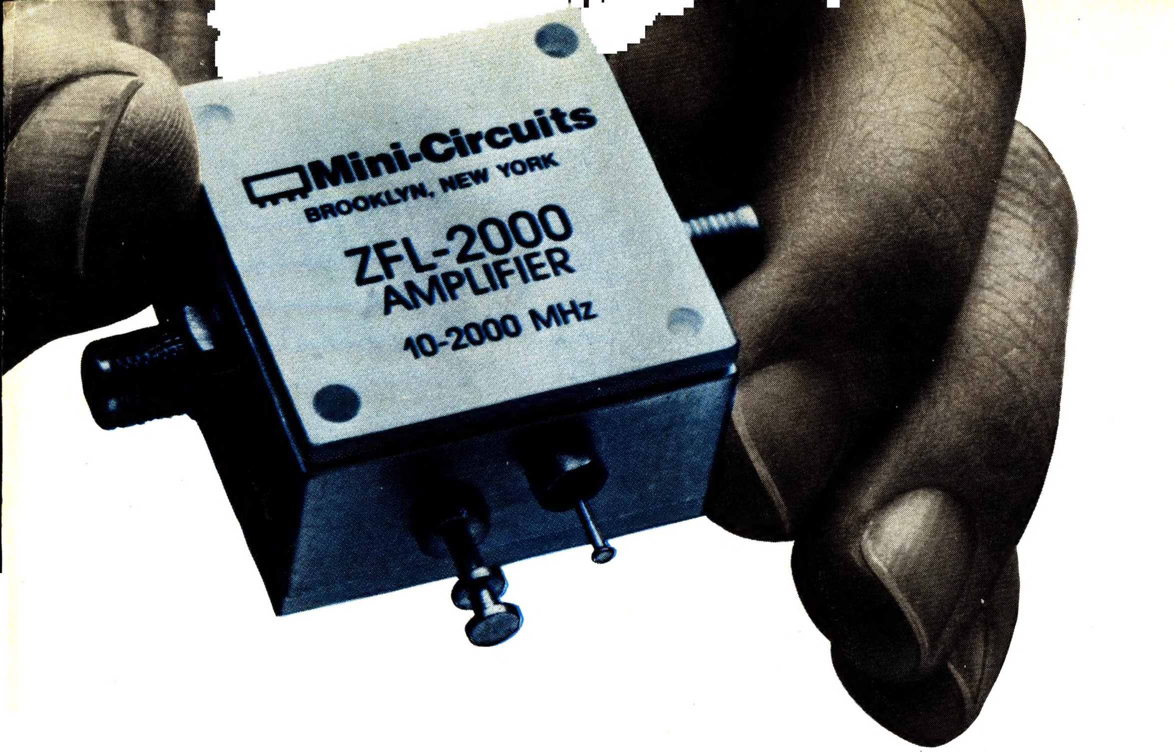

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OPERATING TEMP	−55°C to +100°C

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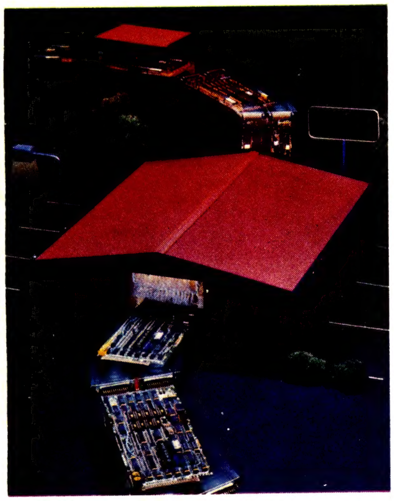
C98 REV. A

Volume 30, Number 1

EDN

January 10, 1985

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: Enhanced 8-bit μPs are capitalizing on the momentum of their popular predecessors. See pg 124. (Photo courtesy Hitachi; concept by Yashi Okita Design)

DESIGN FEATURES

EDN (ISSN 0012-7515) is published biweekly with one additional issue in January, February, March, May, August and October, and two additional issues in April, June, September and November, by Cahners Publishing Company. Division of Reed Holdings, Inc, 221 Columbus Avenue, Boston, MA 02116. Norman L Cahners, Chairman; Saul Goldweitz, President and Chief Executive Officer; Ronald G Segel, Executive Vice President and Chief Operating Officer. EDN is published by the Cahners Magazine Division; J A Sheehan, President; William Platt, Executive VP. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN, 270 St Paul St, Denver, CO 80206.

Continued on page 7

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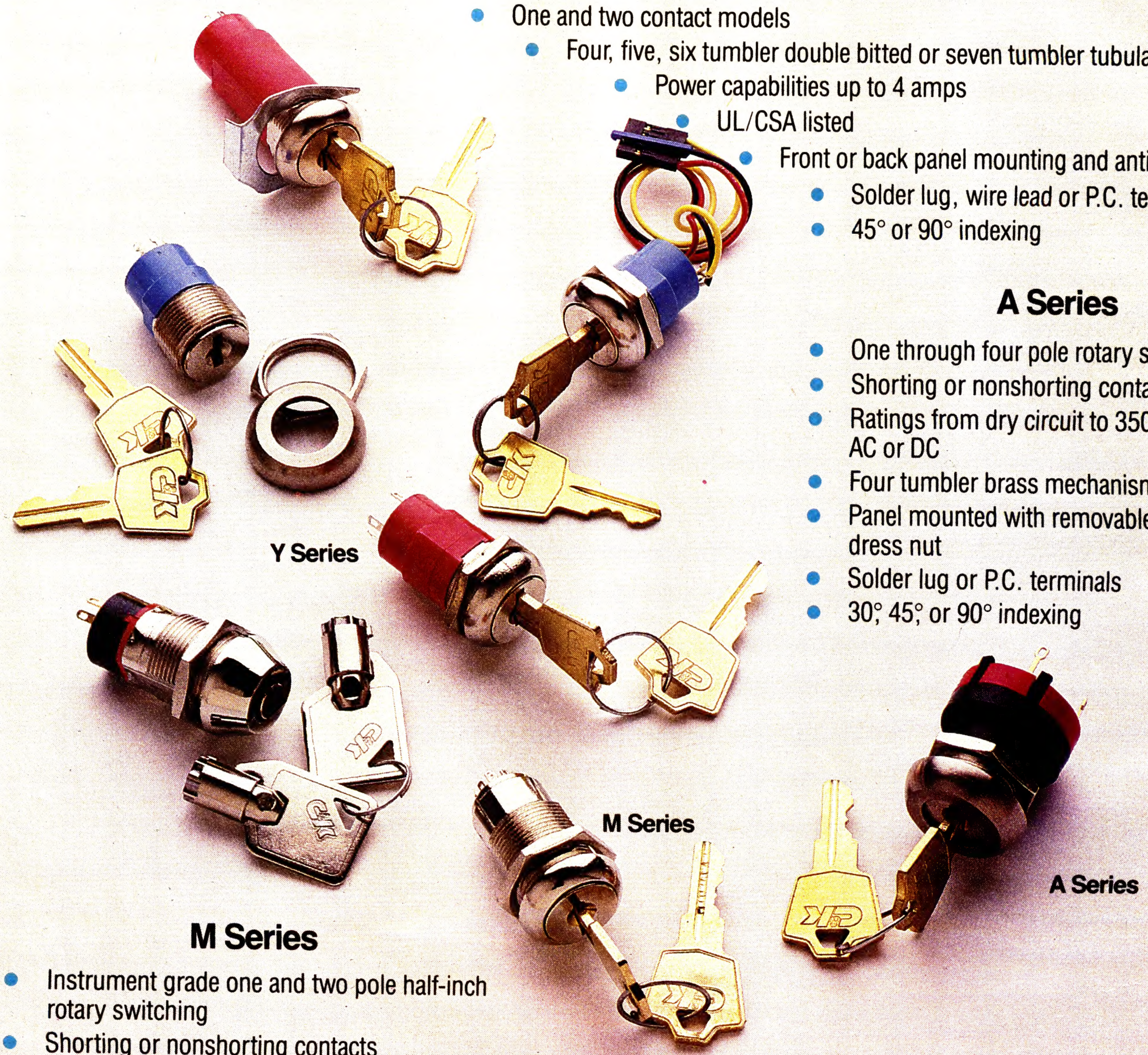

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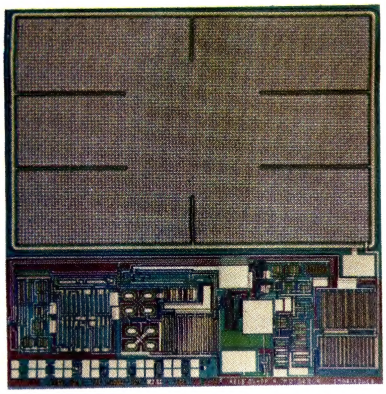
Continued from page 5



Emerging mixed-technology products based on CMOS plus bipolar or power-MOSFET processing are combining logic functions and high-current-output capability on one chip (pg 51).

You can employ a variety of techniques to make your products conform to FCC-dictated EMI/RFI regulations. When choosing shielding materials, consider shielding effectiveness, cost, bulk, weight and appearance (pg 83).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

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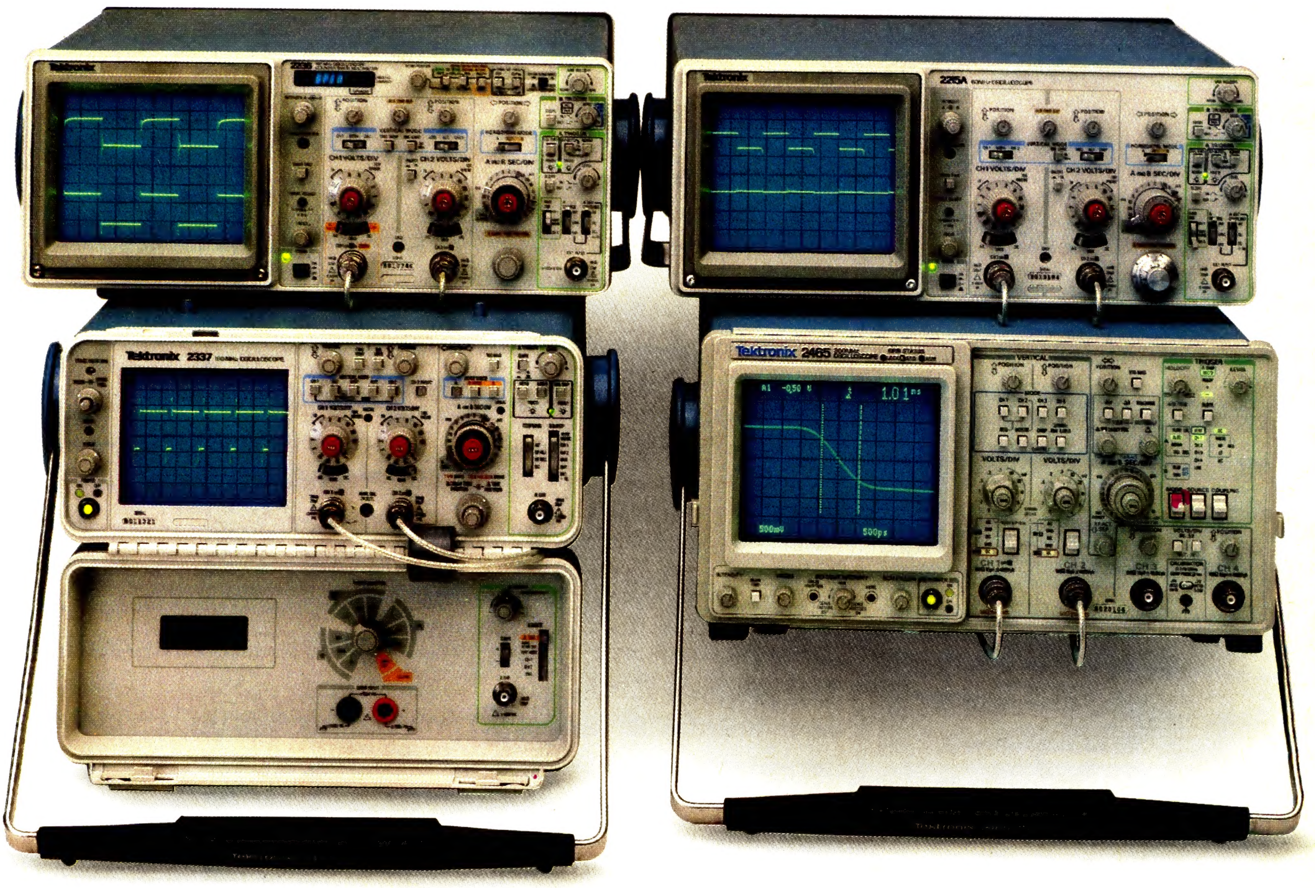

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January 10, 1985

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EDITORIAL 45

Far too many engineers, during the middle years of what should be long and rewarding careers, work at unchallenging assignments that barely utilize their technical skills. But are engineers themselves solely to blame?

NEW PRODUCTS

PROFESSIONAL ISSUES

LOOKING AHEAD 406

μC suppliers step up pursuit of OEMs and VARs. . . Programmable controllers give way to industrial μCs.

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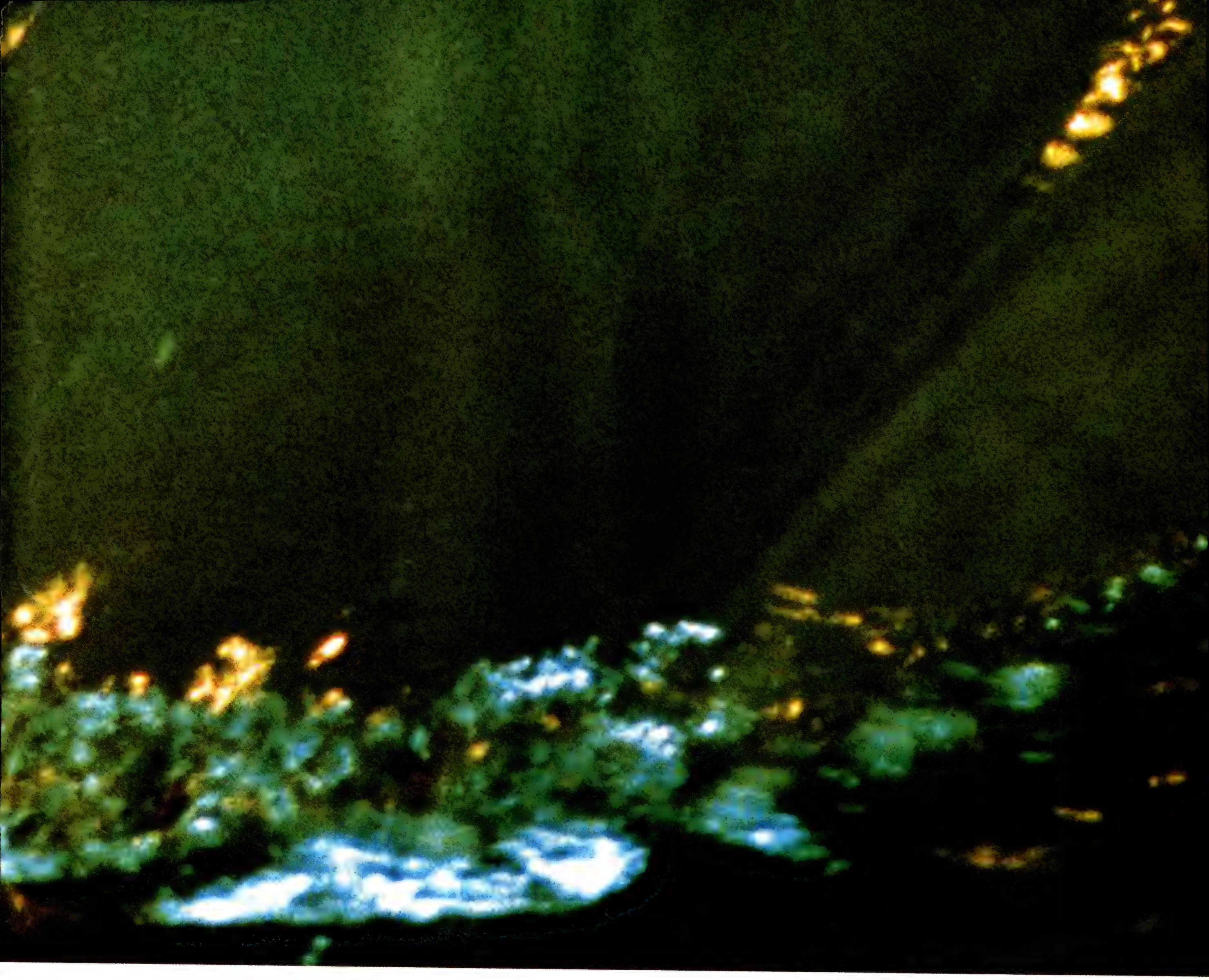

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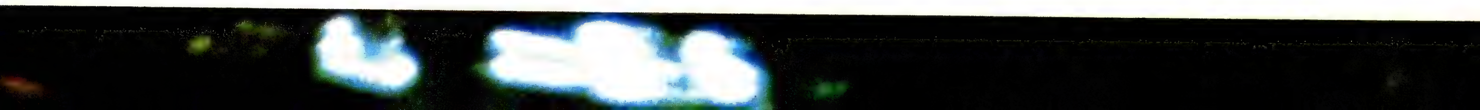

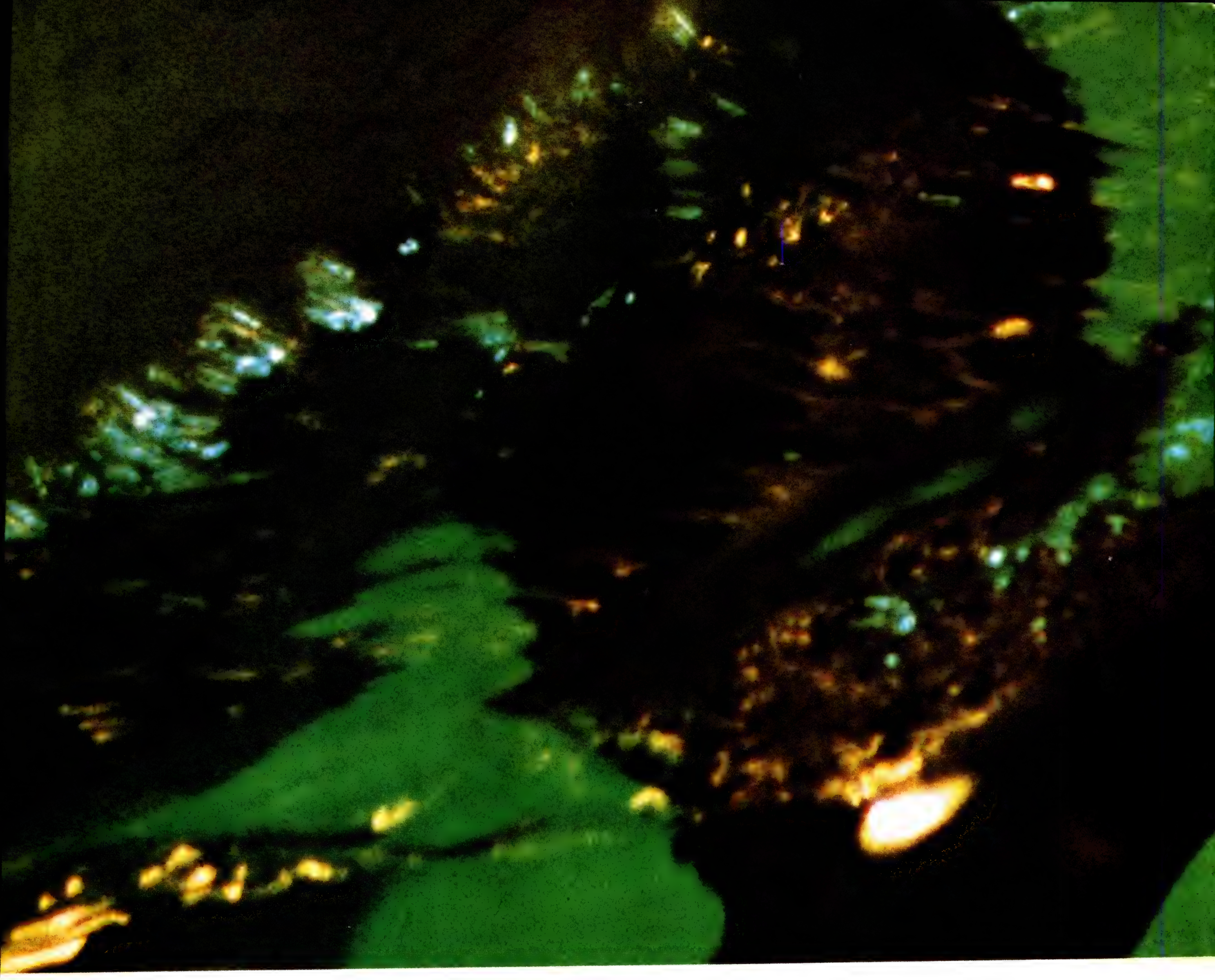

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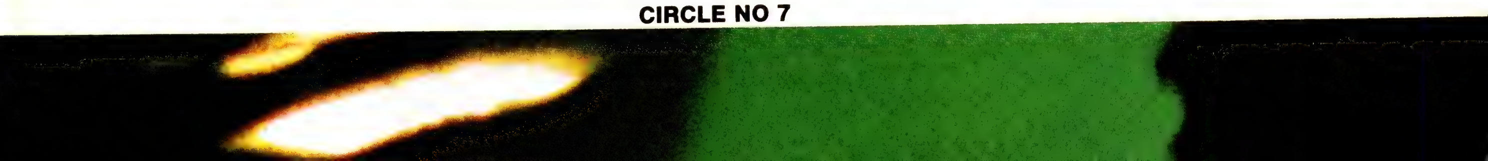

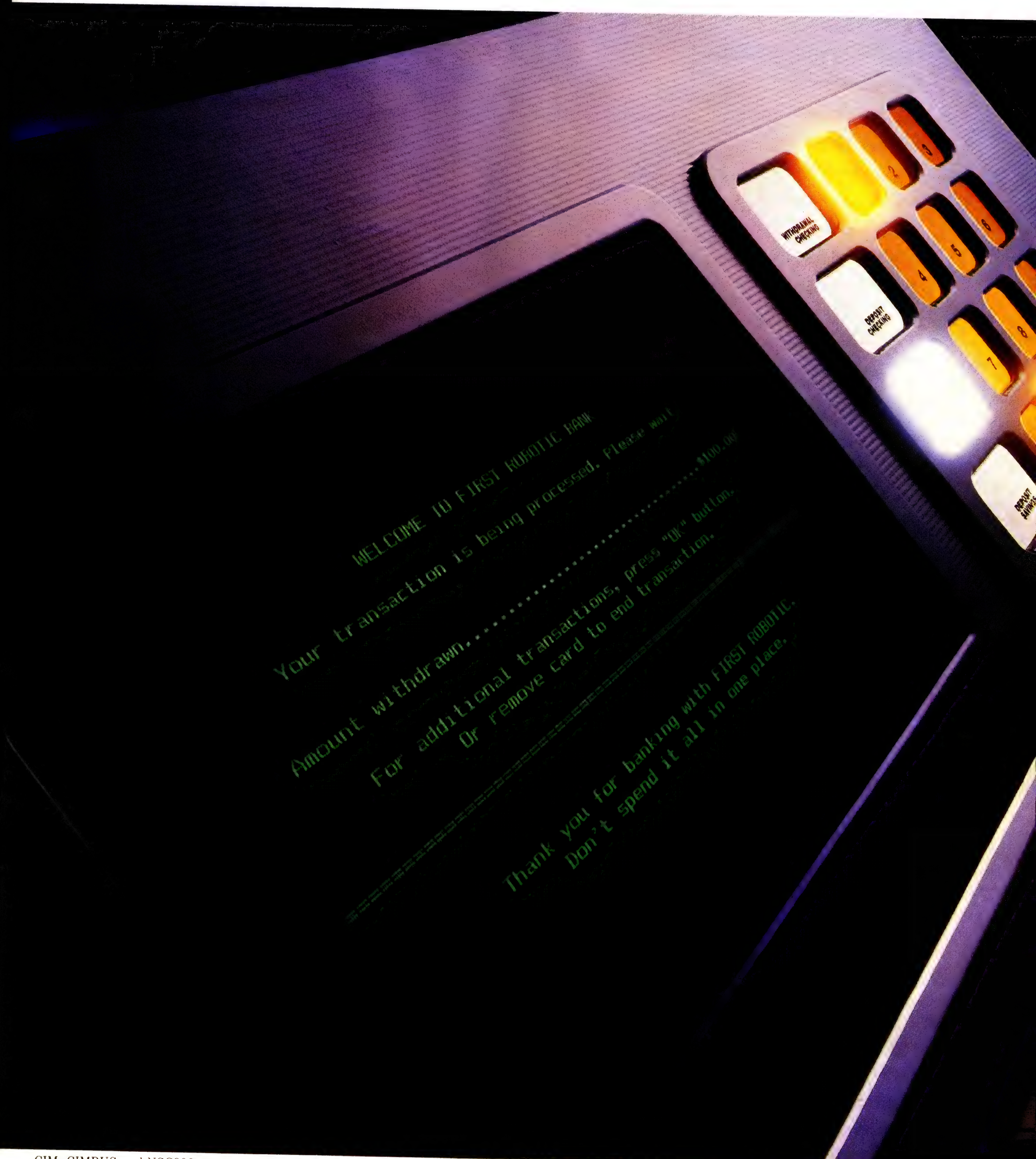

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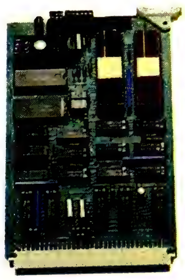

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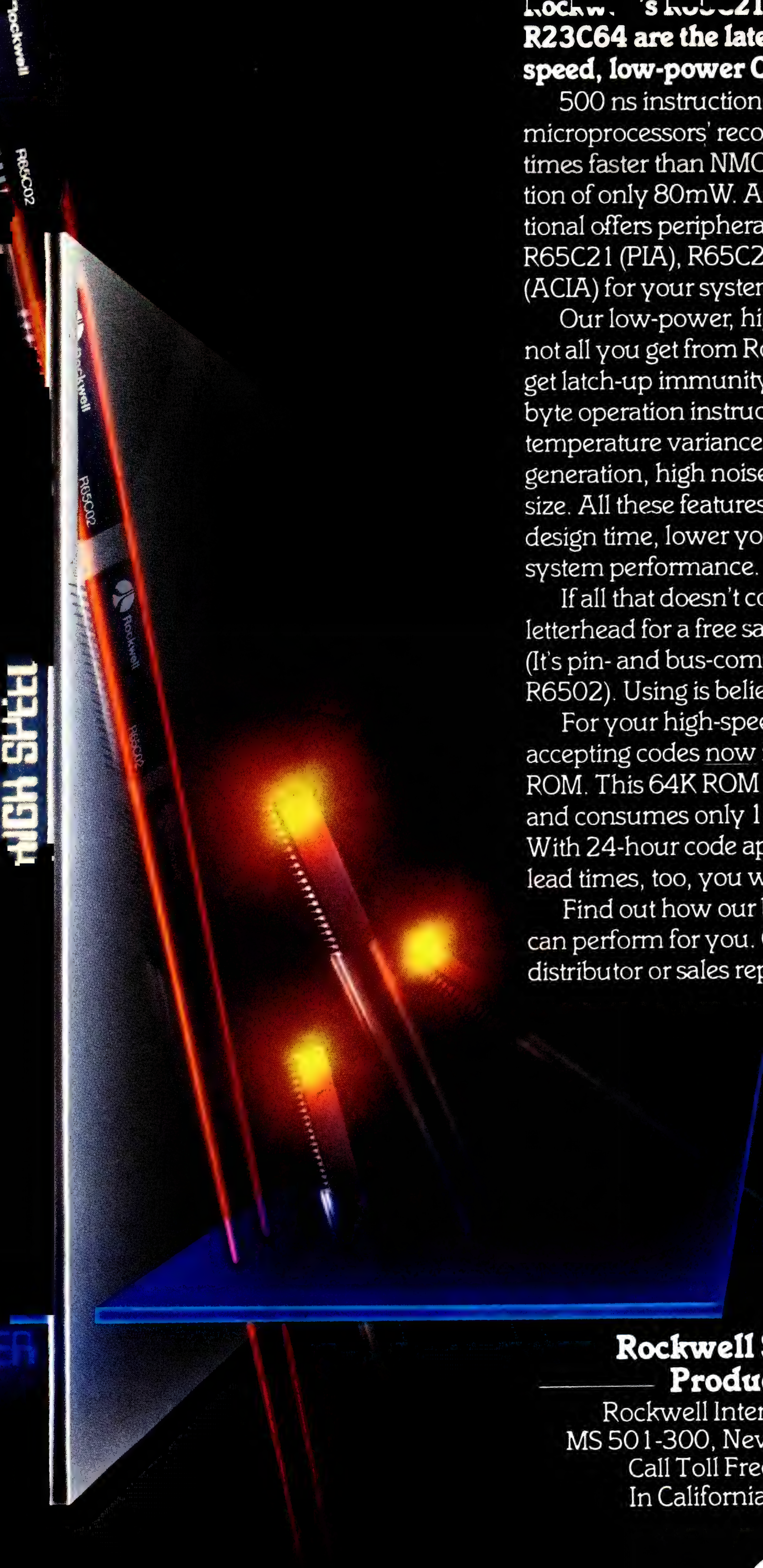

Rockwell's R65C21, R65C24, R65C51 and R23C64 are the latest members of our high-speed, low-power CMOS family.

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CIRCLE NO 10

NEWS BREAKS

EDITED BY JOAN MORROW

SEMICONDUCTOR MARKET SOFTENS AS BUYERS TRIM ORDERS

Semiconductor manufacturers received just $67 in orders for every $100 in products they shipped in October, according to the Semiconductor Industry Association (SIA). That figure translates to a book-to-bill ratio of 0.67 for October, a steep drop from the healthy 1.53 ratio reported in January 1984. The decline in orders is expected to continue as semiconductor users try to reduce the large inventories accumulated during the spending spree of late 1983 and early 1984. Canceled orders and postponed delivery schedules caused October billings to decline 12% compared with billings for September.

"While the short-term situation is of great concern to the industry, we believe that the underlying fundamentals of the economy will support continued long-term growth," said SIA president Thomas Hinkelman. Hinkelman said the Dept of Commerce estimates that the semiconductor industry grew 18% in 1984 and forecasts another 15% growth in 1985.—Deborah Asbrand

DEVELOPMENT GROUP CREATES CONSUMER PRODUCTS FOR OEMS

XXCAL Inc (Los Angeles, CA) has established a consumer products division that will develop and prototype peripherals and accessories for personal computers. The new division intends to license its products to major computer manufacturers. The firm's efforts will focus on technical improvements in areas such as image digitization, optical scanning, laser disks, and videotape interfacing.—Ed Teja

3-PORT MODEM HAS ADDED SECURITY AND CONTROL FUNCTIONS

The CH1763 intelligent, 212A-compatible modem uses standard DTE and phone-line signals and comes with an 8-bit parallel I/O port for computer control. Cermetek Microelectronics (Sunnyvale, CA, (408) 752-5000) puts the circuitry in a 44-pin module that provides autodialing, pulse or tone dialing, redialing, and data rates of 110, 300, or 1200 bps. The parallel port controls and tests the modem's status without disturbing normal data flow. Thirteen special control operations let system developers add extra security to a communication system. The modem supports synchronous and asynchronous protocols and is FCC approved.—Jon Titus

LAP-SIZE COMPUTER HAS IBM PC DISK COMPATIBILITY

Featuring a 5¼-in. floppy-disk drive, the 12-lb Model 25 lap computer from Datavue (Norcross, GA) gives you the ability to use IBM PC software right off the shelf. Its smoothly scrolling, 80-character × 25-line LCD yields monochrome graphics with a 640 × 200-dot resolution. Four shades of gray let the Datavue 25 support color software. The unit includes one serial and one parallel port, as well as a real-time clock and built-in battery backup. The keyboard has 10 function keys and offers cordless, infrared operation. A built-in RAM disk lets you set aside part of the computer's 640k-byte max memory as an emulated disk-storage area. You can use either the unit's ac power cord or the optional 4-hr 12V battery. The base unit provides 128k bytes of RAM for $2195.—J D Mosley

AEA TAKES PROPOSED FEDERAL TAX CHANGES TO TASK

The American Electronics Association (AEA) has outlined a 4-pronged offensive it hopes will effectively block proposed changes in the federal tax structure that it believes will harm the electronics industry. AEA senior vice president Ralph

Thomson says AEA officials have so far met with representatives of the Treasury and Commerce departments, the Office of Management and Budget, and the White House to voice their concerns.

Most vigorously opposed is a planned change in the tax on capital gains, which AEA officials claim will deplete the pool of available investment money and hurt the growth of the electronics industry. The maximum tax on capital gains is much lower than that levied on personal income in order to encourage investors to seek long-term investments. When the capital gains tax was reduced in 1978 and again in 1981, the amount of capital available from investors soared. Opponents of the increase fear that if passed, the measure will cause the investment market to dry up as it did after the increase that occurred in 1969.

Prompted by the 1984 trade deficit in electronics products, the AEA is pushing for a reduction of the federal deficit, which it hopes will boost US companies' performance in the international market. AEA officials plan continued support of a permanent 25% R&D tax credit to replace the current statute, which is scheduled to expire this year.—Deborah Asbrand

RESOLVER/DIGITAL CONVERTER PROVIDES FOUR SPEED OPTIONS

The Model 1S74 resolver/digital converter from Analog Devices (Norwood, MA) combines the four members of the firm's 1S64 Series in one 40-pin hybrid package. The four converters incorporated are the 10-, 12-, 14-, and 16-bit Models 1S14, 1S24, 1S44, and 1S64, respectively. You can choose the resolution your resolver system requires by applying appropriate logic levels to a pair of resolution-select terminals. Maximum rotational speeds attainable with the four resolution selections are, respectively, 40,800, 10,200, 2550, and 630 rpm.

The converter provides an analog tachometer/generator output that indicates the resolver's rotational speed. You can use this output for speed monitoring or as a stabilization aid in servo systems. The company claims this velocity output is as accurate as that offered by the best grade electromechanical tachometer generators. The converter is available in commercial-grade (0 to 70°C) and military-grade (−55 to +125°C) versions; the two grades cost $326 and $652, respectively.—Bill Travis

CAD/CAM SOFTWARE RUNS ON 4361 MINICOMPUTERS

McDonnell Douglas Automation Co (St Louis, MO), also known as McAuto, reached an agreement with IBM to market Unigraphics II CAD/CAM software on IBM systems. As part of the agreement, McAuto will join the family of IBM value-added remarketers. Running on IBM 4361 minicomputers, the CAD/CAM programs will feature IBM 5080 graphics terminals as entry stations.

The configuration chosen by McDonnell Douglas for Unigraphics II will take maximum advantage of the file-management and database-management utilities available in the 4361. The package specializes in 3-D modeling. McAuto will continue to support Unigraphics II on Digital Equipment Corp and Data General systems. In a typical 4-workstation arrangement, the CAD/CAM package, including the IBM hardware, will cost $600,000.—Eva Freeman

300k-BYTE MICROWAFER DRIVE OFFERS 21k-BPS DATA RATE

Bridging the gap between disk- and tape-drive systems, the Model 201 microwafer system from Entrepo (Sunnyvale, CA) provides low-cost, high-performance data

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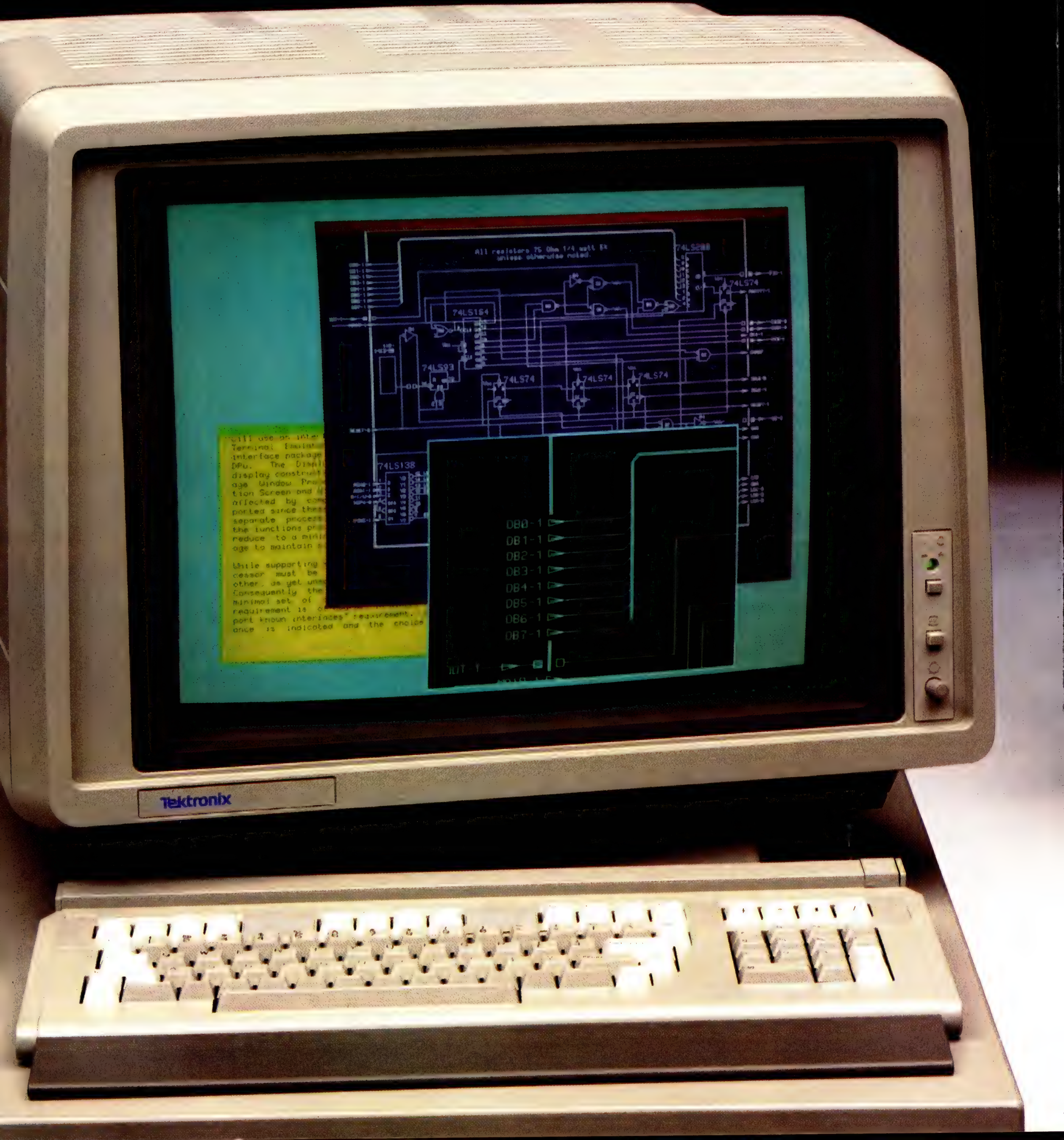

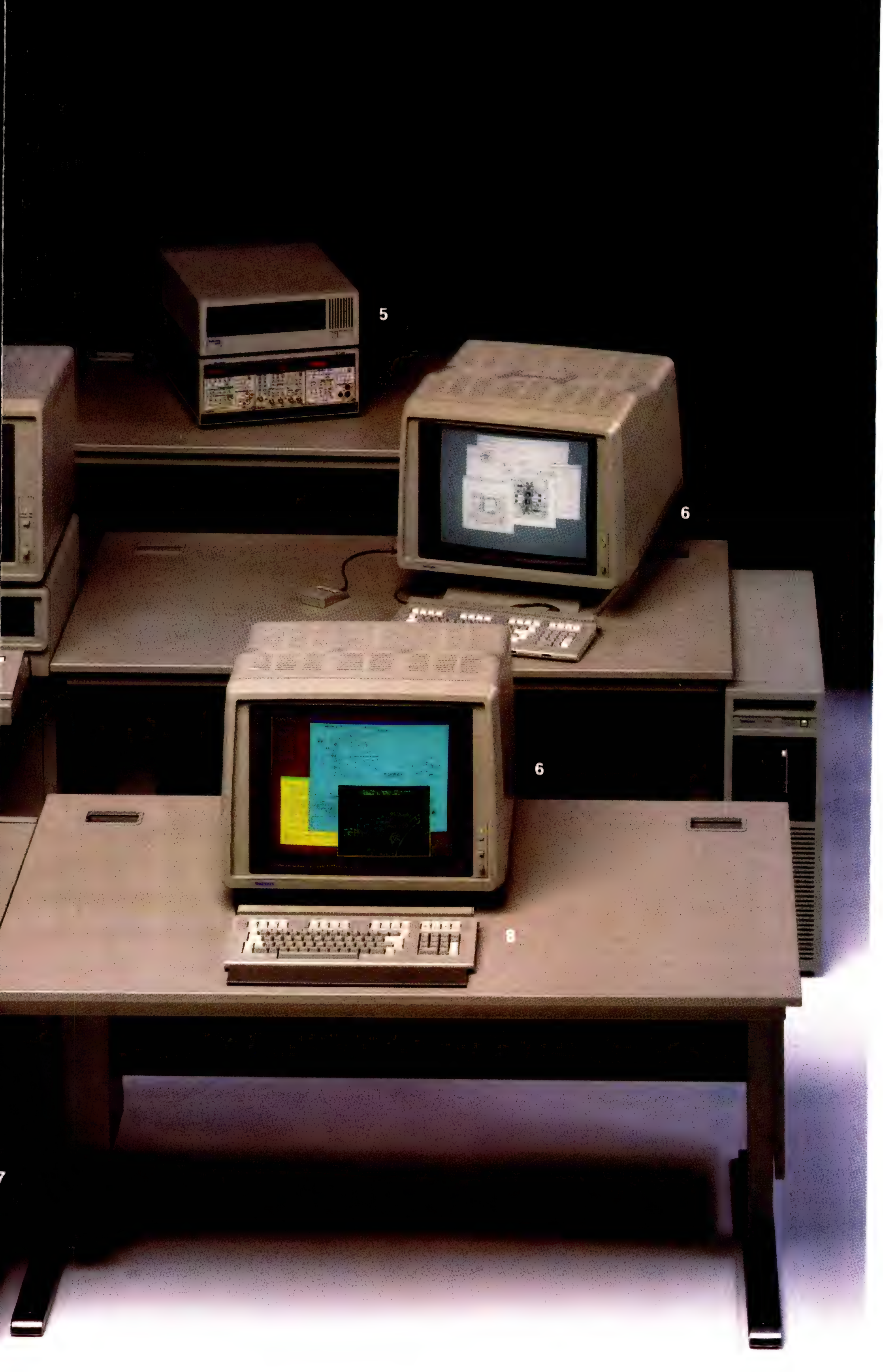

Photo Left: In the Tek 6000 Family, you can choose from the broadest, most compatible, most powerful array of workstations ever. You can select, configure and expand to fit the exact needs of every task and every member of the team; continue to utilize your host-based software and existing graphics terminals; and expedite documentation and manage data independently of specific programs, using Tek's excellent, integral software tools.

1. Tek 4107 terminal in-use with PLOT 10 TekniCAD Computer-Aided Drafting package.
2. Low-cost, personal UNIX system configuration.
3. Peripheral cabinet houses 9-track tape and SMD disks.
4. Tek 4115B terminal integrated into workstation.
5. Instrument controller with real-time operating system.
6. New window-managed displays help deliver the full benefits of multiprocessing.
7. Tek 6200 dual-wide configuration enables limitless expansion.
8. Keyboards, displays and display stands all incorporate human engineering at its best.

ries, Inc., International Business Machines, Intel Corporation, and National Semiconductor. 4115B display courtesy of PDA Engineering

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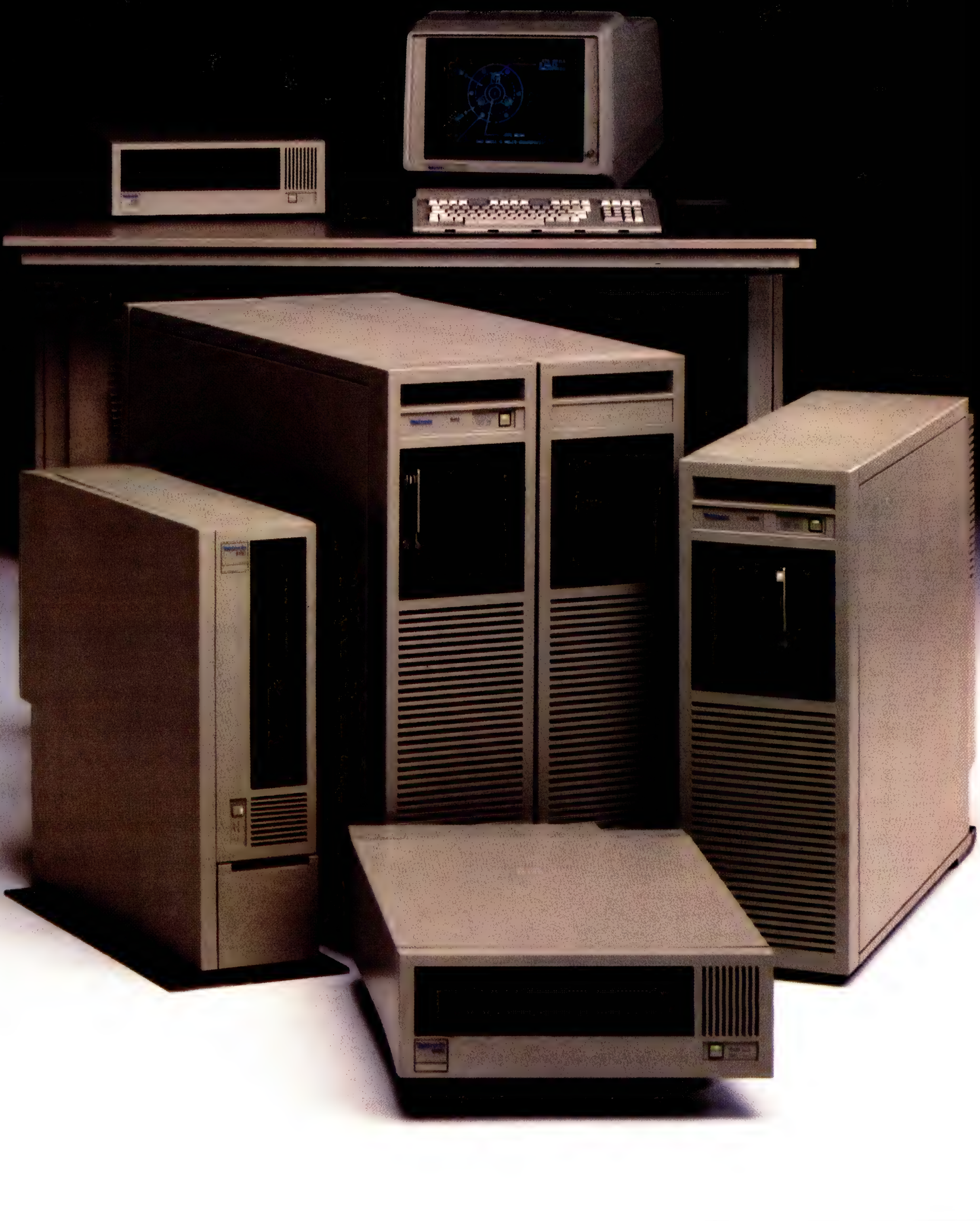

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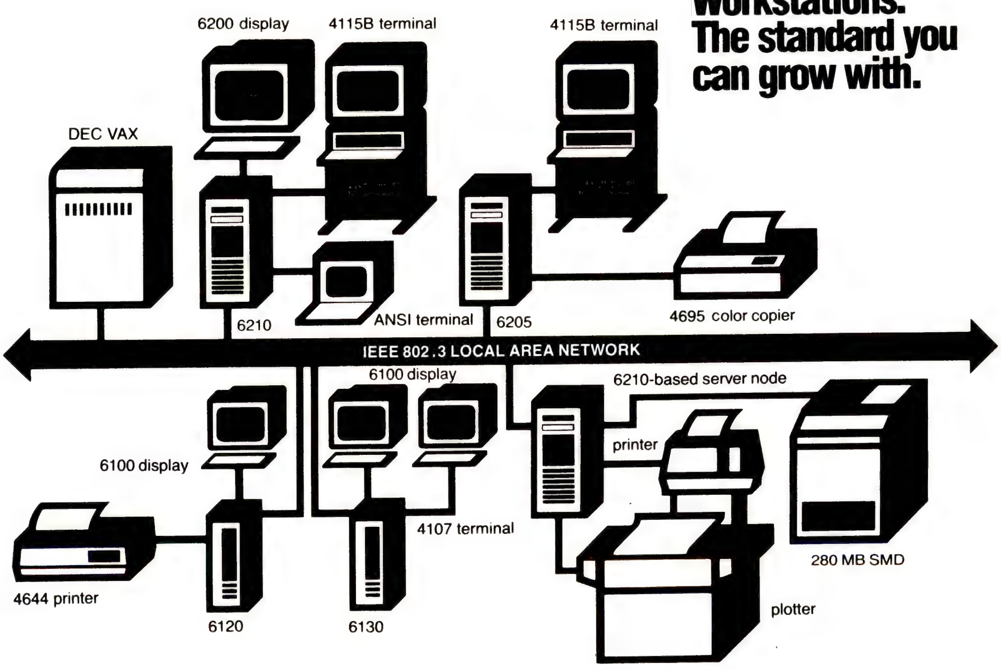

The 6000 Family's LAN supports communications with other workstations and selected hosts, peripheral sharing, electronic mail, and a distributed file system

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A CONCISE COMPARISON OF THE 6000 FAMILY

		6110	6120/6130	6205/6210	6212
Processors		32016 CPU	32016 CPU 32081 FP Processor	32016 CPU (6205) 32032 CPU (6210) 32016 I/O Processor 32081 FP Processor	Dual 32032 CPUs 32016 I/O Processor 32081 FP Processor
	Optional		PC Co-Processor	32032 CPU (6210)	
Memory		256 KB	1 MB	1 MB	4 MB
	Optional/Additional	512 KB, or 1 MB	2 MB	9 MB	16 MB
Storage		360 KB diskette	360 KB diskette 10 MB Winchester (6120) 20 MB Winchester (6130)	40 MB Winchester	80 MB Winchester
	Optional	10 MB Winchester	20 MB (6120) 40 MB, or 80 MB Winchester (subs) External 40 MB cartridge tape	40 MB or 80 MB Winchester 40 MB cartridge tape 9-track tape 280 MB SMD disks (1.1 GB max) 360 KB diskettes	40 MB or 80 MB Winchester 40 MB cartridge tape 9-track tape 280 MB SMD disks (1.1 GB max) 360 KB diskettes
Interface Ports		RS-232C (2) GPIB LAN	RS-232C (2) GPIB LAN	RS-232/RS-422 RS-232C (3) LAN, 8-bit parallel	RS-232/RS-422 RS-232C (3) LAN, 8-bit parallel
	Optional	High-speed GPIB & Serial 8-bit & 24-bit parallel Multibus adaptor Additional Dual RS-232	High-speed GPIB & Serial 8-bit & 24-bit parallel SCSI Multibus adaptor Additional Dual RS-232	High-speed Serial Multibus adaptor	High-speed Serial Multibus adaptor
Display Options			6100 Series: 13 in. 640 x 480 color 13 in. 640 x 480 monochrome 4010, 4100, 4110 Series	6200 Series: 19 in. 1024 x 768 color 19 in. 1024 x 768 monochrome 4010, 4100, 4110 Series	6200 Series: 19 in. 1024 x 768 color 19 in. 1024 x 768 monochrome 4010, 4100, 4110 Series
Peripheral Options					
	4644 Dot Matrix Printer	yes	yes	yes	yes
	4695 Color Graphics Copier	yes	yes	yes	yes
Operating Systems		RTOS	Proposed ANSI BASIC (6120) Mini-UTEK (subset) (6120) UTEK* (6130)	UTEK*	UTEK*
	Optional		UTEK* (6120) PC Co-Processor Support		
Languages			Proposed ANSI BASIC (6120)		
	Optional	Executes object code From FORTRAN 77, C, ISO Pascal and Proposed ANSI BASIC	C ISO Pascal Enhanced FORTRAN 77 Proposed ANSI BASIC (6130)	C ISO Pascal Enhanced FORTRAN 77 Proposed ANSI BASIC	C ISO Pascal Enhanced FORTRAN 77 Proposed ANSI BASIC
Graphics Libraries			GKS Level 0b (subset 6120)		
	Optional		GKS Level 3c (6130) PLOT 10 IGL & TCS PLOT 10 TekniCAD (6130)	GKS Level 3c PLOT 10 IGL & TCS PLOT 10 TekniCAD	GKS Level 3c PLOT 10 IGL & TCS PLOT 10 TekniCAD
General Purpose Software Options					
	Statistics	N/A	yes	yes	yes
	Document Processors	N/A	yes	yes	yes
	Graphics Editor	N/A	N/A (6120) yes (6130)	yes	yes
	Project Manager	N/A	N/A (6120) yes (6130)	yes	yes
	Spreadsheet	N/A	yes	yes	yes
	Database Manager	N/A	N/A (6120) yes (6130)	yes	yes

*UTEK is based on the BSD 4.2 UNIX operating system plus System V enhancements.

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storage in a compact 3 × 1½ × 1-in. unit that operates from one 5V power supply. Because of the drive's MFM encoding/decoding scheme, Model 201's removable endless-loop microwafer data cartridges have an unformatted data capacity of 300k bytes, which translates into 256k bytes of formatted data storage. The system also features an average access time that's less than 8 sec for 64k bytes of data. The $25 (OEM qty) 201 is an alternative to tape-recording systems commonly used with low-end μCs. A built-in write-protect mechanism ensures data integrity.—J D Mosley

SERVICE BUREAU CUTS PC-BOARD TURNAROUND

By combining experienced designers, CAD software, and a fiber-optics photoplotter, Design Express (Pasadena, CA) designs pc boards in about half the time taken by typical service bureaus. The firm designs boards using the Calay V03 system. Design Express handles pc boards of any size and can accommodate analog, ECL, and surface-mount devices in designs.—Eva Freeman

SINGLE-BOARD COMPUTER USES NS32032 32-BIT CPU

The GS-32 single-board supermicrocomputer from Goodspeed Systems (East Haddam, CT) uses National Semiconductors' NS32000 Series μPs. The μC can operate with either the NS32016, which has 32-bit internal and 16-bit external data buses, or the NS32032, the full 32-bit CPU. To substitute the readily available NS32016 with the more powerful NS32032, you need only move one jumper: The change is 100% software transparent. The $5500 GS-32 also includes the NS32081 floating-point unit, the NS32021 timing-control unit, and the NS32082 memory-management unit. As a result, you can configure the GS-32 for multiuser and multitasking systems.

Complementing the central-processing chips are an onboard memory and a Z80B microprocessor that controls I/O operations. You can increase the installed RAM from 512k bytes to 2M bytes by substituting the 64k-bit chips with 256k-bit devices. The Z80B accesses all of the RAM in addition to six serial-I/O channels, 32 parallel lines, as many as four floppy-disk drives, and a SCSI port. —David Smith

SINGLE-BOARD COMPUTER EXECUTES IBM PC SOFTWARE

A new family of single-board computers from Mostron Inc (Milpitas, CA, (408) 946-1727) will take IBM PC compatibility into industrial applications. Intended for process-control and industrial applications, the boards provide an 8088 CPU and math coprocessor; much of the logic comes in proprietary CMOS gate arrays. The boards cost approximately $500 (OEM).—Ed Teja

TELECOMM-IC FIRMS INK DUAL-SOURCING AGREEMENT

Under the terms of a bilateral dual-sourcing agreement, Gould AMI (Santa Clara, CA) and Mitel Corp (Kanata, Ontario, Canada) will exchange designs for their lines of telecommunication ICs. Mitel will produce Gould AMI's series of 300- and 1200-baud modem chips, including the S3530 300-baud modem, the S35212A 1200-bps modem filter, a future 1200-bps modem, and various call-progress monitoring devices. In exchange, Gould AMI will become a second source for Mitel's MT8980/81 digital time/space crosspoint switches, the MT8975 T1 trunk interface, the MT8978 CCITT-standard trunk interface, the MT8940 T1 digital phase-lock loop, and the MT8970 digital line-interface circuit. According to Mitel's vice president of marketing John Freeman, Gould AMI's second sourcing of his firm's products is a strong endorsement of the ST-bus (Serial Telecom), a system bus designed for the digital communication of data, voice, and control messages.—Bill Travis

NEWS BREAKS

MOSAIC ARRAYS SPEED MACRO-BASED LINEAR DESIGNS

By arranging on-chip components into an orderly mosaic-like structure, the FB300 Series of linear arrays from Micro Linear Corp (San Jose, CA) allows you to design linear circuits using a macrocell library that translates directly into predefined layout. Using Micro Linear's Linear Cad I software for the IBM PC, you can design circuits using these macros much as you would design digital semicustom ICs. Because the macrocells translate into precharacterized layout, you benefit from accurate simulations and reduced turnaround time (six weeks from simulated schematic to prototypes). The library currently includes 24 macrocells with linear and digital functions.—David Smith

PC-COMPATIBLE CAE/CAD SOFTWARE AVAILABLE FOR RENT

US Instrument Rentals (San Mateo, CA) has signed a 1-year renewable agreement with Personal CAD Systems (Los Gatos, CA), giving USIR exclusive rental rights to P-CAD products. CAE/CAD programs from P-CAD run on IBM PCs and PC-compatible machines. As part of the agreement, P-CAD will supply USIR with software updates, including new programs and revisions.

Leases for pc-board-design packages start at $295/month, while schematic-entry leases begins at $250/month. IBM PC/XT and IBM PC/AT systems cost $360 and $375/month, respectively, in a leasing arrangement. —Eva Freeman

COMPANY SELLS MULTIBUS-BOARD LINE

After announcing on October 8, 1984 that it would discontinue its board-level and system-development business, Advanced Micro Devices agreed to sell its assets in Multibus board-level products to Central Data Corp (Champaign, IL). The agreement calls for Central Data to purchase manufacturing rights, design information and documentation, manufacturing equipment, raw materials, and marketable inventory. Also, Central Data agrees to provide service and warranty coverage for the existing base of AMD board-level products.—David Smith

COMMUNICATIONS PROTOCOL TESTER PROVIDES REMOTE OPERATION

The Chameleon II, a portable data-communications protocol simulator/analyzer from Tekelec (Calabasas, CA), now offers automatic remote operation, real-time analysis, automatic program loading, and simplified menu presentations. The Chameleon II provides 12 upgraded and three new protocol-support software packages that let you create protocol violations and wrong-state commands at will for certification testing. You can also perform SDLC and X.25 statistical analysis, as well as direct-to-disk analysis using the unit's two 3½-in. microfloppy drives. Simulation trace capabilities let you play back data through the X.25 or SNA trace for frame interpretation. The basic system costs $19,500 with dual disk drives, 74k bytes of RAM, 40k bytes of PROM, and full EIA-interface status LEDs.—J D Mosley

DATA-COMMUNICATIONS LINE EXPANDS ETHERNET SUPPORT

The Everyware open network now offers IEEE-802.3 Ethernet support for Xelos, an AT&T Unix System V-based operating system. You can also obtain SNA/3270 terminal support and use the BSC bisynchronous communication gateway for 3270 terminal support. The Ethernet Terminal Server (ETS) now provides access to as many as 32 RS-232C interfaces, peripherals, and computers on one LAN, including the ability to download ETS facilities from the host. Everyware was developed by Perkin-Elmer (Oceanport, NJ) to support Unix, SNA, and ISO-OSI Ethernet standards.—J D Mosley

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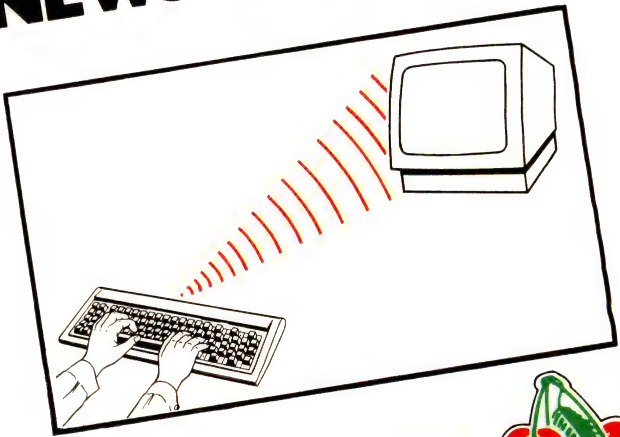

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NEWS BREAKS: INTERNATIONAL

EDITED BY JOAN MORROW

LAP-SIZE COMPUTER TO FEATURE 2000-CHARACTER LCD

Fujitsu is expected to introduce a 2.7-kg computer that will feature an LCD with 640 × 200-dot graphics capability. The LCD will be able to display 2000 alphanumeric characters or 40 × 11 Kanji characters. The 16-bit machine will employ Digital Research's CP/M-86 operating system. Fujitsu will test-market the computer in Japan before exporting it to overseas markets.

IBM JAPAN INTRODUCES ITS FIRST HOME COMPUTER

The IBM JX from IBM Japan features a display capacity of 640 × 200 dots in 16 colors or a 720 × 512-dot high-resolution mode when a ROM cartridge is used. The new system, IBM Japan's first home computer designed for the Japanese market, is manufacturered by Matsushita Electric Industrial Co.

The 64k-byte main memory is expandable to 512k bytes of RAM. A 128k-byte ROM gives the computer Kana-Kanji conversion, a Kanji dictionary, and a Japanese-language Basic interpreter. The computer can interface with two 3½-in. floppy-disk drives. Priced from $678 (¥ 166,000) to $1522, the machine will run IBM PC programs if a separate ROM cartridge is used.

HIGH-DENSITY LCD AIMED AT US MARKET

Seiko Denshi Kogyo has begun sampling its high-density dot-matrix LCDs in the US, with the goal of capturing 20 to 30% of the LCD market in two to three years. The F642D's panel measures 285 × 122 mm and consists of 128,000 picture elements. Production starts early this year at a projected annual rate of 200,000 devices; in two to three years, Seiko hopes to export the LCD to the US at an annual rate of 500,000 units.

LCD TABLET SERVES AS DISPLAY AND COMPUTER-INPUT DEVICE

Hitachi has developed a liquid-crystal display tablet that serves as a display unit and a computer-input device for characters and graphics. It consists of an electromagnetic tablet joined to a 640 × 200-dot large-area LCD. Characters and graphics can be written onto the input device with an electromagnetic stylus pen. It will accept as many as 2300 characters (including Kanji, Kana, and alphanumerics) and recognize characters at a speed of 0.2 to 1 sec/character. It can also recognize 30 types of flowchart graphics and read them in 0.5 sec. Recognition rate is claimed to be 99.5% for characters, 95% for graphics. After verifying the input, the display will reproduce a clean copy of the hand-written inputs in approximately 1 sec. Hitachi hopes to commercialize the tablet in one or two years.

1M-BIT DYNAMIC RAM FEATURES 70-NSEC ACCESS TIME

Toshiba Corp has become the sixth Japanese company to announce a 1M-bit dynamic RAM. The device, which furnishes a 70-nsec access time, uses a 1.2-μm design rule and the firm's buried-oxide isolation technology for isolating the devices integrated onto the chip. Toshiba says it will be able to mass produce the dynamic RAM in two years.

The firm also claims that the device is designed so that it can be easily housed in a plastic package. The chip comes in a 30-mil, 18-pin standard dual-in-line package, which is the standard size used for 256k-bit dynamic RAMs. The 4.78 × 13.23-mm chip uses dual-layer polysilicon and dual-layer aluminum interconnect technologies. Power consumption is 270 mW during operation and 15 mW during standby.

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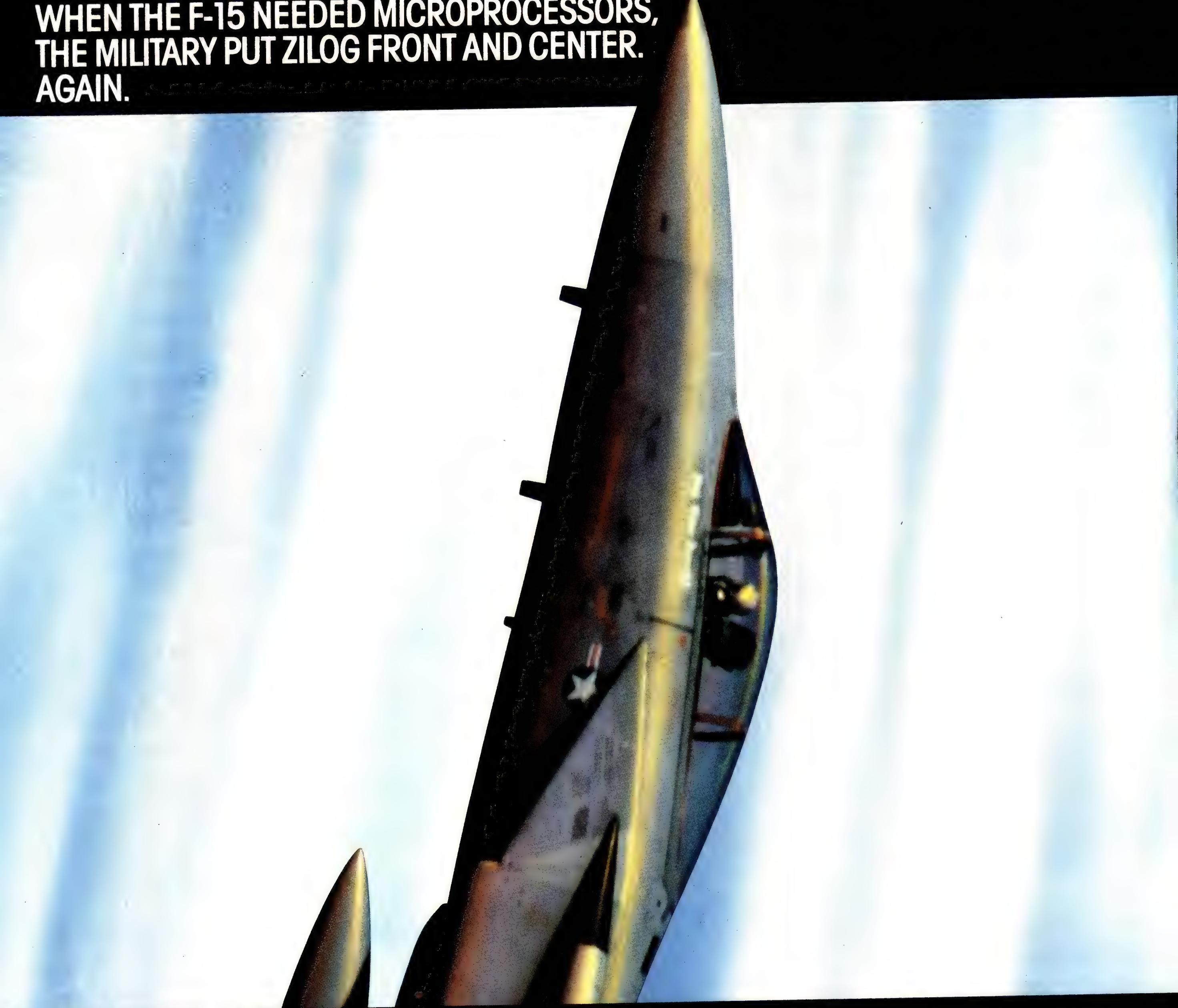

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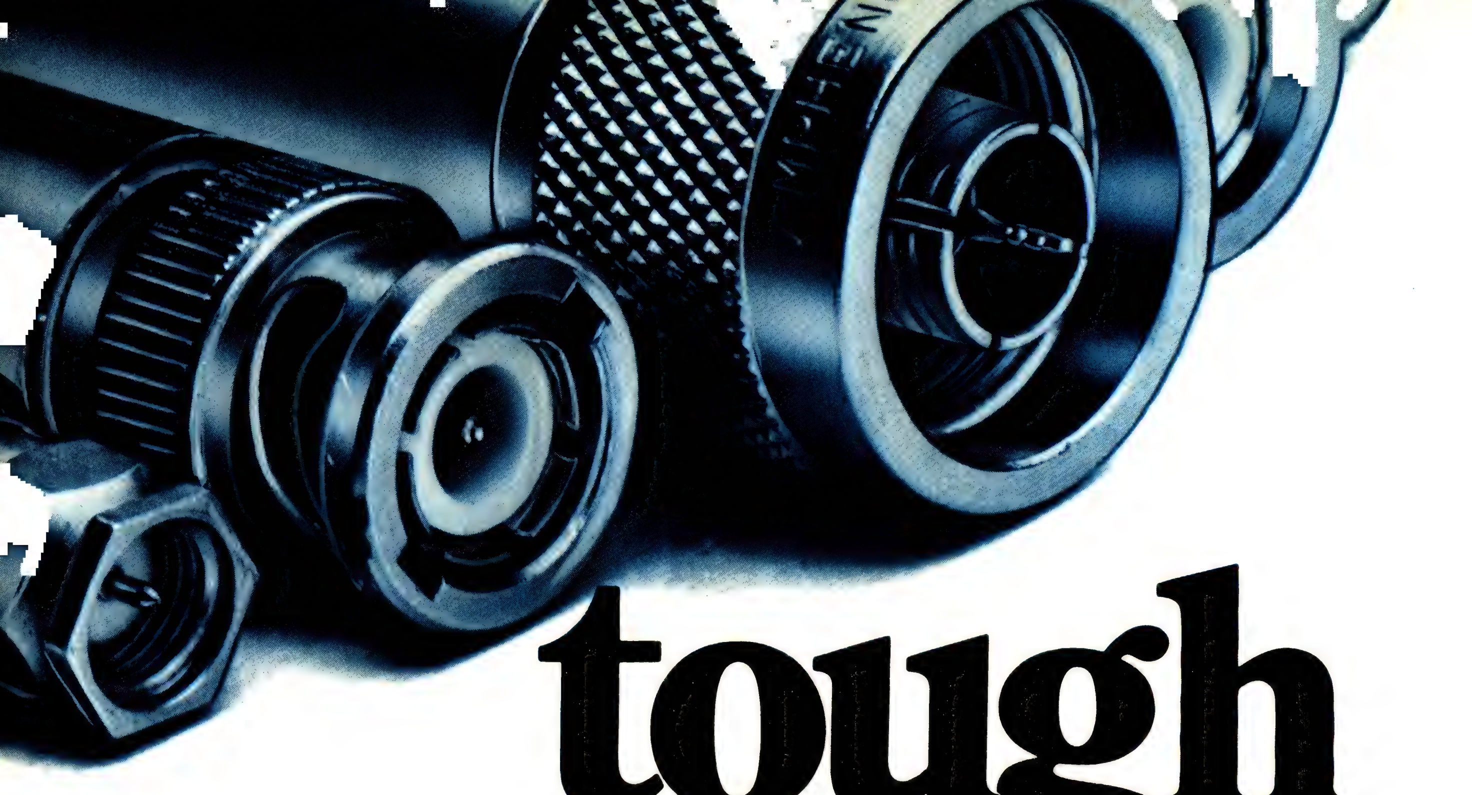

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		DC–1000	1000–1500	DC–1000 MHz	1000–1500 MHz
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1	●	●	●	●
2	●			
3	●	●■	●	●
4	●			
5	●			
6	●	●■	●	●
7	●			
8	●			
9	●			
10	●	●■	●	●
12	●			
15	●			
20	●	●■	●	●
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1000-2000 MHz	25 dB min.
2000-2500 MHz	20 dB min.
SWR	1.5 max. ("on" state)
SWITCHING SPEED	1 μsec. (max.)
MAXIMUM RF INPUT	+20 dBm
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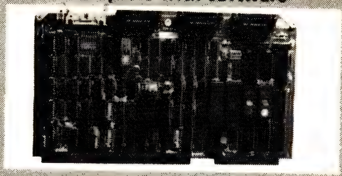

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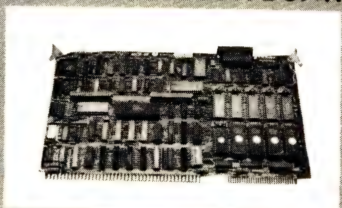
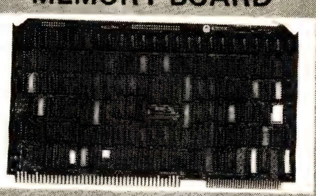


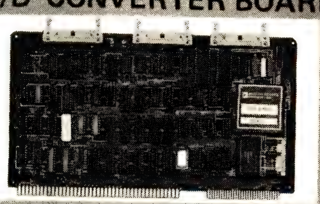
•Special control port for multi-processing applications • 32K to 256K bytes configurable in RAM or EPROM via an addressing PROM • (1) RS-232C asynchronous port • (8) Interrupt levels • (2) iSBX Links
•RAM Supports external battery back-up. Intel 8088 CPU

MEMORY BOARD



•16M bytes addressable • 8/16-bit Data Transfer • Designed around our High Speed Data Acquisition Bus • (3) Access
•(1) MULTIBUS (R) • (2) Ports on Private Bus • Up to 1M bytes of dynamic RAM (auto refresh, parity error check)

A/D CONVERTER BOARD



•8/16-Bit Data • Design around our High Speed Data Acquisition Bus • (32) Analog Inputs (± 10V) • 12-bit resolution, 0.2% precision
•Sampling Frequency controlled by software or external hardware
•High Speed Acquisition Mode via private bus (32 channel burst = 256 us) • Low Speed Acquisition Mode via MULTIBUS (R)

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CIRCLE NO 15

SIGNALS & NOISE

Frustrated with IBM PC modem boards

Dear Editor:

I read your Technology Update article "Consider overall system requirements when choosing modem boards for the IBM PC" (EDN, October 18, pg 77) with much interest, albeit a little frustration. The modem boards described are no doubt very cost effective in the US, but they are not usable throughout the majority of other countries, for three main reasons.

First, they do not modulate to a CCITT international standard (they are all Bell 103 or 212 compatible). Second, in many European countries (eg, West Germany and the Republic of Ireland), it is illegal to connect modems to the PSTN (Public Switched Telephone Network) except those supplied and connected by the local PTT (Post Telegraphe Telephone). Finally, many European countries require equipment which is to be connected to PTT facilities to be type approved. This approval can only be given to complete pieces of equipment; hence, a modem card cannot be type approved, but a PC with a built-in modem can be. Type approval, however, is an expensive and long procedure, and it would not be financially viable to submit all possible configurations of a particular PC for approval.

We Europeans are unable to take advantage of card modems; we must pay for a serial interface and a stand-alone modem. A CCITT V.22 modem (equivalent to the Bell 212) costs around £650 in the UK. Hence my frustration!

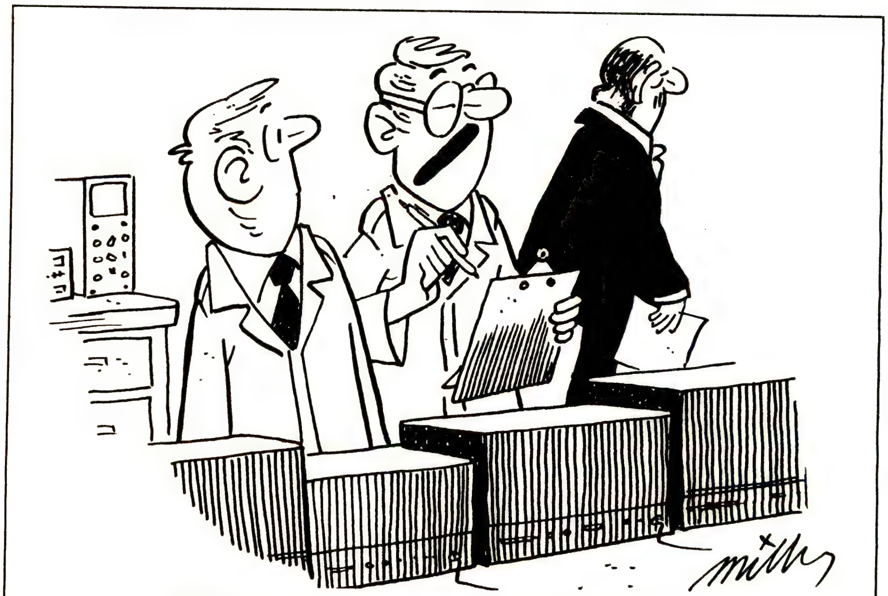
Sincerely,
Steve Kay
Manager, Network and Technical Support
Online Computer Library Center
Birmingham, UK

Inlude another OS in EDN's directory

Dear Editor:

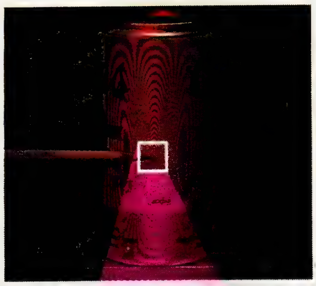
Compiling the Fifth Annual μC Operating Systems Directory (EDN, October 31, pg 114) is an important service that EDN provides to the electronics community. However, we feel that to be complete, the directory should have included the MICRO/OS line of on-chip operating systems for single-chip microcomputers.

MICRO/OS is a real-time multitasking operating system designed specifically for single-chip microcomputers. It offers designers an



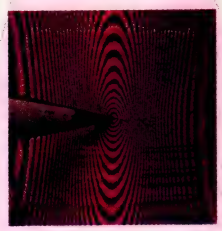
"CRITICAL? FOR HIM, 99 44/100 PERCENT PURE IS CONTAMINATED."

Visualize **Minute Deformations** at the touch of a button



In 10 seconds, you see exactly how a sample deforms or vibrates. You get the total picture of the dimensional changes, down to a fraction of a wavelength of light. This HC-1000 imaging system is fully automated and is as easy to use as a Polaroid® camera.

The crisp lines you see form a topographic map of the deformation when the pop top can is lightly touched. The elevation between successive contour lines is precisely 12.4 microinches.



Contour lines show how the can changes shape as a result of a slight deformation.

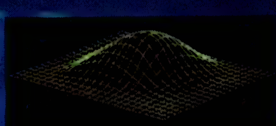
Visualize **Thermal Problems** at the touch of a button

Our HC-1000 camera helps design more sophisticated computer disc drives. The goals are to minimize warping of the housing during warmup, and minimize resonant amplification of the read-heads. Corrective action becomes easy when you can get the total picture and pinpoint the problems.

Other engineers depend on the HC-1000 to study the turn-on/warm-up response of the circuit boards, laser housing, and gyroscopes, and to observe the dimensional temperature sensitivity of radio dish antennas at −120°C.

The figures tugging and pulling on this 5 1/2 inch disk drive have been sketched in to help visualize the nature of the thermal deformations revealed by the holographic fringe pattern.

Visualize **Vibration** at the touch of a button



Holography provides a quick way to watch the entire part vibrate, identify its various resonant frequencies, and determine exact vibration amplitudes at any point on the part. This technique compliments computer modeling to provide engineering data needed to design reliable parts for today's critical needs.

Real-time holography is often used to locate resonant frequencies, while time average holography produces a sharp detailed modal map of the vibrating part. Our HC-1000 can do both, in 10 seconds.

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CIRCLE NO 16

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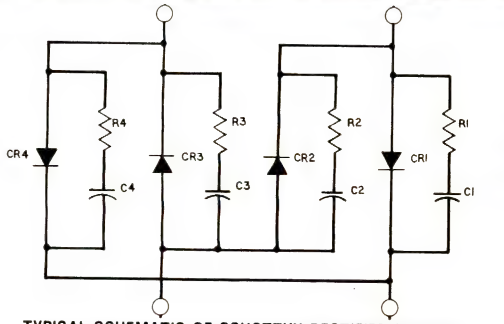
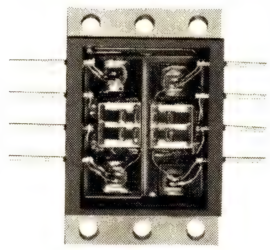


TYPICAL SCHEMATIC OF SCHOTTKY RECTIFIER BRIDGE



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CIRCLE NO 18

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Sincerely,
Ed Thompson
President
Micro Computer Control
Hopewell, NJ

Typos creep in

Dear Editor:

I would like to point out that there are a few typographical errors in the Design Idea "Z80 routine tests RAM at power-on" (EDN, October 18, pg 325). In the section of code labeled "RAM30," the Z80 HL and DE registers should both contain the starting address of RAM. In the section labeled "RAM21," the RAM start address was incorrectly stated. As a side note, for readers who need only a Go/No-Go RAM test for power-up, the code involved in setting and checking bits in register E′ can be omitted, thus bringing the total size of the RAM test to approximately 80 bytes.

Sincerely,
Norman R Bartek
Consultant
Bartek Associates
Park Ridge, IL

(Ed Note: In the section of code labeled "RAM21," the seventh line should read:

```
LD HL,04000 ;RAM START
            ADDRESS
```

In the "RAM30" section of code, the second line should read:

```
LD DE,04001 ;RAM START
            ADDRESS
```

These typographical errors occurred at the editing stage. We apologize for any confusion the errors may have caused.)

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CIRCLE NO 19

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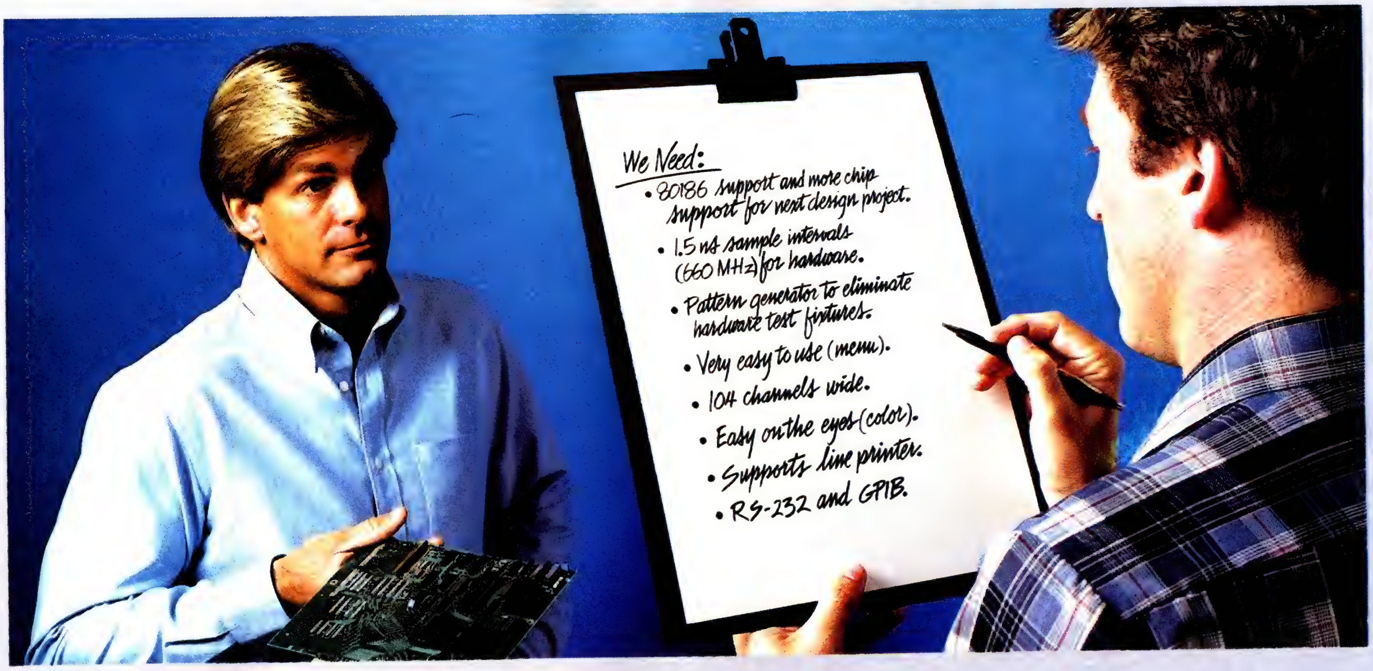
You do.



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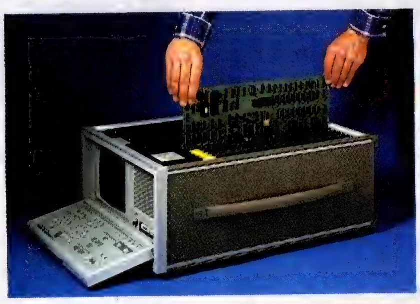

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8039	6802	Z80	1805
8085	6803	Z8001	NSC800
8086	6805	Z8002	F9450
8088	6808	Z8003	1750A
80186	6809	Z8004	UNIBUS
80188	68121	6502	Q-BUS
GPIB	ASCII	EBCDIC	

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CALENDAR

Microcomputers in Control Systems: Hardware, Software, and Interfacing, George Washington University, Washington, DC. Chip Blouin, Continuing Engineering Education, George Washington University, Washington, DC 20052. (202) 676-8527; (800) 424-9773. January 14 to 18.

Measurement Science Conference, Marriott Hotel, Santa Clara, CA. John Schulz, Ford Aerospace and Communications Corp, Box A, Bldg 4, Rm 28, Newport Beach, CA 92660. (714) 720-4787. January 17 and 18.

Robots in Clean Room Applications, San Jose, CA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. January 22 to 23.

Successful Soldering, Anaheim, CA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. January 23 to 24.

Information Services Seminar (ISS), Newport Beach, CA. SEMI, 625 Ellis St, Suite 212, Mountain View, CA 94043. (415) 964-5111. January 27 to 30.

7th Annual Communications Networks Conference & Exposition, Washington Convention Center, Washington, DC. Communications Network '85, Box 880, Framingham, MA 01701. (617) 879-0700; (800) 225-4698. January 28 to 31.

Mecom '85, Bahrain. Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. February 2 to 4.

Automated Manufacturing Conference, Don Ce Sar Hotel, St Petersburg Beach, FL. Frost & Sullivan, 106 Fulton St, New York, NY 10038. (212) 233-1080. February 4 and 5.

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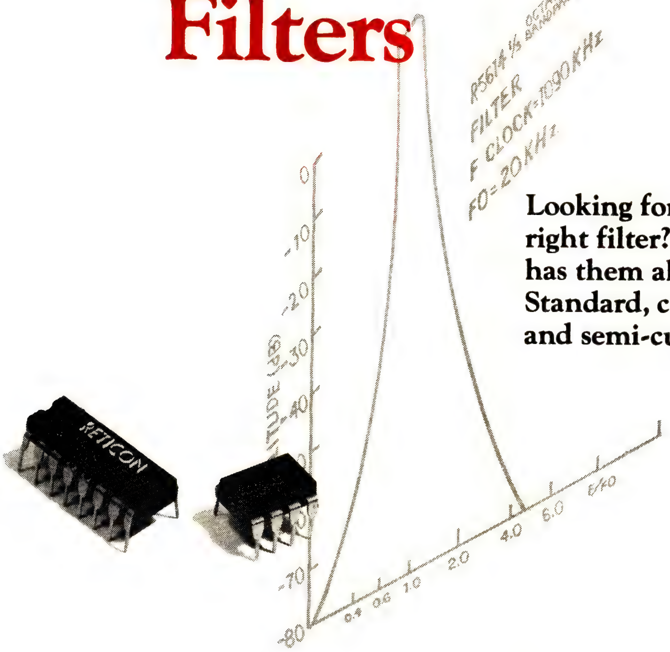

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CIRCLE NO 23

CALENDAR

Power Conversion Products Council International (PCPCI), Doubletree Inn, Scottsdale, AZ. PCPCI, Box 637, Libertyville, IL 60048. (312) 362-3201. February 6 to 8.

Computer Business Graphics, Bonaventure Intercontinental Hotel, Ft Lauderdale, FL. Carol Every, Frost & Sullivan, 106 Fulton St, New York, NY 10038. (212) 233-1080. February 20 to 23.

Information Management Exposition & Conference (Info/Central 85), O'Hare Exposition Center, Chicago, IL. Info/Central, 999 Summer St, Stamford, CT 06905. (203) 964-8287. February 20 to 22.

Info/Software 85, O'Hare Exposition Center, Chicago, IL. Info/Software, 999 Summer St, Stamford, CT 06905. (203) 964-8287. February 20 to 22.

Automated Design and Engineering for Electronics Exposition and Conference (ADEE West '85), Anaheim, CA. CEG, Box 5060, Des Plaines, IL 60018. (312) 299-9311. February 26 to 28.

National Electrical Manufacturers Association (NEMA) Liability Seminar, Hyatt Regency Tampa, Tampa, FL. NEMA, 2101 L St NW, Washington, DC 20037. (202) 457-8400. March 4 to 5.

ISDN '85, Bally's Park Place Hotel, Atlantic City, NJ. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. March 4 to 8.

National Design Engineering Show, McCormick Place, Chicago, IL. CEG, 999 Summer St, Stamford, CT 06905. (203) 964-0000. March 11 to 14.

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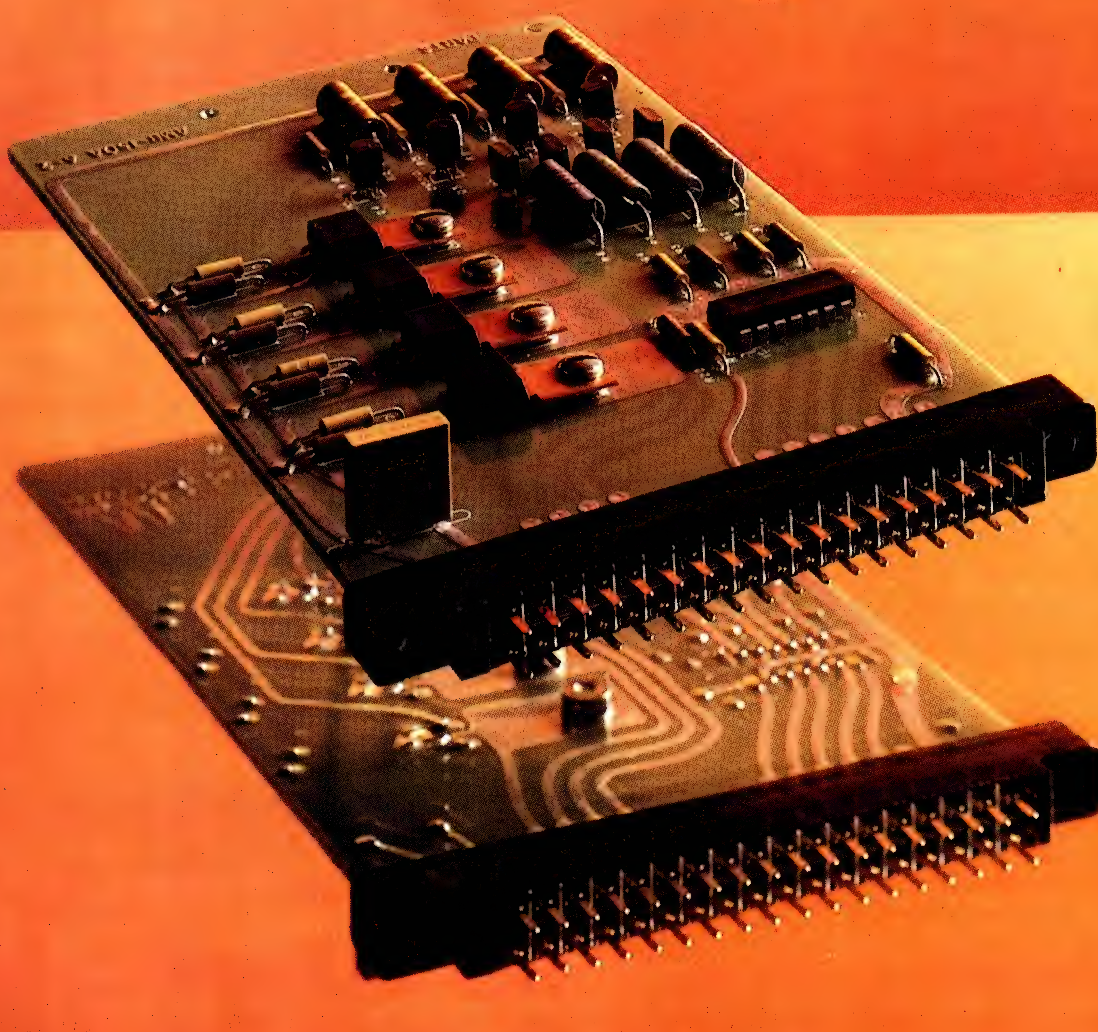

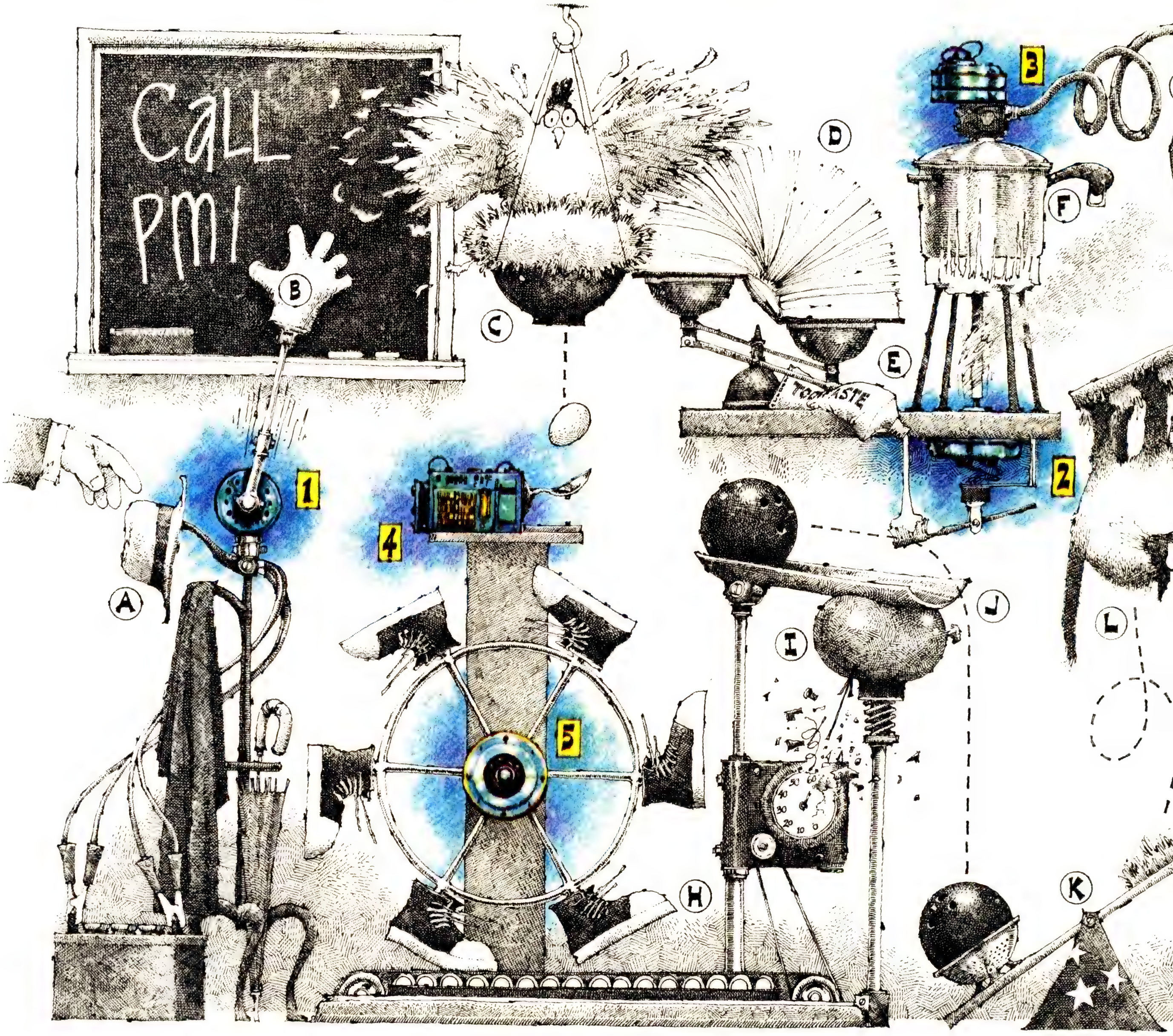

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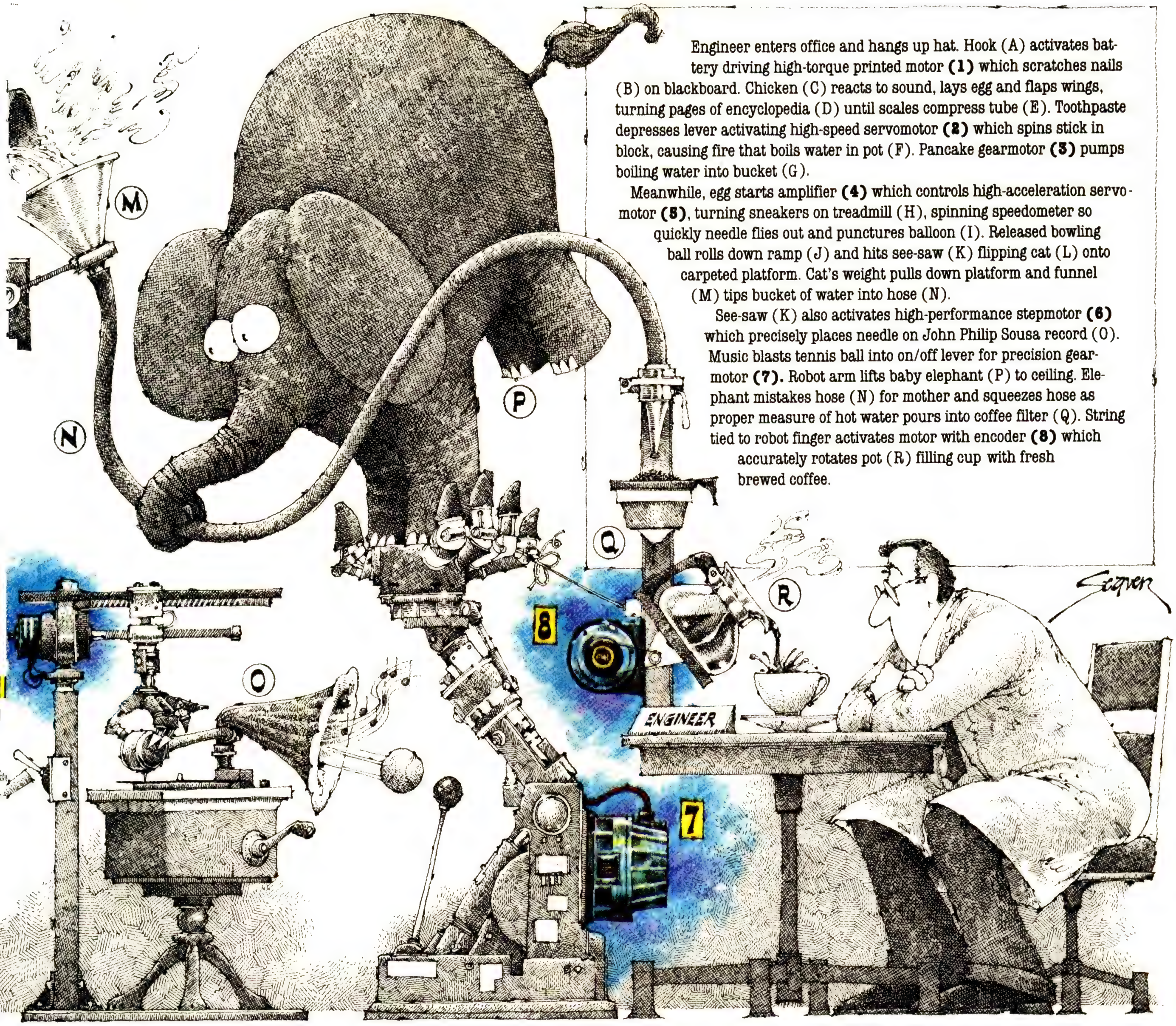

Engineer enters office and hangs up hat. Hook (A) activates battery driving high-torque printed motor **(1)** which scratches nails (B) on blackboard. Chicken (C) reacts to sound, lays egg and flaps wings, turning pages of encyclopedia (D) until scales compress tube (E). Toothpaste depresses lever activating high-speed servomotor **(2)** which spins stick in block, causing fire that boils water in pot (F). Pancake gearmotor **(3)** pumps boiling water into bucket (G).

Meanwhile, egg starts amplifier **(4)** which controls high-acceleration servomotor **(5)**, turning sneakers on treadmill (H), spinning speedometer so quickly needle flies out and punctures balloon (I). Released bowling ball rolls down ramp (J) and hits see-saw (K) flipping cat (L) onto carpeted platform. Cat's weight pulls down platform and funnel (M) tips bucket of water into hose (N).

See-saw (K) also activates high-performance stepmotor **(6)** which precisely places needle on John Philip Sousa record (O). Music blasts tennis ball into on/off lever for precision gearmotor **(7).** Robot arm lifts baby elephant (P) to ceiling. Elephant mistakes hose (N) for mother and squeezes hose as proper measure of hot water pours into coffee filter (Q). String tied to robot finger activates motor with encoder **(8)** which accurately rotates pot (R) filling cup with fresh brewed coffee.

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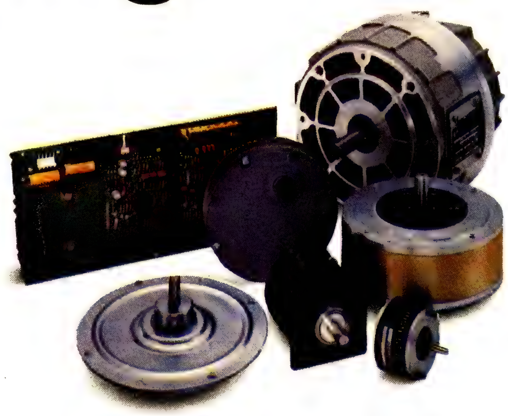

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CIRCLE NO 24

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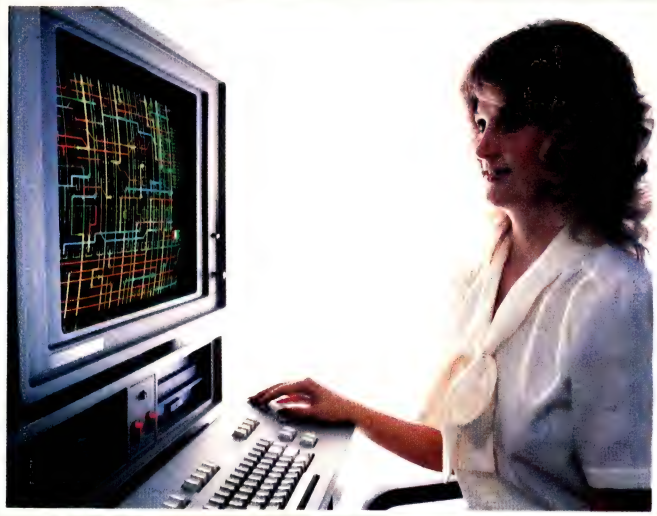

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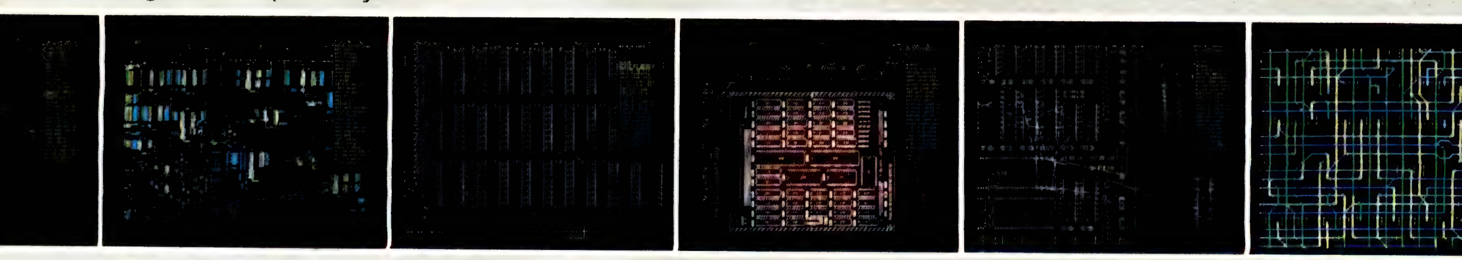

Documentation must be ready, when the product is ready.
Two features of MERLYN-PCB are significant here. Because the system is a continuous process design system, **the schematic of record is maintained.** The system has forward and backward annotation. And it provides the correct and necessary information — data capture — required for a thorough net list generation. When symbols are retrieved from the library, MERLYN-PCB brings forth the schematic symbol and the physical part definition, including electrical properties — thereby eliminating the time consuming task of identifying and specifying each device at the end of the design process.

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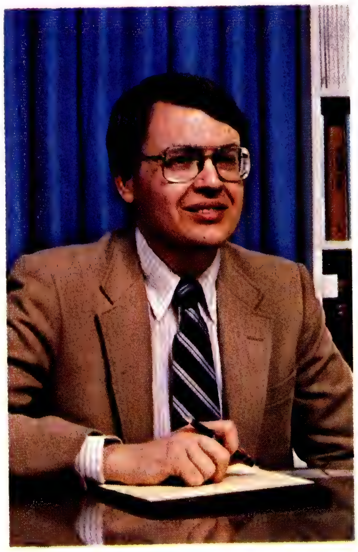
CIRCLE NO 25

Technical obsolescence: a preventable problem



Far too many engineers, during the middle years of what should be long and rewarding careers, work at unchallenging assignments that barely utilize their technical skills. In later years, the tasks they perform are increasingly menial. And although age discrimination sometimes contributes to this unfortunate situation (EDN, December 13, 1984, pg 35), technical obsolescence also plays a major role. All too often, engineers find that the skills they worked so hard to develop are no longer the ones in demand.

But are the engineers themselves solely to blame? As EDN Staff Editor Deborah Asbrand reports in Professional Issues (pg 383), some companies recognize that technical obsolescence is also a corporate responsibility. Realizing that busy engineers have little time for study that isn't directly related to the job at hand, these progressive companies make educational time available, either within the regular work schedule or as sabbaticals, in what amounts to an engineer-maintenance program.

Such programs are commendable for several reasons. The most obvious reason is simply that the programs augment a scarce resource—engineering talent—with benefits both to individual engineers and to companies. But in addition, whether or not companies realize it, some of their best employees are the ones most in need of time for additional technical education. The most dedicated employees are the ones most likely to spend extra time working on their projects—projects using current technology. Thus, they have little time for developing expertise in evolving technologies. By making time available to these workers, companies help ensure that their most dedicated employees remain the most capable.

Avoiding technical obsolescence is a two-way activity, of course; incentives to increase technical skills have little effect on engineers who lack ambition and dedication. Fortunately, though, ambition and dedication are common traits in engineers. The best-managed companies recognize this and invest in programs that encourage personal technical growth. The final result, like the final result of all good investments, is a net positive gain.

Gary Legg

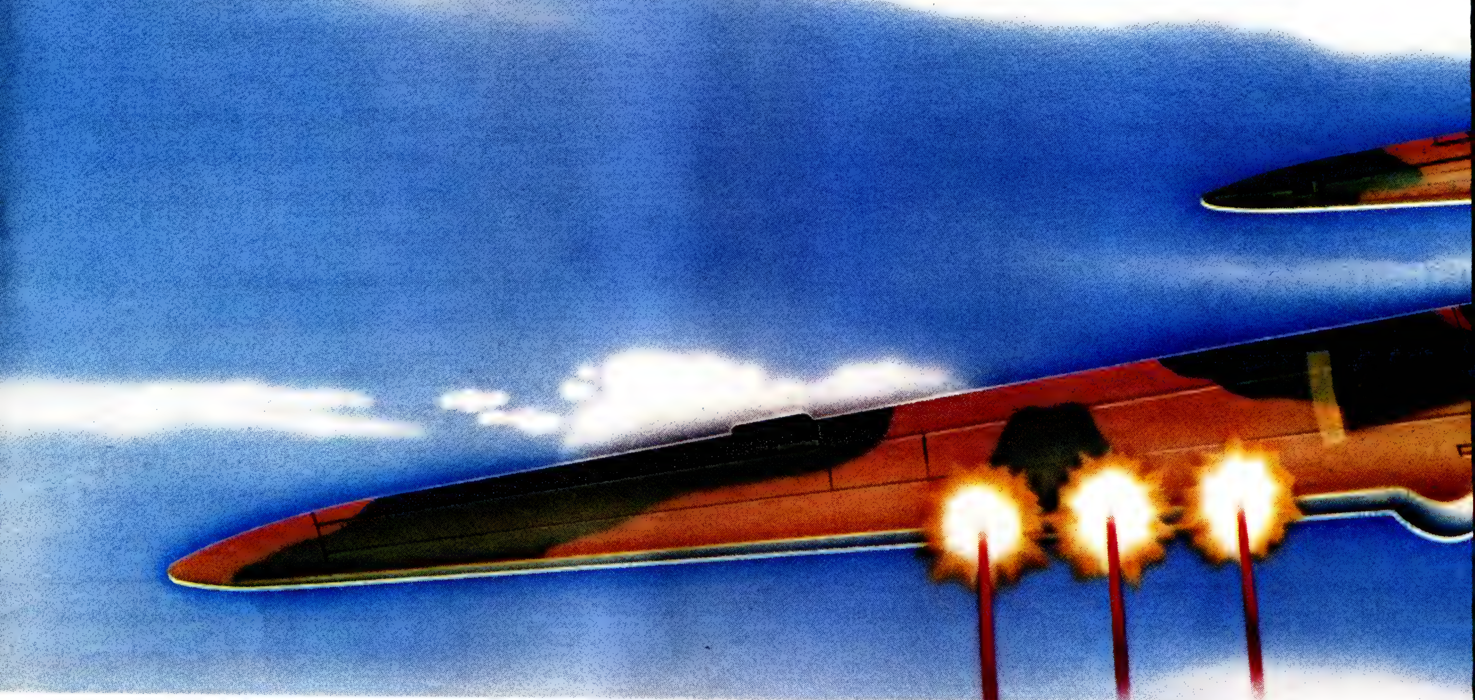
Gary Legg
Editor

Jesse H Neal
Editorial Achievement Awards
1981(2), 1978(2), 1977, 1976, 1975

American Society of
Business Press Editors Award
1983, 1981

1-800-5

Realism for your new entertainment



As an entertainment system designer, you know that today's electronics technology permits the generation of CRT-displayed graphics with all the fidelity of a first-quality color motion picture; but until now, not at a price economically feasible for low- and medium-priced entertainment equipment.

High-quality graphics generators have required a stack of printed circuit boards densely packed with SSI/MSI integrated circuits at a cost well beyond sensible budgets for low-cost microcomputer systems. This has caused the majority of graphics displays for popularly-priced entertainment systems to suffer from limited resolution and color selectivity.

New high-quality graphics at a remarkably low cost.

Entertainment systems can be vastly improved now with design-in support and low-cost technologies from Motorola. For colorful, high-resolution graphics in home video and computer games where realistic computer animation is needed, there's Motorola's cost-effective Raster Memory System (RMS). This available-under-$20 in-production-volume chip set at last makes professional, quality graphics affordable for your next entertainment system.

Using only two chips, the RMS, under MPU control, converts a graphics program stored in memory into the complex video stream that can produce high-quality displays on the CRT. At an astonishingly low cost. No longer is expensive static display RAM needed. The RMS utilizes system memory comprised of industry-standard DRAM with capacities ranging from 16K to 1M bytes.

With the RMS you can select 32 colors from a universe of 4096 shades to use on a virtual accommodating and smooth scrolling screen.

With the advent of the RMS, graphics quality is now primarily dependent on the sophistication of the software, the amount of memory available and the power of the MPU.

A range of MPUs for every entertainment application.

The RMS chip is designed to operate with a wide range of processors including three of Motorola's powerful MPUs: the 8-bit MC6809, the 8/16-bit MC68008 and the 16/32-bit MC68000.

Motorola's MC6809 MPU has the most complete set of addressing modes available on any 8-bit microprocessor today and interfaces with over fifty M6800 peripherals. In addition, you're never locked into a specific design with an upward source-code compatible instruction set.

The MC68008 MPU allows the design of cost-effective systems using 8-bit data buses while providing the system throughput benefits of a 32-bit microprocessor architecture. The performance of the MC68008 is greater than any 8-bit microprocessor and superior even to several 16-bit microprocessors.

The industry-leading MC68000 is a fully-implemented 16-bit microprocessor with 32-bit registers, a rich instruction set and versatile addressing modes.

With this line of compatible processors, you'll satisfy all the price/performance tradeoffs in your design requirements.

Modulators and encoders give the big picture.

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The MC1374 is a TV modulator circuit that packs an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator all on one low cost chip. It is designed to generate a TV signal

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from both audio and video inputs. The MC1374's wide dynamic range and low distortion make it particularly well-suited for applications such as video tape recorders, video disc players, TV games and subscription decoders.

The MC1377 is a color television RGB-to-PAL/NTSC encoder used to generate a composite TV signal from baseband red, blue, green and sync inputs. It is ideal for encoding signals from color cameras and graphics generators.

Opening new markets with AM stereo.

Radio designers are noting the significant advantages AM stereo has over FM in range of coverage and fade resistance.

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In the absence of a good stereo signal, CQUAM® produces an undegraded monaural output for existing radios. When both channels are modulated the noise increase in stereo is a maximum of 3.0 dB . . . even less on program material.

Years of refinement have made Motorola's CQUAM® the leading contender in the race for a "world standard" in AM stereo systems. Even with four FCC approved competitors, Motorola's CQUAM® has captured more than 140 new AM stereo stations this year and leads in production with over nine major manufacturers.

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Motorola has tripled the number of application engineers it has throughout the U.S. and Canada.

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The RMS system can simultaneously display any 32 colors from its palette of 4096 colors in adjacent pixels. The above illustration is a continuous tone artist's representation.

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MOTOROLA

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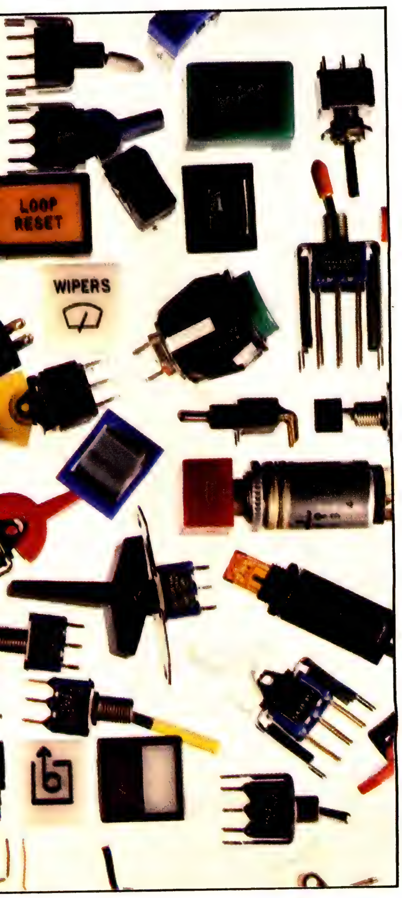

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CIRCLE NO 26

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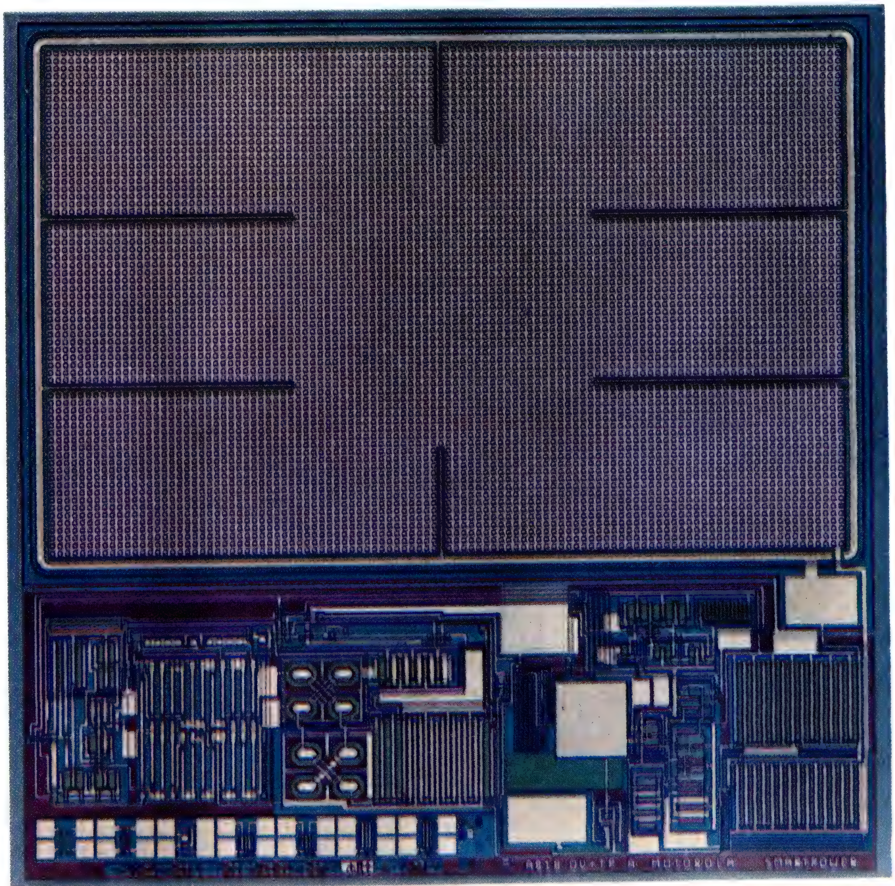
CIRCLE NO 27

Mixed-process, CMOS-driven power ICs come slowly but inexorably to market

Bill Travis, *Senior Editor*

Integrated circuits that combine logic blocks with high-current output devices make eminent sense. The logic can provide such committed functions as overvoltage or overcurrent shutdown, for example, or it can provide a convenient interface between output drivers and a microprocessor. Such ICs, however, demand an almost contradictory mixture of technologies—for example, CMOS and bipolar or CMOS and vertical power-MOSFET processing. A few such mixed-technology products do exist, however, and others are about to emerge.

Fully in step with CMOS's seemingly unstoppable march to ubiquity, the recently introduced circuits that will be discussed in this article use onboard CMOS logic to control the output power devices, but they differ widely in their choices of these output devices' construction and configuration (source or sink, for example). The output-device choices made stem principally from the respective manufacturers' processing experience.



This overvoltage and temperature-protection IC *from Motorola uses CMOS logic and a vertical-MOS output thyristor. Model MPC2005/2006 protects against supply voltages higher than 6.2V and junction temperatures greater than 125°C. The plastic-housed MPC2005 handles 150A surges; the metal-packaged MPC2006 handles 350A peak.*

Power MOS mates with CMOS

As an example of a company profiting from its expertise in specific technologies, consider Motorola Semiconductor's Smartpower II Series. These ICs combine CMOS logic with vertical power-MOSFET (dubbed TMOS) output devices. The Smartpower devices that preceded this latest family mixed CMOS with bipolar devices; the recent ICs make economical use of silicon by taking advantage of the company's TMOS-processing refinements.

Introduced last year, Model MPC2005/2006 overvoltage and temperature-protection circuit **Fig 1a** is a crowbar IC that has a vertical-MOS output thyristor. If it senses a voltage higher than 6.2V (±0.3V) or a junction temperature higher than 125°C, it places a short circuit directly across the line. The MPC2005, packaged in a plastic TO-220AB case, handles 15A continuous, 150A surge (for capacitive discharge). Housed in a TO-204AA metal case, the MPC2006 conducts 35A continuous, 350A surge.

The 6.2V shutdown voltage for these devices is designed to protect 5V logic against surge voltages. For other supply voltages, you can use an external-trip-voltage pin as shown in **Fig 1b.** You configure the R_1-R_2 divider so that the desired trip voltage on the supply line produces 2.4V (±0.2V) on the pin. Note that you can also place a capacitor across R_2 in order to obtain a delayed trip time.

If the IC trips because of a temperature higher than 125°C, you must remove power and allow the system to cool to 75°C before reapplying power. Thanks to the device's CMOS construction, it dissipates a negligible 10 mW before shutdown.

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- ☐ custom supplies on request
- ☐ supplies designed for fast, easy service
- ☐ full-, half-, and quarter-rack size power supplies
- ☐ only one IEEE-488 bus address required per programmer.

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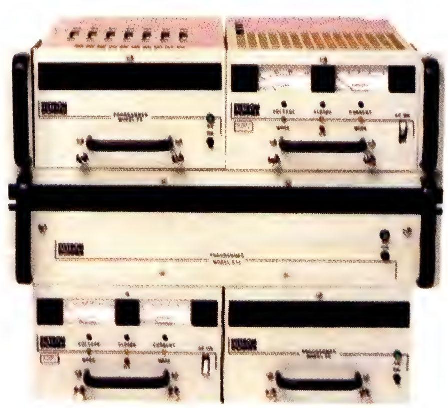

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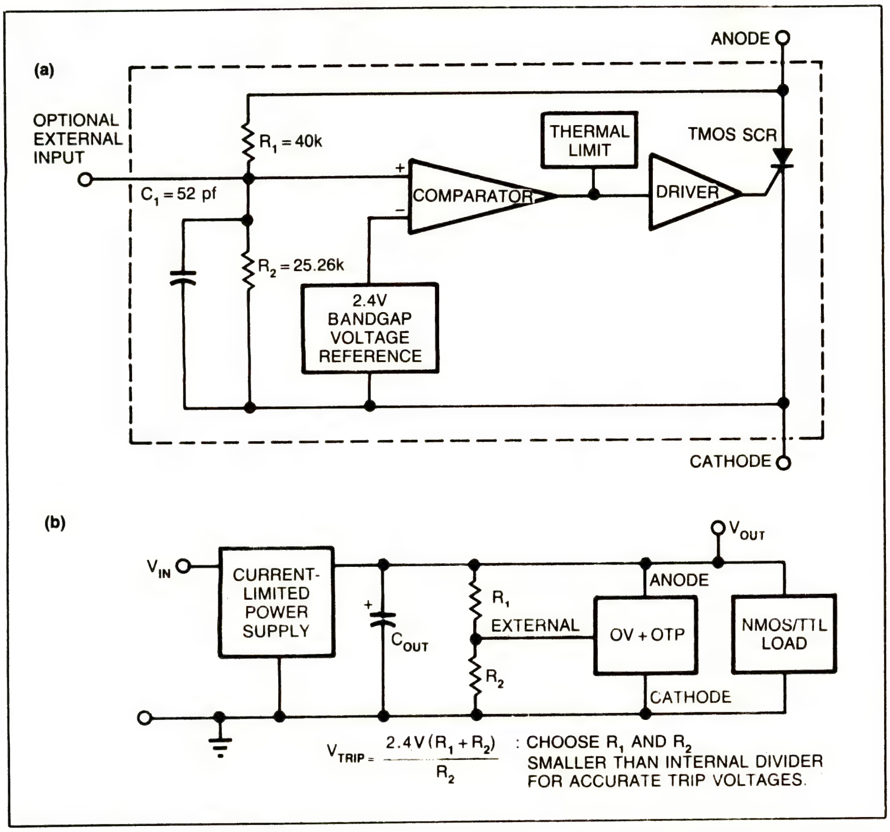
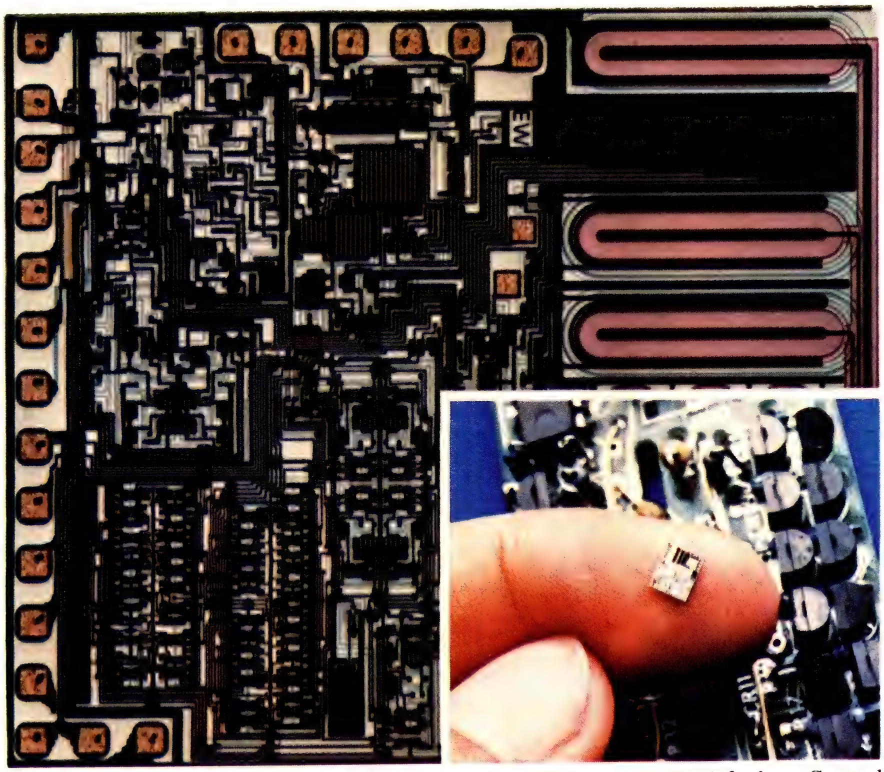


Fig 1—A crowbar IC with a MOS output thyristor, *Motorola's MPC2005/2006 Smartpower circuit* ***(a)*** *protects logic circuitry against excessive supply voltages and junction temperatures. You can change its 6.2V trip point by dividing down the supply voltage* ***(b).***



Combining low-level CMOS logic with high-voltage and -current output devices, *General Electric's process allows any mix of MOS and bipolar devices. The high-voltage output devices can be of bipolar or NMOS construction.*

Therefore, its junction temperature is equal to the ambient temperature. Prices for the MPC2005 family start at \$4.50 (100).

Switch on the high side

The preceding ICs serve as sinks —they *draw* current from the positive rail to ground. There's a great demand, though, for ICs that *source* current; ie, drive grounded loads. And a good deal of this demand originates in Detroit, MI, (see **box,** "The (practically) wireless automobile"), where it's considered highly desirable—if not mandatory—that a load be permanently grounded rather than connected to the positive rail.

The problem with making a current-source output, or high-side switcher, is one of technology limitations and drive. It would be easy to do with pnp-bipolar open-collector or p-channel-MOSFET open-drain stages, but these suffer from disadvantages when compared with their n-polarity counterparts. The pnp bipolar, for example, has much lower h_{FE} than an equal-area npn; the p-channel MOSFET has a much higher $r_{DS(ON)}$ than an equal-silicon n-channel unit.

An elegant solution to the high-side-switcher problem, and one that will probably find use in many future ICs, is to use an open-source, n-channel power MOSFET at the IC's output. This solution, however, brings up the drive problem. To turn an n-channel device on, you must apply a gate voltage that's 5 to 10V higher than the source voltage, which entails a voltage higher than the supply line.

The XPC1500 logic-to-power switch from Motorola uses an open-source, n-channel TMOS output device. To obtain the high gate voltage needed for turn-on, the IC uses a charge-pump circuit—essentially, a voltage multiplier. The source follower operates from a logic-level input and supplies load currents as high as 16A from power supplies ranging from 10 to 28V.

The (practically) wireless automobile

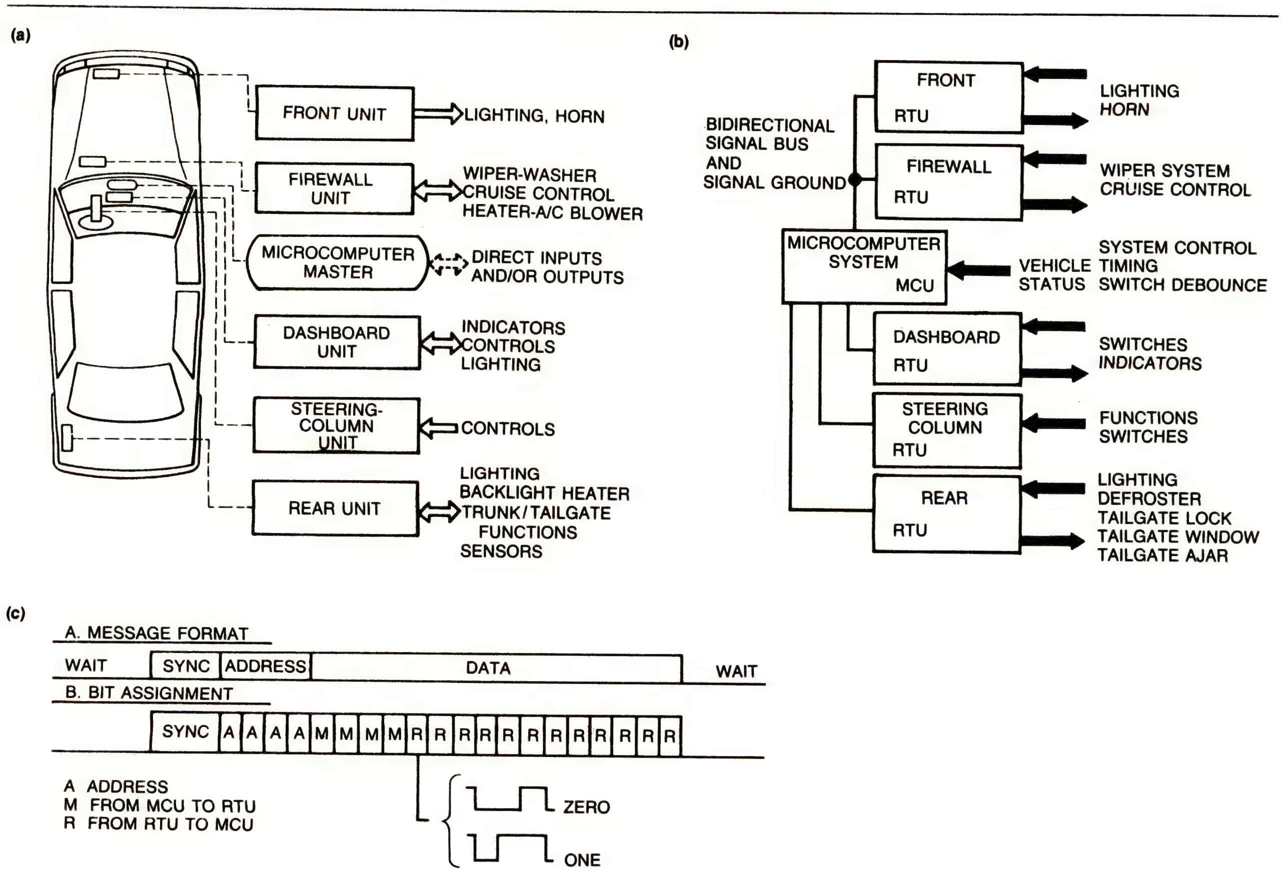
The use of logic-controlled, remote semiconductor switches in automobiles has been a hot topic of discussion for several years. Such a system would have the obvious benefit of eliminating many yards of wire that now exist in cars. But eliminating wire is not the only advantage of an electronic switching system. Perhaps even more important is the possibility of an intelligent interaction between remote locations and the master control unit.

The **figure** shows some details of a possible electronically controlled automobile. The drawing in **(a)** shows the various remote-transceiver units that control functions in the car's various locations. In the case of the rear unit, for example, you can see that one wire from the microcomputer master controls several functions: for example, tail lights, the backlight heater (rear-window defroster), the trunk and tail-gate functions (eg, remote-controlled trunk release), and various sensors.

What differentiates the remote-transceiver-unit scheme from a mere digitally controlled switch is that the RTU could possibly send feedback to the microcomputer master. In **(b)**, note that the rear transceiver unit can inform the master that the tail gate is ajar. In a similar manner, it could sense defective tail lights and other failures. One possible bit assignment for the serial-bit train to and from a transceiver is seen in **(c)**. In this case, four bits serve for the address, four serve for the master's commands to the RTU, and 12 are for the RTU's feedback to the master.

With such compelling advantages of an electronic automotive-control system, why is its adoption taking so long? The answer is simple—high cost, and the need for ICs that combine logic functions and efficient high-current switching devices. The barriers are tumbling, though: When ICs like the ones described in this article are in full production, prices will fall to levels acceptable to Detroit purchasing agents.

The second impediment to the RTU's acceptance is also destined to disappear. Emerging mixed-process ICs incorporate low-loss, high-side-switching outputs. The use of a charge pump with n-channel power MOSFETs, for example, allows turning these devices fully on in a source-follower configuration. Perhaps even more promising, the p-channel modulated-conductivity transistor (RCA's ComFET, Motorola's GEMFET, and GE's IGT) provides the low saturation voltage of a pnp bipolar transistor, and features the low drive requirements of a MOSFET.



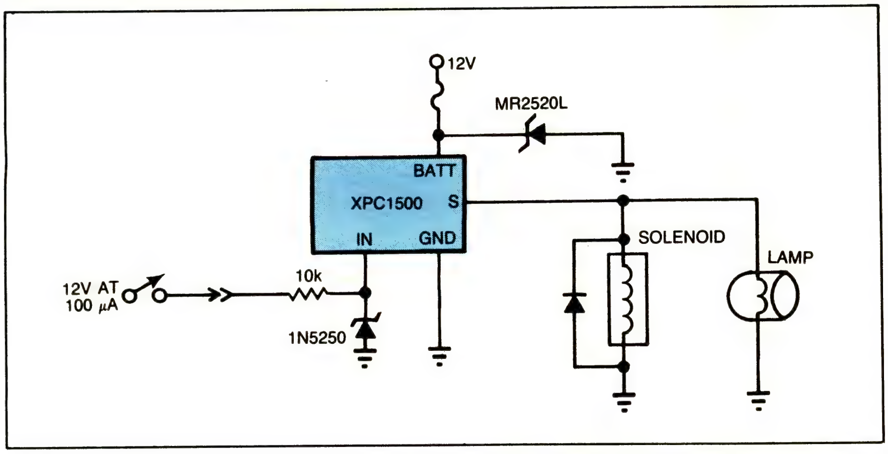


*Fig 2—**Designed for high-side-switching applications,** Model XPC1500 Smartpower IC from Motorola contains a charge pump that supplies a voltage higher than the supply voltage to the TMOS output device's gate. The output device is a source follower that uses the company's TMOS III technology.*

The XPC1500, which should be announced this quarter, can replace an electromechanical relay. **Fig 2** shows a typical application, in which the IC drives a solenoid and an incandescent lamp. Note that in an unprotected system, you must use an overvoltage clamp on the supply bus; you should also protect the IC's input with a zener-diode clamp. One more precaution: The diode clamp across the load protects the device from inductive kickback voltages upon turn-off.

By using serial data encoding, you can use one line to control multiple load switches. **Fig 3** shows a hookup in which a serial bus controls seven loads. An obvious application for this technique is to control remote multiple loads in automobiles.

According to Gary Fay, manager of advanced development, the switch uses 5-μm processing; the power-output MOSFET uses the same technology as the company's recently announced TMOS III power MOSFETs. Motorola's first Smartpower circuits used CMOS logic and bipolar output devices. Some examples are the firm's MPC100/102/104 3-terminal regulators—these are 10A, 80W devices that provide regulated outputs of 5, 12, and 15V, respectively. The internal mixed CMOS and bipolar circuitry provides thermal and short-circuit protection.

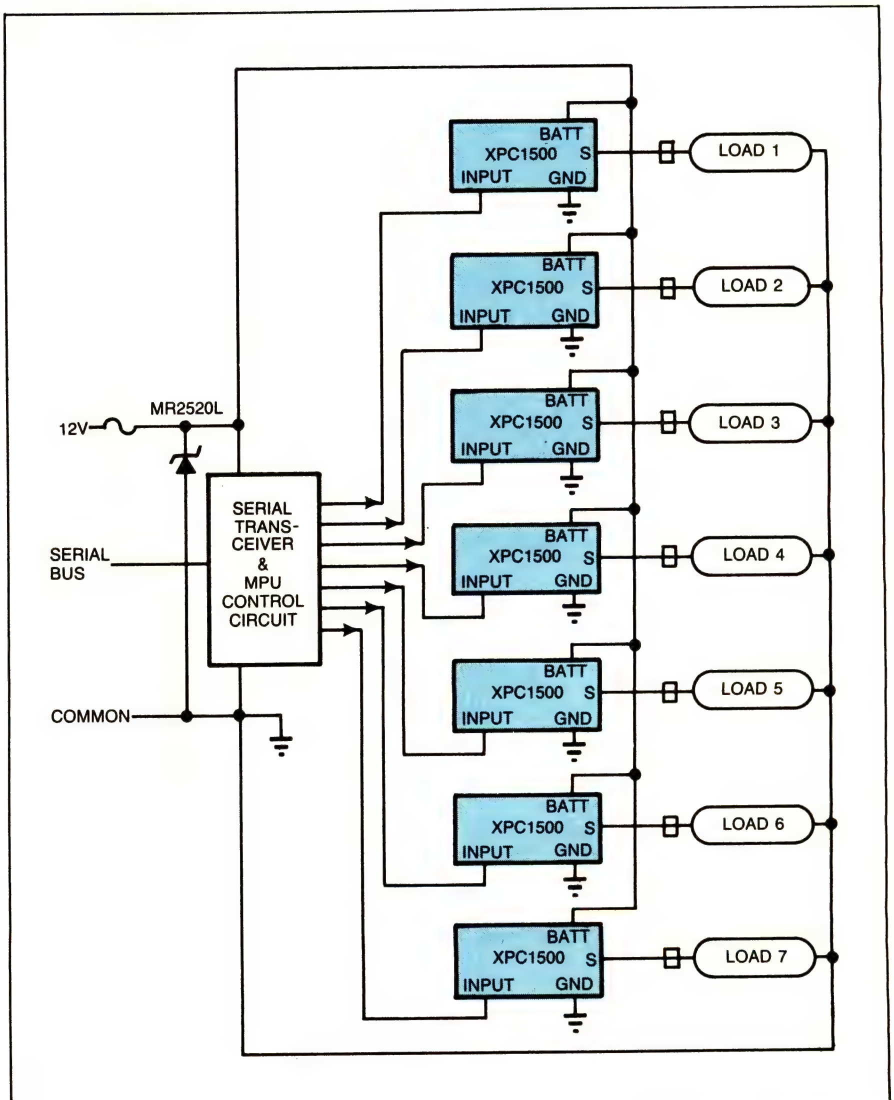
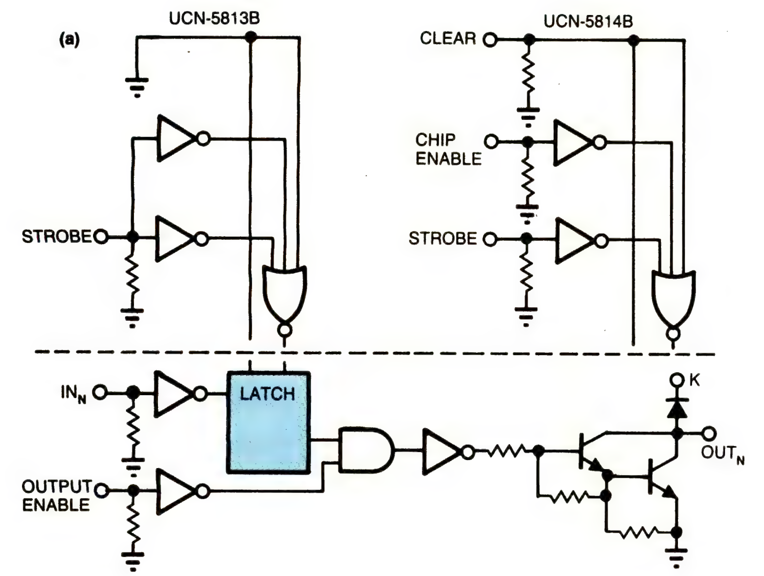


*Fig 3—**This multiple high-side-switching system** uses Motorola's XPC1500 Smartpower ICs. The method uses serial data encoding and a microprocessor control unit to control seven independent loads. A typical application is in automobiles—the loads could be, for example, rear lights and tail-gate functions.*

In mixing CMOS and bipolar processing, a company can go one of two ways, depending on its expertise: It can develop a bipolar process that fits with its existing CMOS technology, or vice versa. According to Mark Heisig, Sprague Electric Co's interface-product applications-engineering manager, his company chose the vice versa—it developed a metal-gate CMOS process that complements the firm's established bipolar technology.

Two recent concrete results of the CMOS/bipolar marriage are the UCN-5813 and UCN-5825 families.



(b)

OUTPUT ENABLE	CLEAR	CHIP ENABLE	STROBE	DATA IN	OUTPUT	NOTES
UCN-5813B						
1			X	X	0	A
0			X	X	n−1	A
0			0	X	n−1	A
0			X	X	0	B
0			1	0	0	B
0			1	1	1	C
UCN-5814B						
1	X	X	X	X	0	A
0	0	0	X	X	n−1	A
0	0	X	0	X	n−1	A
0	1	X	X	X	0	B
0	0	1	1	0	0	B
0	0	1	1	1	1	C

A—DOES NOT AFFECT THE LATCH STATE.
B—RESETS LATCH STATE TO 0.
C—SETS LATCH STATE TO 1.
X—IRRELEVANT.
n−1—IS PREVIOUS OUTPUT STATE.

Fig 4—Using CMOS logic and npn Darlington outputs, *Models UCN-5813B and -5814B from Sprague Electric Co **(a)** handle loads as heavy as 480W. The quad outputs switch currents as high as 1.5A. The truth table in **(b)** shows the logic differences between the two models. Note that all outputs have uncommitted diodes that you can connect for inductive-kickback protection.*

The first family comprises two similar parts: the UCN-5813B and -5814B 4-bit BiMOS quad latch/drivers. (BiMOS is the company's name for the mixed process.) The block diagram in **Fig 4a** shows the difference between the two parts: They're identical except for the fact that the -5814B contains additional clear and chip-enable lines. **Fig 4b** gives the logical truth table for these two parts.

The UCN-5813 is a low-side (sinking) switch. The bipolar output specs 50V sustaining voltage and sinks currents as high as 1.5A; uncommitted diodes allow protecting the outputs against inductive kickback. The -5813B and -5814B come in 16- and 22-pin DIPs, respectively, and handle loads as heavy as 480W. The CMOS inputs are compatible with CMOS, PMOS, and NMOS logic families; TTL and DTL drivers could require a pull-up resistor to ensure a proper logic-one level.

The packages for the -5813B and -5814B have 300- and 400-mil pin centers, respectively, and they both offer a heat-sink tab for thermal transfer. The packages can dissipate 2.2W max at 25°C, to derate by 22.2 mW/°C above 25°C. The circuits operate over −20 to +85°C.

Using the output's 1.25V max saturation-voltage spec, you can easily calculate maximum currents and duty cycles in your application. Applications for the UCN-5813B/5814B include stepper-motor drivers, hammer drivers in impact printers, and incandescent-light drivers.

Similar to the -5813B parts but accepting a serial data input, Models UCN-5825B and -5826B (**Fig 5**) latch/drivers also have four bipolar

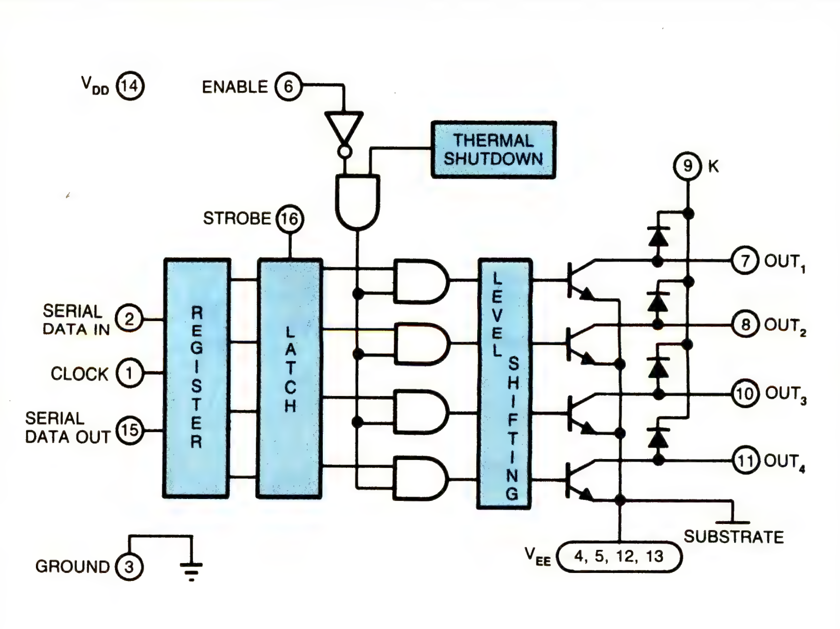


Fig 5—This CMOS/bipolar combination *from Sprague Electric Co is similar to the circuits in Fig 4, but it accepts serial input data. Models UCN-5825B and -5826B handle output currents as high as 2A; they sustain 35 and 60V, respectively. The ICs contain thermal-shutdown circuitry.*

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You Get The Facts: Raytheon has data sheets on each product including theory of operation and a complete application note on a dual tracking power supply using the **RC4391** and **RC4193**.

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Semiconductor Division
350 Ellis Street
Mountain View, CA 94043
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RAYTHEON
Semiconductor Division

CIRCLE NO 29

outputs. The input circuit is a 4-bit CMOS shift register, followed by a 4-bit data latch. The two parts differ only in sustaining voltage: The first sustains 35V; the second, 60V.

The UCN-5825B/5826B contains thermal-shutdown circuitry and output-clamping diodes (for inductive applications). The thermal-shutdown circuit disables all output transistors when an over-temperature condition exists. You must then reset the device by using the enable pin.

Each output handles currents as high as 2A. The UCN-5825B/5826B comes in a 16-pin DIP with heat-sink tabs. Its thermal characteristics are the same as the previously described UCN-5813B/5814B. The IC's logic inputs are compatible with CMOS, NMOS, and PMOS; again, with TTL drive you might need pull-up resistors to obtain a correct logic-one level.

What's coming

Mixed-technology, high-current ICs are in their infancy now. The relatively few products described here represent only the manufacturers' early efforts. In the future, you can expect ICs—from the manufacturers mentioned here and many others—with enhanced current and voltage capabilities and more complex logic circuitry.

Using the BiMOS-II process, for example, Sprague Electric predicts its ICs will attain current capabilities approaching 4A and output breakdown voltages of 150V, possibly 200V. What's more, the company's bipolar expertise allows it to develop respectable-beta pnp output stages for high-side switching—an important consideration for applications in Detroit.

You can expect Motorola, too, to continue to refine its Smartpower ICs. And this company's emphasis will be on its TMOS III power-MOSFET technology, a process that yields power devices with extremely low $r_{DS(ON)}$. Note that the company has another ace up its sleeve—the GEMFET process, a technology that yields power devices with the low saturation voltages of bipolars and the low drive requirements of MOSFETs. Although nothing concrete is in the works right now, it's reasonable to assume that these power devices will find their way onto chips with on-board logic.

Future participants

The few products described here represent two manufacturers' early efforts in mixed-technology, high-current devices. Other semiconductor makers, too, are developing power devices based on widely disparate processes. Although their efforts haven't yet resulted in concrete, publicly offered products, you can expect announcements of such ICs during this year and next.

Consider, for example, General Electric Co's high-voltage, high-current process that uses junction isolation. The process combines bipolar and MOS devices. According to the company, the flexibility of the process allows designers to configure circuits that contain any mix of unlatchable CMOS, NMOS, PMOS, TTL, RTL, and ECL logic, as well as npn and pnp bipolar transistors.

The devices' output drivers can deliver currents as high as 2A peak. In addition to this high-current capability, the process permits the fabrication of high-voltage npn bipolar transistors and NMOS devices. The bipolar, for example, specs a square safe operating area bounded by 500V and 100 mA; the MOSFET has a 500V breakdown voltage and conducts 100 mA.

In terms of concrete products, GE is developing (for a proprietary application) a circuit embodying the described features. The company plans to announce availability of the IC as a standard product in the first quarter of this year.

Power-DMOS outputs

Opting for DMOS (diffused, or lateral MOS) power outputs, as opposed to the vertical MOS structure used in the Motorola circuits, SGS Semiconductor Corp is also developing a capability for mixed-technology power ICs. The planned circuits will combine bipolar, CMOS, and power-DMOS devices. You can expect the announcement of an IC containing bipolar linear circuits and DMOS power outputs in the first half of this year; more ambitious circuits mixing all three technologies will appear shortly thereafter.

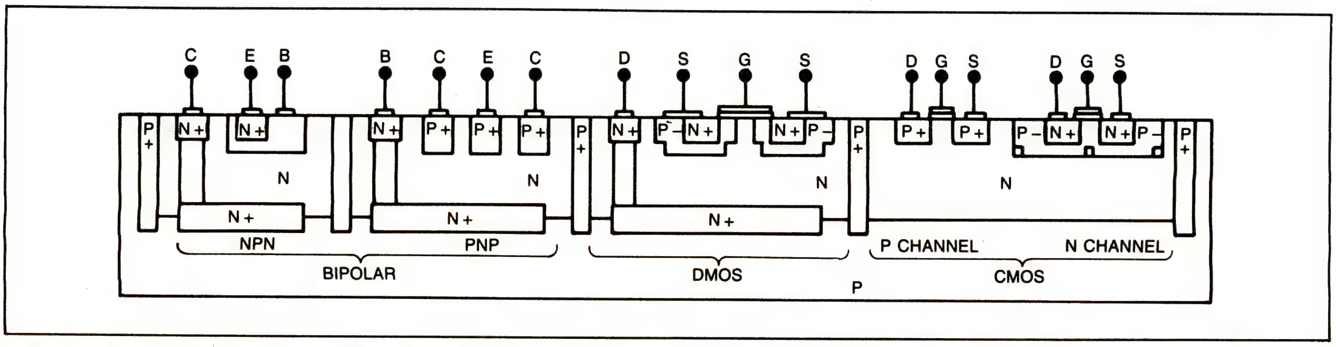
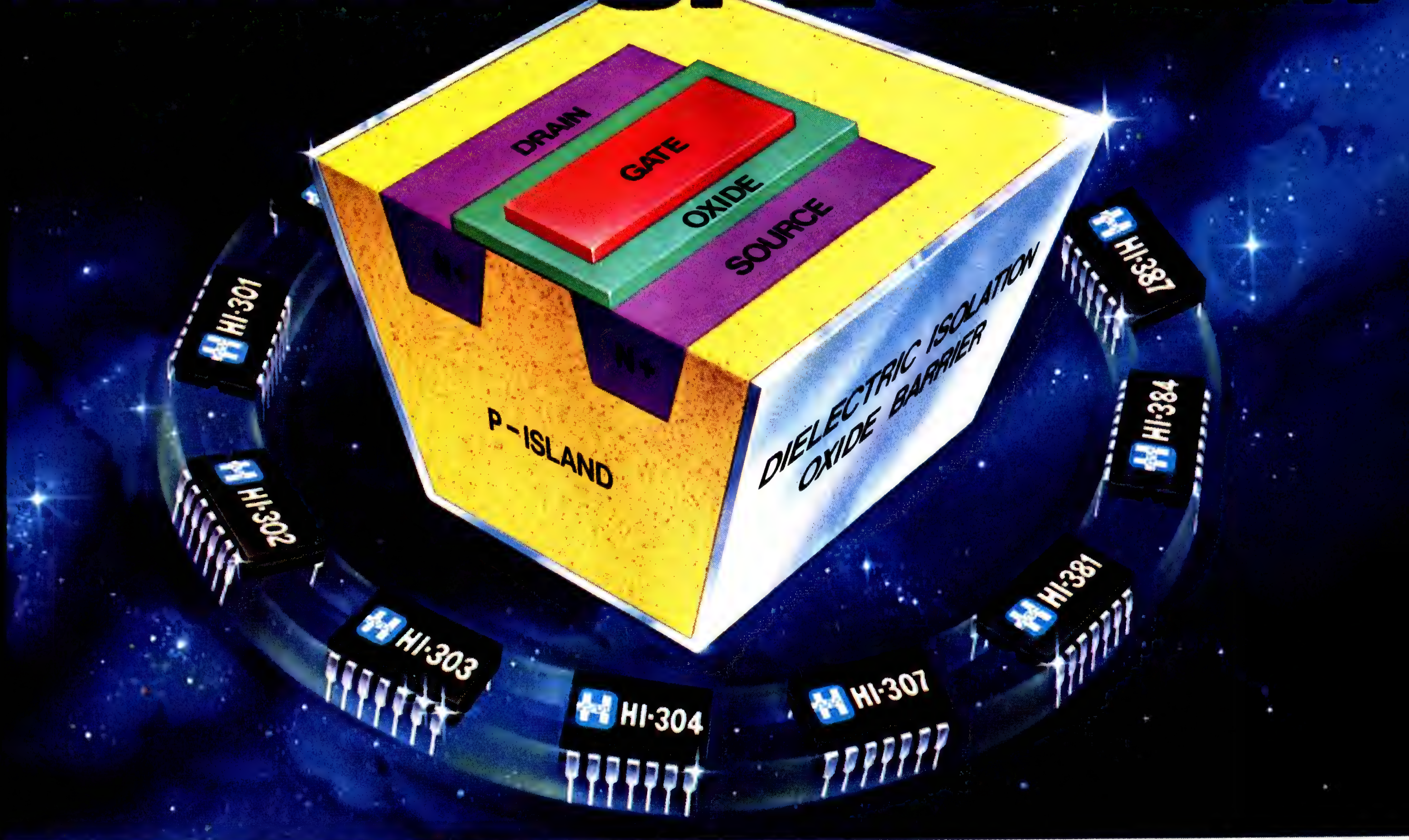


Fig 6—Combining bipolar, CMOS, and DMOS devices, *upcoming power ICs from SGS Semiconductor will handle load power as great as 500W and output currents as high as 10A. Three planned generations in the ICs' evolution will spec drain-source breakdowns of 60, 250, and 450V. The last two versions will operate directly from US and European line voltages, respectively.*

HARRIS SPECTRUM



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Harris 30X/38X Product Summary

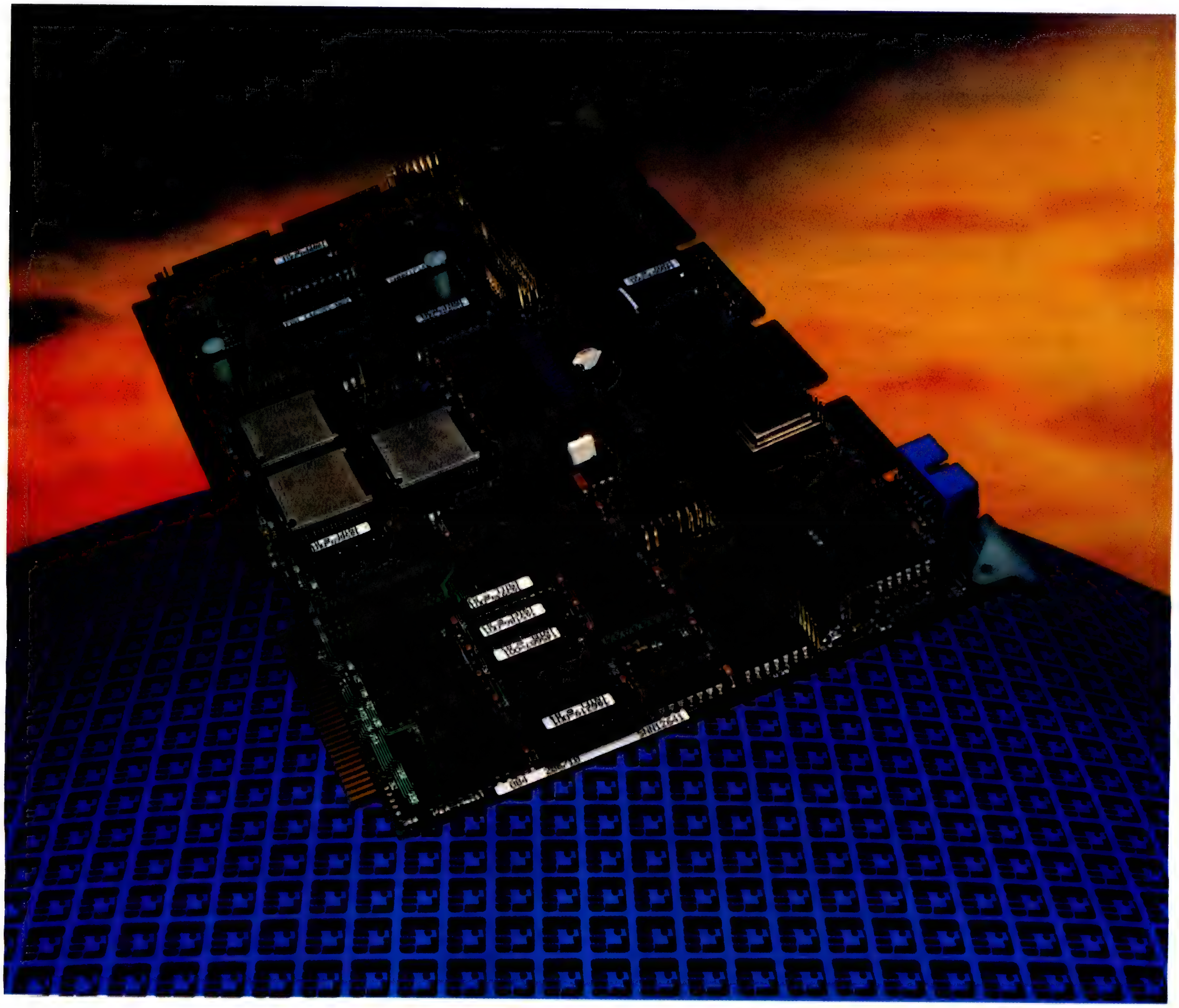
FUNCTION	DEVICE	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$(NA) (TYP)	$t_{(ON)}$(NS) (TYP)	$t_{(OFF)}$(NS) (TYP)	P_D(mW) (TYP)
2 x SPST	HI-300	35	0.04	210	160	1
	HI-304	35	0.04	210	160	0.3
	HI-381	35	0.04	210	160	1
SPDT	HI-301	35	0.04	210	160	1
	HI-305	35	0.04	210	160	0.3
	HI-387	35	0.04	210	160	1
2 x SPDT	HI-303	35	0.04	210	160	1
	HI-307	35	0.04	210	160	0.3
	HI-390	35	0.04	210	160	1
2 x DPST	HI-302	35	0.04	210	160	1
	HI-306	35	0.04	210	160	0.3
	HI-384	35	0.04	210	160	1

Harris Semiconductor: Analog · Bipolar Digital
CMOS Digital · Gallium Arsenide · Semicustom · Custom

HARRIS

For your information, our name is Harris.

CIRCLE NO 30



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CIRCLE NO 31

Fig 6 shows the construction details of the projected SGS ICs. While predicted performance is somewhat sketchy, the company divulges that in high-frequency switching applications, the circuits will deliver output power as high as 200W; currents will be as high 10A. In applications requiring dc drive, these figures become 500W and 10A, respectively. The DMOS output devices' $r_{DS(ON)}$ is 0.15Ω.

The first-generation mixed-process devices (dubbed MD²MOS by the manufacturer) will use the company's DMOS 1 output MOSFETs; these transistors spec 60V drain-source breakdown. Future generations will incorporate DMOS 2 and 3 devices and will withstand 250 and 450V, respectively. These voltage levels are needed, for example, for US and European off-line converters, respectively.

Applications for the MD²MOS circuits include dc/dc converters, audio switching amplifiers, dc-motor control, and generally driving inductive loads (the outputs incorporate intrinsic freewheeling diodes that clamp inductive-kickback voltages).

For automobile applications—the promising area for ICs that combine CMOS logic with high-side-switching outputs—two companies, Siemens Corp and RCA Solid State Div, are devoting large efforts to the development of such circuits.

Although specific details about Siemens' first planned offering (dubbed SmartFET) are not available, the company reveals that you can expect an initial product announcement in the middle of this year, with full production starting next year. As with many of the ICs discussed here, the Siemens part was developed for a specific (automotive) customer.

Meanwhile, RCA is looking toward Detroit, too—but on a very long-term basis. According to Ralph Hartz, in charge of automotive-market development, the company's ICs combining advanced CMOS (called QMOS) and power devices will make their Detroit debut in 1988 and 1989. Hartz predicts that the automotive traditional-wiring/intelligent-bus cost crossover point will occur around 1989.

It's not clear exactly what output devices RCA will opt for. The company has three choices: power MOS-

For more information . . .

For more information on the integrated power ICs described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

General Electric Co
80 Wolf Rd, Suite 500
Albany, NY 12205
(518) 454-2533
Circle No 732

Integrated Power Semiconductor Ltd
2727 Welsh Ave, Suite 201
Santa Clara, CA 95051
(408) 727-2772
Circle No 733

Motorola Semiconductor Products Inc
Box 20912
Phoenix, AZ 85036
(602) 244-4911
Circle No 734

RCA Solid State Div
Route 202
Somerville, NJ 08876
(201) 685-6228
Circle No 735

SGS Semiconductor Corp
1000 East Bell Rd
Phoenix, AZ 85022
(602) 867-6100
Circle No 736

Siemens Corp
Colorado Components Div
800 Hoyt St
Broomfield, CO 80020
(303) 469-2161
Circle No 737

Siliconix Inc
2201 Laurelwood Rd
Santa Clara, CA 95054
(408) 988-8000
Circle No 738

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115 Northeast Cutoff
Worcester, MA 01606
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CIRCLE NO 32

FETs, bipolar transistors, or p-channel ComFETs, which are modulated-conductivity devices. The first, of course, would need some sort of charge-pump circuitry to raise the gate voltage above the 12V supply.

The ComFET seems to make sense. The company claims to have mastered the process to make a p-channel device that has similar characteristics to its n-channel ComFET, with no onerous costs in additional silicon. The p-channel ComFET makes an ideal high-side switch; its output characteristics resemble those of a pnp power transistor.

Hartz reveals that RCA's initial target is to make load-driver ICs with a complexity of 500 to 600 gates. The output devices will handle 3 to 6A, and will withstand an automobile's 60 to 70V load-dump transients. These first ICs will switch upon address recognition; future plans are for devices that also reflect fault information to the CPU.

Semicustom mixed-bag ICs

The circuits described so far were developed on a full-custom basis, either for the merchant market or for specific customers. But these fully committed designs entail long development times. Siliconix, however, has opted for a standard-cell, semicustom approach for its mixed-process power ICs.

According to vice president Art Fury, the use of standard cells allows designers to develop prototype power ICs in a very short time. The cells available now include CMOS logic and analog blocks, and high-voltage and -current DMOS output devices. The company has four additional device types in development, which include

- A bilateral-switch circuit for switching high-voltage ac signals
- A depletion-mode (normally on) circuit for high-voltage current regulators and telecomm switching
- A modulated-conductivity device combining high input impedance and low on resistance
- A synchronous rectifier for emerging 3V power converters.

Fury says that Siliconix will announce two standard power ICs later this year. One combines CMOS logic and analog circuitry with two 100V power devices: one supplying 6A, the other 12A. The second IC marries a CMOS gate array with eight 200V, 200-mA DMOS output transistors.

Because Siliconix's power ICs are capable of managing high voltages as well as heavy currents, the company estimates the circuits will find wide application in the electrical-products industry. The firm's 60-pg compendium of integrated-power technology combines a discussion of Siliconix's approach with a collection of technical-journal reprints that treat high-power ICs in a general way.

Hands across the sea

Perhaps the best indicator of confidence in a new technology is the formation of a company devoting its efforts wholly to that technology. Consider, for example, Integrated Power Semiconductors. The Scotland-based company's long-term plans are to develop ICs combining CMOS circuitry and bipolar power outputs.

Just as do many start-up companies, IPS intends to establish itself by offering as its first products improved versions of several industry-standard power ICs, including motor-control and power-driver circuits. These first efforts will use bipolar technology; low-level CMOS circuitry will come later. EDN

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Finalization of your logic schematic involves simulation, testability analysis, test-pattern generation, and test-pattern grading. This can be done by TI or by you, using your in-house design tools or the computers at your nearest TI Regional Technology Center.

Chip layout can also be done by you using TI-provided specifications or by TI.

Following layout, TI performs a post-routing simulation which ensures that your performance specification is met. A schematic verification determines that your functional specification is met. And a design-rule verification makes sure that all geometric design rules are met.

The final simulation becomes, upon your approval, the benchmark by which all prototype units are tested.

The prototypes are shipped to you for in-system evaluation. At your go-ahead, we produce and deliver, typically within 8 to 12 weeks.

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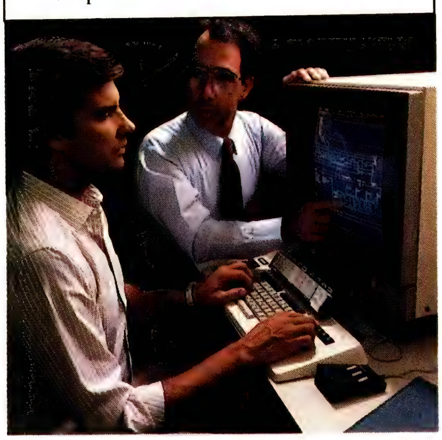

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CIRCLE NO 136

Design centers expand your CAE experience while implementing your ICs in silicon

David Smith, *Associate Editor*

If you're considering semicustom-IC design, don't hesitate to solicit the aid of a design center. Although committing a critical piece of your design to an outside service might seem inimical to controlling the myriad intricacies of the project, you needn't view the semicustom-IC design center as a looming foreign presence. Instead, consider it as a newly hired semicustom expert on your own staff. Not only can it design customized ICs quickly and accurately (and transmit the fabrication and testing data to the manufacturer), it can also give your design group considerable exposure to computer-aided engineering (CAE) and to the IC-design and -fabrication processes.

Like any other staff member, the design center—whether an independent one or one operated by a silicon foundry or a distributor—is subject to your judgment, perceptions, and decisions at every critical design stage. You can maintain a great deal of control of your project—as much as if you were to choose a pc-board implementation. Furthermore, in the role of CAE expert, the design center can train you in workstation operation, logic and timing simulation, IC design, and fault and testability analysis.

On occasion, however, budget or schedule constraints may dictate that you hand off the project to a design center entirely. In this case, your participation in the design of your IC could be limited to a few reviews and to picking up your tested prototypes. This approach allows your firm's valuable manpower to address the remainder of the system design because the design center can guarantee that the ICs' performance will match the simulation results that you review and accept. Also, with this approach, the actual IC design is in the hands of the center's experienced engineers, who are familiar with both the IC-design systems and the practices that result in efficient, testable chips.

POWER CALCULATIONS FORM

CUSTOMER INFORMATION

COMPANY NAME: ______

ENGINEER'S NAME: ______

CIRCUIT NAME: ______

CIRCUIT DATA

ARRAY SERIES MILLIWATTS/GATE (P): (CHECK ONE) — P = ______ .025 (3000 SERIES) / ______ .020 (5000 SERIES) / ______ .018 (7000 SERIES)

OPERATING FREQUENCY (F) (IN MEGAHERTZ) — F = ______ MHz

AMBIENT OPERATING TEMPERATURE (T_a) (IN DEGREES CENTIGRADE) — T_a = ______ C

NUMBER OF GATES (G): — G = ______

NUMBER OF OUTPUTS (B): — B = ______

OUTPUT LOAD CAPACITANCE (C): (IN PICOFARADS) — C = ______ pF

REGISTER PERCENTAGE (R): (GATE COUNT OF REGISTERS/TOTAL GATES) — R = ______

INTERNAL POWER DISSIPATION (P_{int}) (IN MILLIWATTS)

$P \times F \times G \times \{[R \times 0.1] + [(1 - R) \times 0.3]\} = P_{int}$ — P_{int} = ______ mW

EXTERNAL POWER DISSIPATION (P_{ext}) (IN MILLIWATTS)

$0.25\ mW \times F \times B \times 20\% \times C = P_{ext}$ — P_{ext} = ______ mW

TOTAL POWER DISSIPATION (P_{tot}) (IN WATTS)

$P_{int} + P_{ext} \times .001 = P_{tot}$ — P_{tot} = ______ W

JUNCTION TEMPERATURE (T_j) (IN DEGREES CENTIGRADE)

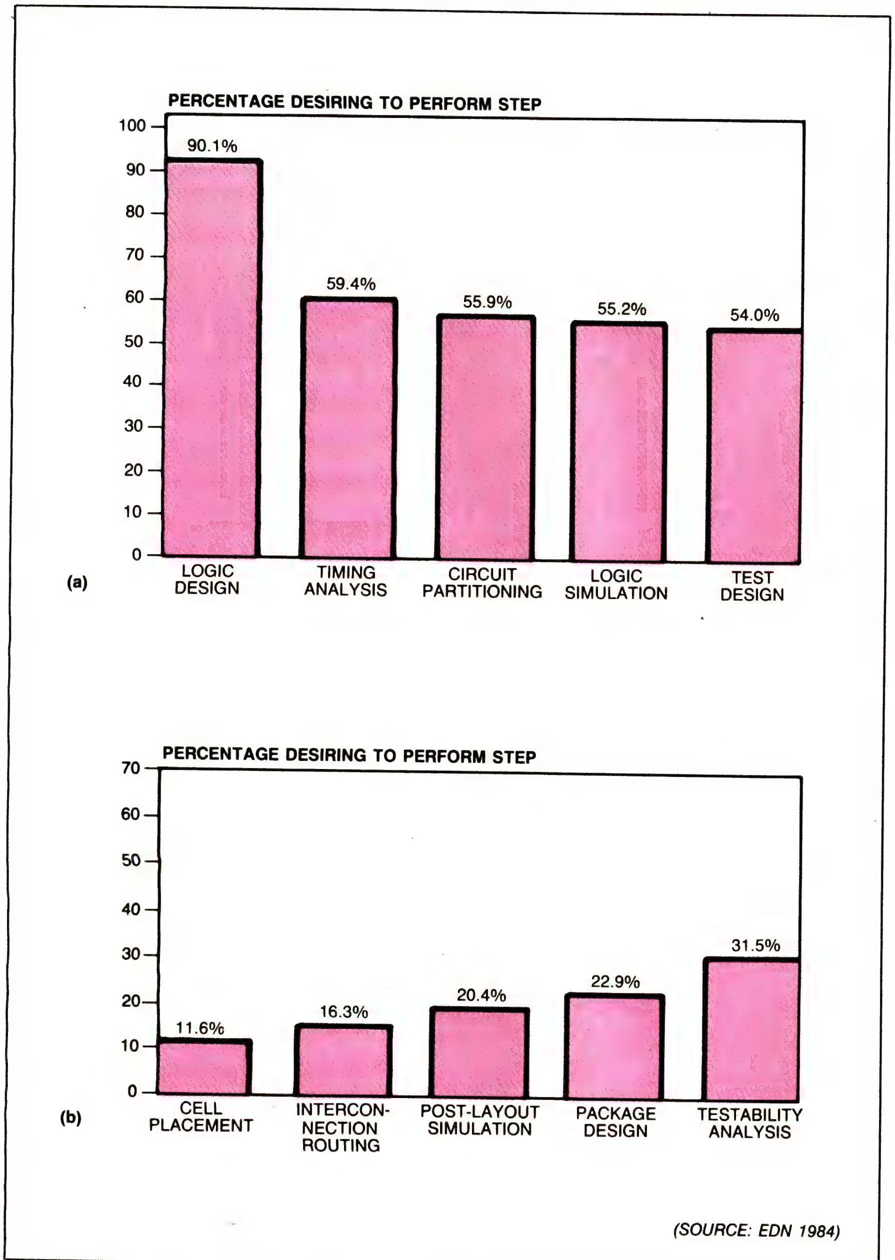
$(P_{tot} \times \theta_{ja}) + T_a = T_j$ — T_j = ______ C

(SOURCE: LSI LOGIC CORP)

***A power-consumption estimate** is part of the up-front engineering offered by design centers. This form, used by LSI Logic Corp (Milpitas, CA), provides a record of power-calculation data.*

Get consultation up front

The two approaches mentioned above represent the ends of the spectrum of available services



***Layout and test steps should be automated** to speed those undesirable parts of the design process. The percentage of designers desiring to perform logic design is high **(a)**; therefore, the front-end tools must be flexible. The less-desired back-end steps **(b)** should require little designer intervention.*

provided by most design centers. In order to cover this spectrum, design centers supply flexible engineering support as well as training and consultation.

The final goal of any design center's efforts is to produce working prototypes that can be fabricated in a silicon foundry. Prototypes require IC layout data, which in turn evolves from verified logic designs. The design center, therefore, must first solicit design projects that are appropriate for their semicustom products. That's why, upon contacting a design center, you can expect a field-applications engineer (FAE) to arrive promptly at your doorstep.

During this first stage of consultation, the FAE must find the best way to partition your circuit for semicustom-IC implementation, taking into account the pinout and gate count of the available devices and packages. Also, the FAE suggests ways to make your design more testable, a critical consideration in IC design. The FAE estimates power consumption, approximate operating frequency, and component cost; you then decide whether to use the design center. In general, a considerable amount of IC- and system-design consultation occurs before you sign a contract or pay for the development of the design.

The cost of the initial consultation is absorbed by the design center either through its design fees (also known as nonrecurring engineering, or NRE, fees) or through its IC-production fees. In either case, the design center guarantees itself a steady flow of projects only by offering the customer a choice of levels of involvement.

Design centers will train

To offer such a choice, the design center must be prepared to train you in the use of its CAE design tools. More often than not, the logic-design tools run on the latest workstations as well as on popular computers, and the design center includes the use of its equipment in the NRE cost (although many centers charge for CPU use as well).

The value of this training on the design center's equipment extends beyond your present design project. According to EDN research (**Ref 1**), the average number of semicustom-IC designs begun by companies already using semicustom ICs grew by 44% between 1983 and 1984. In addition, the average number of semicustom-IC designs performed per designer, now 3.3, is expected to increase to 4.6 by 1986. Such statistics suggest that your initial foray into semicustom design will lead to further involvement in the technology. For this reason, the quantity and quality of your training can directly benefit future designs.

The engineering training and support and the CAE exposure would be small rewards if your chip did not

Circuit design for semicustom ICs

Translating your pc-board-based design into a semicustom-IC implementation requires considerations peculiar to IC design and to the structures of semicustom ICs. You can expect circuits designed according to the following guidelines to be converted quickly and efficiently into the vendor's macrocells and then placed and routed without significant manual intervention.

- Make your circuits synchronous.
- Keep your buses external to gate-array chips. Routing buses in gate arrays is inefficient and usually consumes excessive power in fast systems. Gate arrays are best for combinational (glue) logic.
- Try to partition your design into stand-alone blocks with the minimal number of interconnections. (**Ref 2** contains a detailed discussion of system partitioning.)
- If you use 3-state buffers within the chip, never let their outputs float. If the outputs drive any inverter pairs, they can succeed in turning on both devices at once, causing excessive power consumption and possibly device failure.
- Don't design in any structures, such as delay chains and one-shots, that depend on raw gate speed for delay. Those functions should be provided in the macro library.
- Don't implement large amounts of RAM or ROM on semicustom devices. Standard memory components are much more cost effective.
- Allow for several pairs of power and ground pads, especially in designs with high I/O counts. Typically, you'll need one pair of power and ground pads for every 16 outputs that could change state at the same time.
- Avoid large fan-outs on edge-sensitive signals, and keep rise and fall times as short as possible to avoid having both transistors in inverter pairs turned on for long periods.
- Minimize gate input counts. (Two-input gates are faster than 4-input gates.) In CMOS, NOR gates are faster in high-to-low transitions than NAND gates; NAND gates are faster in low-to-high transitions than NOR gates.

By following these suggestions, you should be able to find a vendor that can fabricate a CMOS semicustom IC operating at clock rates as high as 50 MHz, or a TTL device functional to 200 MHz, or an ECL implementation running at 500 MHz.

Because of the limited number of I/O connections on an IC, expanding gate counts are aggravating the problems of testing. As all design centers will counsel you, introducing test considerations and structures early in your design cycle will save time, money, and considerable vexation—not to mention the time spent on production-floor testing—as you verify your prototype. Some suggestions will increase the testability of your design.

- Combinational logic is much easier to test than sequential logic, which must be initialized.
- When you use sequential logic, add test points, reset lines, shift-register structures, or other means of initializing and controlling the states of the logic.
- Break up long counters; add logic that allows you to control the state of the counters without requiring you to clock through the entire sequence.
- Use test pins to exercise your I/O buffers independently of the internal logic.
- When specifying timing relationships between signals, try to allow enough margin to take into account the skew of the tester.
- Determine a test strategy early in the design cycle, such as one based on LSSD (level-sensitive scan design) techniques, and stick to it. Many macro libraries include cells that support a particular test strategy. Take advantage of other test structures that might already exist on the chip.
- Partition the design into separate units that you can control and test individually.

The following articles provide more information on designing for testability.

- Bennets, R G, "Practical Guidelines for Designing Testable Custom/Semicustom ICs," *VLSI Design*, April 1984.
- Williams, T W, et al, "Design for Testability—a Survey," *IEEE Transactions on Computers*, January 1983, Vol C31, No 1.

In addition, the proceedings from the International Test Conferences held annually in Philadelphia, PA, contain numerous papers about designing for testability.

perform to expectations. That's where the center's design expertise comes into play: Operating as part of your internal design team, the design center has the tools and the personnel to complete your design within a specified time frame, barring the unforeseen difficulties that can attend any engineering project.

In addition, because the design center has an intimate relationship with its manufacturer and familiarity with your design, it shields you from many of the typical difficulties that can appear when moving from the design stage to fabrication and testing. As a result, most projects meet success with the first batch of prototypes.

Because of this widespread first-pass success, you have the luxury of considering the other aspects of semicustom design when you choose a design center. Exploiting its experience and facilities can offset some of the aspects that discourage semicustom-IC implementation. EDN studies show that users consider high development costs, long development times, high unit costs, and lack of in-house experience to be some of the most discouraging aspects of using semicustom ICs (**Ref 1**). By gaining as much design experience as you can from the design center, you can reduce the time and cost required for each subsequent project, and you can increase your understanding of the present project. (See **Ref 2** for more analysis of users' perceptions.)

There are three types of semicustom design centers, which differ according to their relationship to the IC manufacturer. First, many manufacturers have their own design centers; these centers enjoy close ties to the manufacturer's design systems and experience. In the second arrangement, distributors are opening design centers that can offer a wider range of semicustom products than a single manufacturer could. This type of business, in

Analysis of semicustom-IC cost

These two tables are part of the process that Schweber Electronics uses to estimate the cost tradeoffs of using semicustom instead of standard ICs. You can use them as an example of how to determine the economic viability of implementing your pc-board-based design in a semicustom IC.

Table A compiles the costs of acquiring, testing, and inserting standard ICs into a pc board. The total cost for each entry is divided by the number of ICs covered by that entry, yielding an average cost per IC. The total overhead cost per IC is therefore the total of all of the average costs per IC per entry.

You multiply the total overhead cost per IC by the number of ICs to determine the total hidden cost of the option of implementing your IC with standard components **(Table B).** Add the cost of the ICs to the hidden cost to arrive at the total

TABLE A—HIDDEN IC COSTS

DIGITAL SYSTEM COSTS THAT ARE PROPORTIONAL TO THE NUMBER OF ICs (SOURCE: AMI)

PC BOARD	\$20/BOARD	50/BOARD	\$0.40
PC CONNECTOR	\$5/BOARD	50/BOARD	0.10
SUBRACK (METALWORK, GUIDES, LABOR)	\$200/SUBRACK	1000/SUBRACK	0.20
BACKPLANE (SUBRACK GROUND-POWER PLANE)	\$100/SUBRACK	1000/SUBRACK	0.10
WIRE WRAP (AUTOMATIC)	6¢/WIRE	1/WIRE	0.06
POWER SUPPLIES (\$1/W, 70% UTILIZED)	\$1.50/W	10/W	0.15
RACK (INCLUDING DOORS, FANS POWER DISTRIBUTOR)	\$500/RACK	4000/RACK	0.13
IC ORDERING, RECEIVING & INVENTORY	2¢/IC	1	0.02
IC TESTING	8¢/IC	1	0.08
PC BOARD TESTING	\$5/BOARD	50/BOARD	0.10
SYSTEM CHECKOUT	\$800/RACK	4000/RACK	0.20
BYPASS CAPACITORS (INCLUDING INSERTION LABOR)	\$1/BOARD	50/BOARD	0.02
INSERTION & SOLDERING	6¢/IC	1	0.06
INTERCONNECTING CABLES	\$80/RACK	4000/RACK	0.02
MAINTENANCE PANEL	\$300/RACK	4000/RACK	0.07
SYSTEM ASSEMBLY	\$200/RACK	4000/RACK	0.05
SYSTEMS PACKING & SHIPMENT	\$200/RACK	4000/RACK	0.05
SYSTEM DESIGN, DRAFTING & PROTOTYPE CHECKOUT (÷100 SYSTEMS)	\$2000/RACK	4000/RACK	0.50
SERVICE COST FOR 5 YEARS	\$4000/RACK	4000/RACK	1.00
	TOTAL OVERHEAD COST PER IC		= \$3.31

which the distributor becomes a customer to the user and a supplier to the manufacturer, is new ground for distributors. Finally, independent design centers can offer much of the design support of the manufacturer centers while providing some of the range of products of the distributor-owned centers.

In selecting a particular design center, you can readily assess most of the major factors, such as NRE costs, design time, and suitability of product line. Some factors relevant to your choice are subtle, however, and depend upon the nature of your project.

For example, some centers offer low NRE fees and then charge extra for the CPU time you use during your design. Though it appears that you could save money by choosing this route—as opposed to paying a higher, fixed fee—you should be certain that your design is stable. Each iteration of the design cycle can cost as much for CPU time as the previous one, even though you become progressively more efficient in using the tools. Designs that are very large, or designs whose specifications may change, could use a great deal of CPU time.

Is production a goal?

Another factor to consider closely is your commitment to production. Many design centers don't require a production commitment in order to develop your design. This situation is ideal for vendors whose chips may never go into production (for example, chips slated for use in prototypes built for evaluation by the military). But if your chip is defi-

cost of this option. You should also add the cost of designing the logic and laying out the pc board to the total yearly expenditure. This calculation will accurately determine the first-year expense of this option.

The right-hand column shows the calculation used to determine the cost of the option of implementing your design in semicustom logic. The design center estimates the design fee and the price per chip. You should be aware that the semicustom IC also requires overhead expenses like those of the standard IC, and that these expenses add to the chip price that the design center estimates.

This method yields a rough estimate of your potential cost savings using semicustom ICs. For further information on the economies of semicustom-IC use, **Ref 4** contains the results of the EDN hands-on semicustom design series.

TABLE B—COMPARATIVE COST WORKSHEET

STANDARD PRODUCT

NUMBER OF STANDARD ICs IN (A) DESIGN ______

HIDDEN COSTS/IC (B) ______
(SEE REVERSE SIDE)

TOTAL HIDDEN COSTS ______ (AB)

AVERAGE COST PER CHIP (C) ______

TOTAL CHIP COSTS ______ (AC)

TOTAL OPTION COST/UNIT SOLD ______ (AB + AC)

EST UNITS SOLD/YR (D) ______

TOTAL YEARLY EXPENDITURE FOR THIS OPTION ______ D(AB + AC)

ARRAYS

CONVERSION OR NEW DESIGN?
IF CONVERSION-SCHWEBER OR SELF? ______

TECHNOLOGY TO BE USED ______

VENDOR ______

NO. OF FUNCTIONS OR GATES ______

ARRAY TYPE ______

INPUT PINS # ______ OUTPUT PINS # ______

PACKAGE ______

DESIGN FEE (E) ______

PRICE/CHIP (F) ______

CHIP COSTS/YEAR ______ (DF)

TOTAL 1ST YR OPTION EXPENSE ______ (E + DF)

FIRST YR OPTION EXP/UNIT SOLD ______ (E + DF) ÷ D

TOTAL 2ND YR OPTION EXPENSE ______ (FD)

2ND YR OPTION EXP/UNIT SOLD ______ (F)

nitely going into production, a production commitment puts you in the fabrication queue at the foundry. Some manufacturers even arrange to begin preparing for production quantities in parallel with prototype fabrication. Though you bear the production-preparation costs even if the prototype design is unsatisfac-

For more information . . .

The following semicustom IC manufacturers operate or support design centers. For information on design centers in your area, please contact the manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. (EDN's semicustom IC directory, scheduled for February 21, will provide more information on the support and services these firms offer.)

Array Technology
992 S Saratoga-Sunnyvale Rd
San Jose, CA 95129
(408) 252-9900
Circle No 674

Barvon Research Inc
2680 N First St
San Jose, CA
(408) 262-8368
Circle No 675

California Devices Inc
282 Kinney Dr
San Jose, CA 95112
(408) 295-3700
Circle No 676

Custom Integrated Circuits
5353 Wayzata Blvd
Minneapolis, MN 55416
(612) 542-1115
Circle No 677

Custom MOS Arrays Inc
211 Topaz St
Milpitas, CA 95035
(408) 946-9111
Circle No 678

Dumont Alphatron Inc
10351 Bubb Rd
Cupertino, CA 95014
(408) 446-1491
Circle No 679

Exar Integrated Systems Inc
750 Palomar Ave
Sunnyvale, CA 94088
(408) 732-7970
Circle No 680

Fairchild Camera and Instrument Corp
1801 McCarthy Blvd
Milpitas, CA 95035
(408) 942-2660
Circle No 681

Ferranti Electric Inc
Semiconductor Div
87 Modular Ave
Commack, NY 11725
(516) 543-0200
Circle No 682

Fujitsu Microelectronics Inc
2985 Kifer Rd
Santa Clara, CA 95051
(408) 727-1700
Circle No 683

Gould AMI Semiconductors
3800 Homestead Rd
Santa Clara, CA 95051
(408) 246-0330
Circle No 684

Harris Semiconductor
Box 883
Melbourne, FL 32901
(305) 724-7407
Circle No 685

Honeywell Digital Products Center
1150 E Cheyenne Mountain Blvd
Colorado Springs, CO 80906
(800) 328-5111
in MN, (612) 870-2142
Circle No 686

Hughes Solid State Products
500 Superior Ave
Newport Beach, CA 92663
(714) 759-2942
Circle No 687

Integrated Circuit Systems Inc
1012 W Ninth Ave
King of Prussia, PA 19406
(215) 265-8690
Circle No 688

Integrated Microcircuits Inc
1515 Sixth St
Hopkins, MN 55343
(612) 933-4600
Circle No 689

Intel Corp
5000 W Williams Field Rd
Chandler, AZ 85224
(602) 961-8051
Circle No 690

Interdesign Inc
1500 Green Hills Rd
Scotts Valley, CA 95066
(408) 438-2900
Circle No 691

International Microcircuits Inc
3350 Scott Blvd
Santa Clara, CA 95051
(408) 727-2280
Circle No 692

International Microelectronic Products
2830 N First St
San Jose, CA 95134
(408) 262-9100
Circle No 693

Intersil Inc
10710 N Tantau A
Cupertino, CA 95014
(408) 996-5000
Circle No 694

Kontron Electronics
630 Price Ave
Redwood City, CA 94063
(415) 361-1012
Circle No 695

LSI Logic Corp
1601 McCarthy Blvd
Milpitas, CA 95035
(408) 263-9494
Circle No 696

Master Logic
161 E Evelyn
Sunnyvale, CA 94086
(408) 732-7777
Circle No 697

Matra Design Systems
120B Albright Way
Los Gatos, CA 95030
(408) 370-0977
Circle No 698

MCE Semiconductor Inc
1111 Fairfield Dr
West Palm Beach, FL 33407
(305) 845-2837
Circle No 699

Mitel Semiconductor
350 Leggett Dr
Kanata, Ont, Canada
(613) 592-5280
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Mostek Corp
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Box 20912
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NCR Corp
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NEC Electronics USA Inc
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252 Humboldt Ct
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Irvine, CA 92714
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RCA Solid State Div
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(201) 685-6223
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Signetics Corp
Box 409
Sunnyvale, CA 94086
(408) 739-7700
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STC Microtechnology
2270 S 88th St
Louisville, CO 80027
(303) 673-5151
Circle No 710

Telmos Inc
740 Kifer Rd
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(408) 732-4882
Circle No 711

Texas Instruments
Box 202129
Dallas, TX 75220
Phone local sales office.
Circle No 712

Universal Semiconductor Inc
1925 Zanker Rd
San Jose, CA 95112
(408) 279-2830
Circle No 713

VLSI Technology Inc
1109 McKay Dr
San Jose, CA 95131
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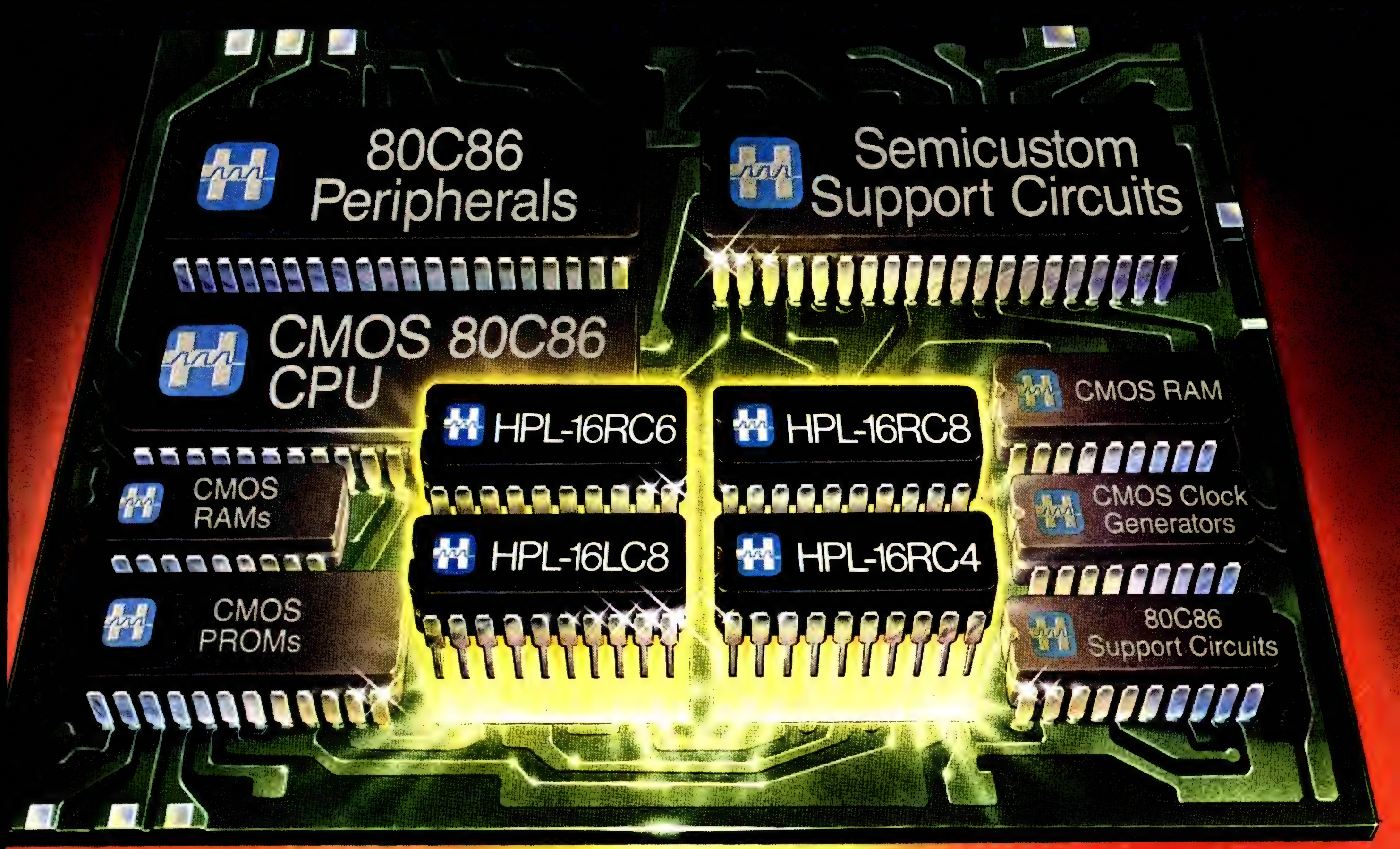

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HPL-16RC4*	Replaces 16R4, 16RP4	5 mA/MHz	
HPL-16RC6*	Replaces 16R6, 16RP6	5 mA/MHz	
HPL-16RC8*	Replaces 16R8, 16RP8	5 mA/MHz	

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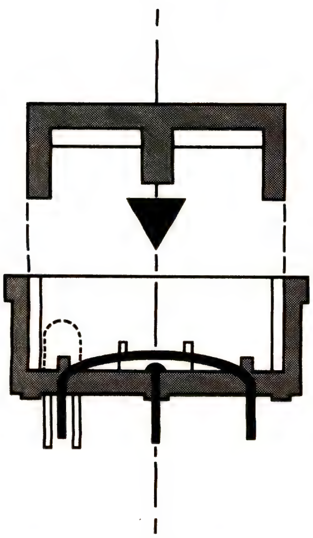

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tory, this approach can shave weeks off IC production should your prototype prove acceptable.

Other factors distinguishing design centers depend on the manufacturer that operates the center or supports its libraries and CAE tools. For example, if a manufacturer's semicustom devices support macros that allow you to specify speed-power combinations, that manufacturer's design center might be best equipped to develop your design efficiently. By using low-power, low-speed macros in noncritical parts of your circuit, the critical paths can be designed for higher speeds without exceeding the power-dissipation limits of the IC. This is particularly important in high-current technologies such as ECL. Designing with these macros can reduce the number of gates required for the critical paths by eliminating buffers and drivers.

Some manufacturers test critical paths during assembly to verify the performance of the devices. Because the number of paths tested varies among vendors, you should determine how many paths your design requires for adequate timing verification. Be sure that your design center performs timing analysis for the necessary paths, and that the manufacturer can test them.

Understand the CAE tools

The success of any semicustom project depends on the accuracy and ease of the CAE tools. The EDN research referred to earlier indicates that, although designers want to maintain control over logic design, they don't look forward to IC-specific tasks—layout, testability analysis, and package design. A CAE system that automates these tasks (the back end of IC design), while giving maximum flexibility to the logic design and analysis (the front end), eases and speeds IC development.

The back-end tasks are the critical steps in assuring that prototype performance matches the logic simulation. Therefore, the software for those tasks is mostly proprietary to the IC manufacturer and runs on the IC manufacturer's mainframes or minicomputers. To execute these steps in the design process, you will be working on those systems; if you already use the same kinds of computers, you won't waste time learning a new machine. Furthermore, if the manufacturer sells its software, porting to your system is a simple task. You should also watch for the use of standard operating systems and database formats.

At the front end of the design, you might be able to use an IBM PC to run programs for schematic capture and even for logic simulation. Many design centers can interface to these packages—a clear advantage if you're already using IBM PC-based design programs. The same reasoning holds for workstations: Examine how much of the design cycle your workstation can perform before you have to begin using the vendor's design system.

As a final selection criterion, be aware that many design-center CAE systems can include an estimation of the loading effects of interconnect routing during the initial timing simulations. The loading effects are calculated from statistical data relating approximate wire length (and hence loading) to fanout. This capability can prevent surprises—and the need for redesign—when postlayout simulation occurs.

Evaluate training aspects

If you consider the CAE capabilities as largely vendor-dependent, then the training aspects represent the area in which, all vendor-related aspects being equal, you should evaluate individual design centers. (Of course, not all vendors are created equal.)

Typically, training consists of several days of instruction and demonstrations in the use of the design system, combined with an introduction to the products and IC technology. You should be able to bring in

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your intended design to work on in class. In fact, some centers claim that you can not only complete your logic design and simulation but also begin layout and resimulation during the training. Training costs usually are not included as overhead in other design-center charges; for a design group of three to 10 people, training typically costs $3000 to $5000.

The training should extend beyond the manipulation of the CAE software. Look for centers that teach design methods for testability, testability analysis, fault grading and analysis, and circuit partitioning. These topics are essential for IC design, and the more exposure you receive, the more advantage you can gain from choosing IC-based implementation.

Finally, receive training as soon as you decide to implement your design in semicustom ICs. Through an expanding knowledge of semicustom design and the help of the design center, you can create efficient IC designs quickly. In addition, redesign can cost you more time and money than an initial investment in extra expertise. **EDN**

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4. Rappaport, Andy, "Hands-on chip analyses determine project success," *EDN*, June 28, 1984, pg 212.

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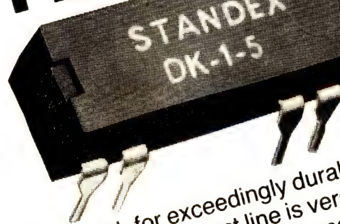

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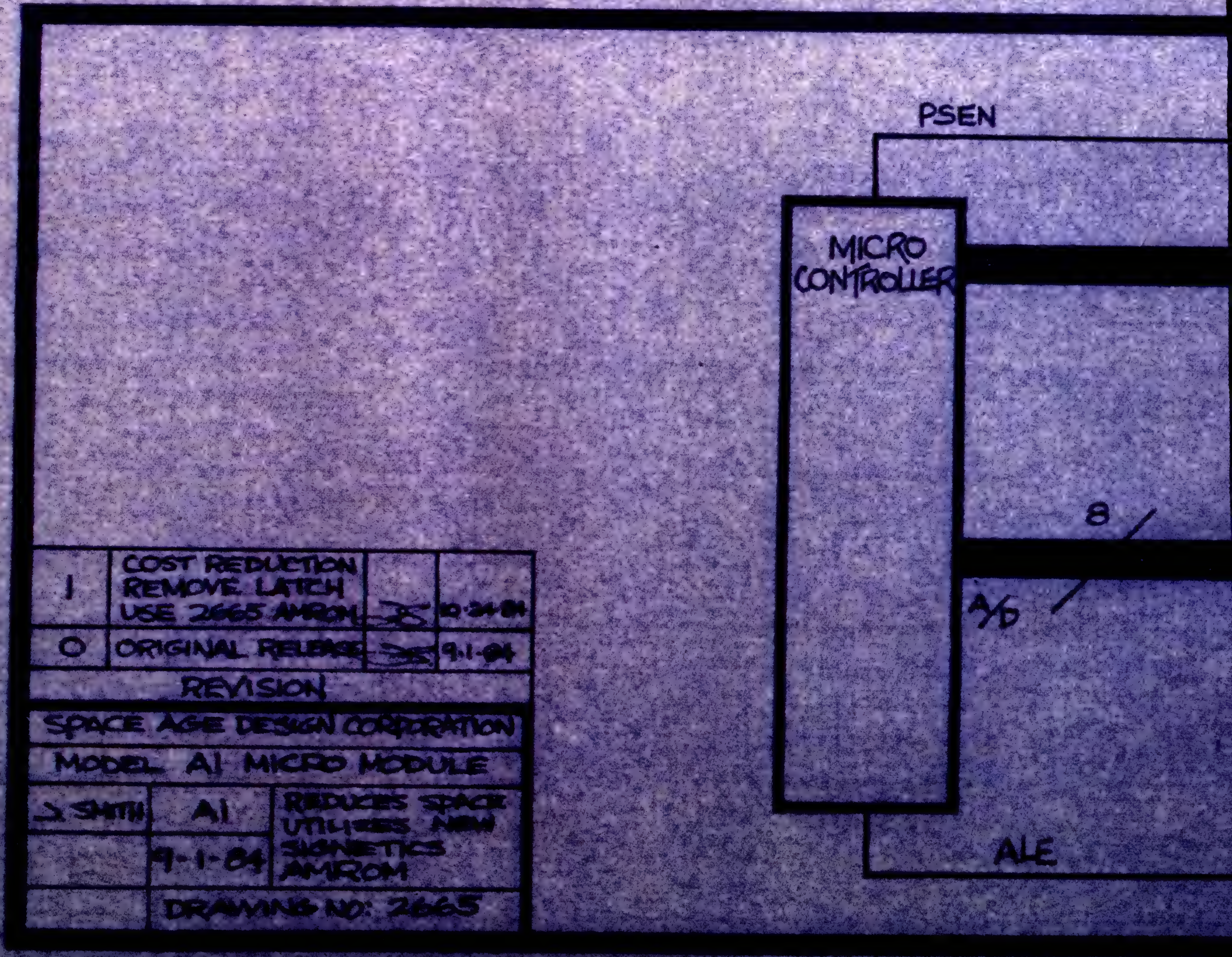

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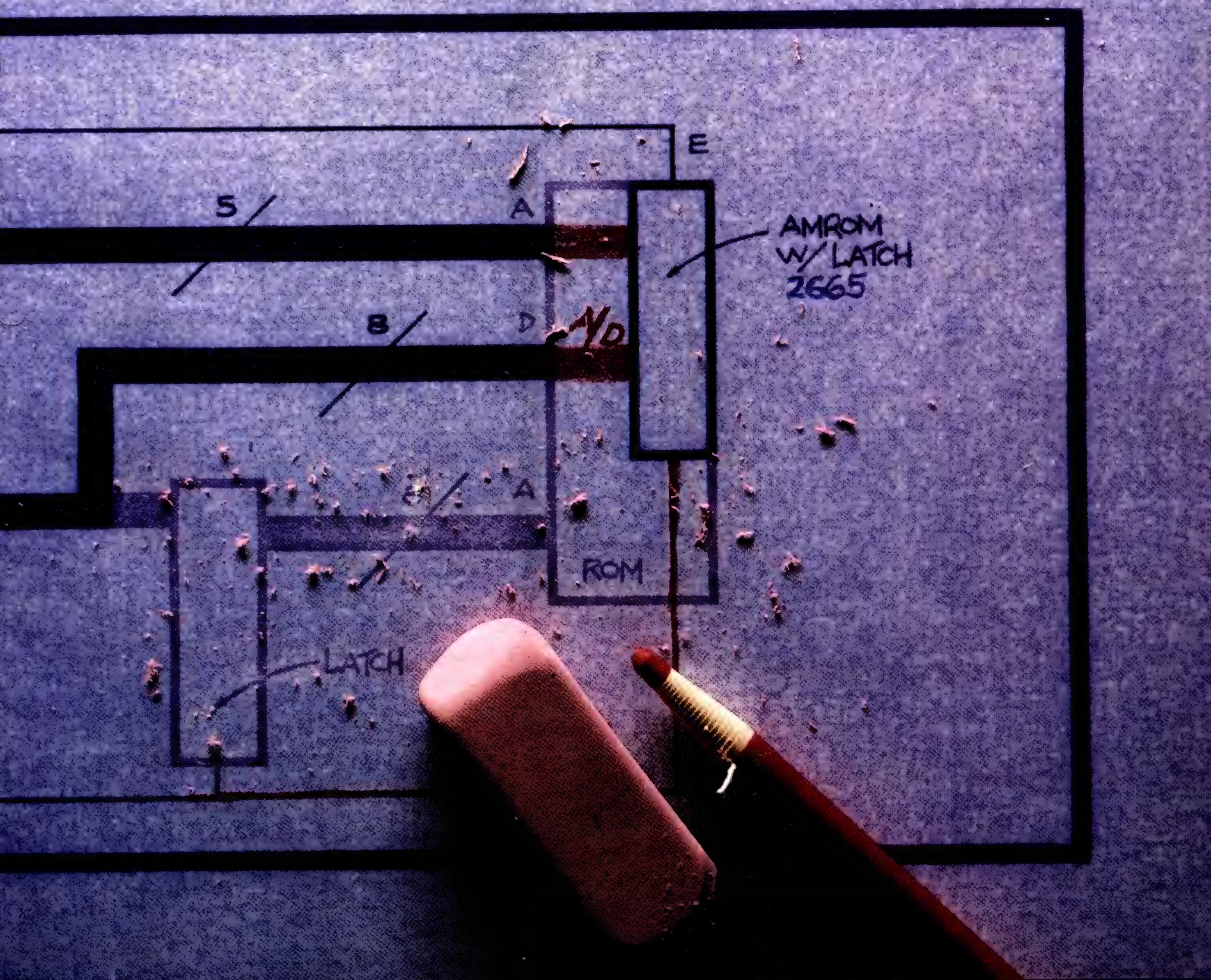

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CIRCLE NUMBER 253

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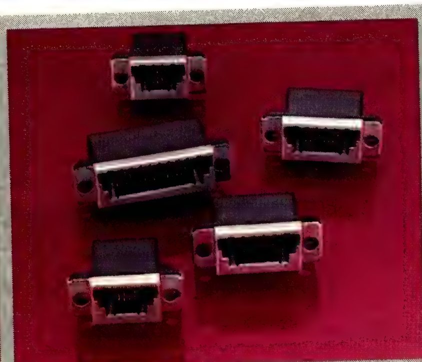

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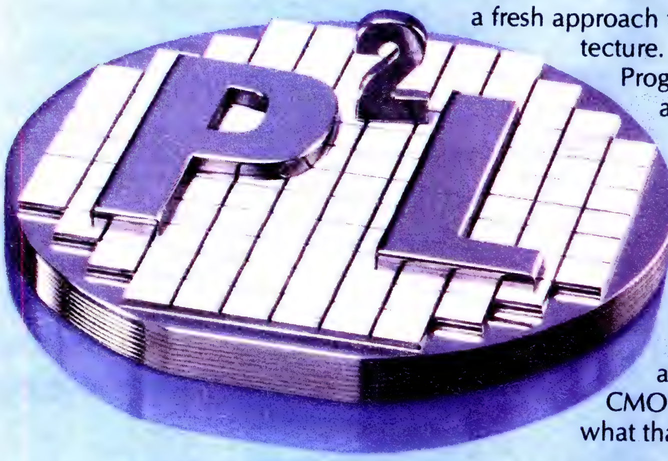

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CIRCLE NO 191

Conductive EMI/RFI shielding materials answer challenge posed by FCC regulations

Robert M Clarke,
Assistant Editor

All electronic devices, especially computing devices, must comply with FCC EMI/RFI regulations. A wide variety of shielding materials is available, but to choose the right material for your product, you must consider several factors, including shielding effectiveness, cost, bulk, weight, environmental tolerance, and appearance.

There are two basic methods of shielding a product: You can either apply a conductor to an existing component or enclosure by taping, spraying, or painting it on, or you can construct an enclosure out of one of several conductive plastics.

In any case, different products will require different shielding materials. To determine which materials provide the best shielding effectiveness (SE) for your product, you have to experiment: You have to use different materials to shield your product, conduct EMI/RFI tests, and compare results.

***Electrically conductive plastics** from Wilson-Fiberfil International let you fabricate shielded parts and enclosures in a variety of shapes and sizes. The plastics use continuous-roll fillers such as (rear, left to right) milled glass, carbon fiber, stainless steel, or chopped fillers such as (front, left to right) carbon fibers, stainless-steel fibers, and aluminum flakes.*

Tests to determine SE vary, and different tests can be used at different frequency ranges. The accompanying **box** discusses a method that's used for low-frequency testing.

Manufacturers' SE specs are another variable: Some manufacturers rate their materials' SE at spot frequencies, such as 30 MHz or 1 GHz, while others provide graphs of their products' SE vs frequency performance across a range such as 1 MHz to 1 GHz.

Moreover, SE can be a function of the thickness of the shielding material as well as the quality of its conductive additives. So when you choose among shielding methods, you often have to compare different processes—paint, electroless plating, or conductive plastic, for instance. You also have to compare materials made by different manufacturers.

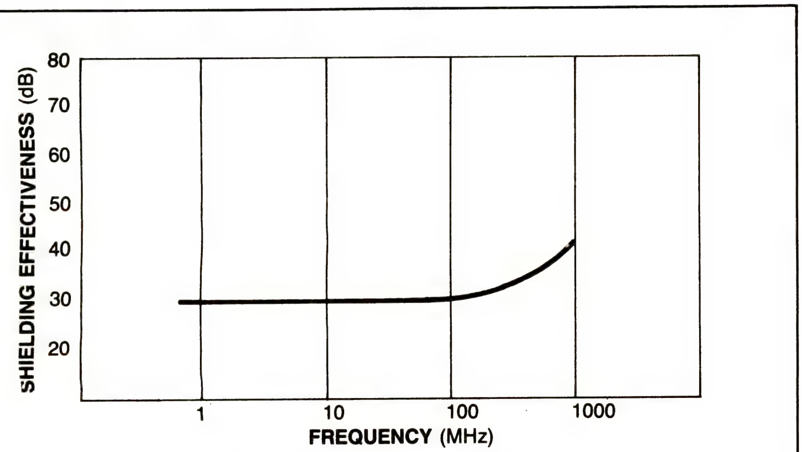

***Fig 1—E-kote 3064** from ACME Chemicals and Insulation Co provides EMI/RFI shielding across the 1- to 1000-MHz range.*

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Together, we can find the answers.

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CIRCLE NO 38

Conductive coatings take several forms: wire sprays, paint, electroless plating, vacuum metallization, and metal foils and tapes. Such coatings are used most often on products on which you can't use a conductive material like metal or a conductive plastic. Typically, conductive coatings are used to shield glass, ceramics, rubber, and nonconductive plastics like polystyrene, polycarbonate, and polyester. Although they provide good shielding, conductive coatings are susceptible over time to wear and flaking.

If you use arc-sprayed zinc, for example, you'll have good shielding results (its SE can be as high as 120 dB) and good conductivity as well as a hard coating. Because the conductor is essentially a contiguous, albeit thin, sheet of metal, the shielding is effective over a wide frequency range. However, you need special equipment to use arc-sprayed zinc, and you must take special precautions.

Paint-on solutions

Although conductive paints provide less shielding (SE as high as 70 dB) than metal coatings, they can be applied with conventional spraying equipment. Acme Chemicals and Insulation Co supplies conductive paints that use conductors such as silver, nickel, or copper as pigments and an acrylic as a binder. This E-kote line of paints contains polar solvents such as xylol or (for solvent-sensitive plastics) nonpolar solvents such as diacetone alcohol. **Fig 1** shows the typical SE of one member of the E-kote line, E-kote 3064.

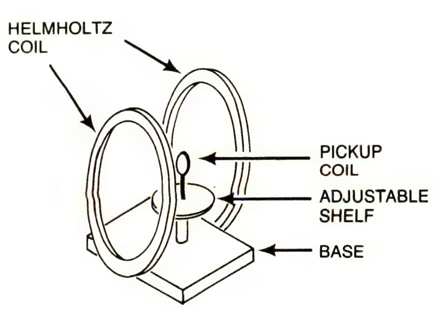
Another conductive-paint manufacturer, Emerson & Cuming, makes a waterborne conductive paint as part of its Eccocoat line. Eccocoat CC-33W is a nickel/acrylic paint whose SE ranges from 32 to 57 dB at 30 to 1000 MHz. Chomerics, a maker of paints and conductive elastomers, sells its Cho-shield line of

Testing SE at low frequencies

Donald R Friesen
The Electro-Mechanics Co

You can perform a straightforward test to find how effectively certain shielding materials attenuate low-frequency magnetic fields. The test can determine shielding effectiveness (SE) over a of 30-Hz to 30-kHz frequency range, although the line frequency is usually the frequency of interest.

The test method requires immersing a hollow test sample in a known, homogeneous magnetic field and measuring the attenuated field inside the sample. This is the basic test procedure described by the American Society for Testing and Materials (ASTM) in test method A 698-74 (available from the Society at 1916 Race St, Philadelphia, PA 19103).



(SOURCE: ELECTRO-MECHANICS CO)

By shielding a pickup loop with a test sample *and using the magnetic field produced by a Helmholtz Coil, you can measure the sample's shielding effectiveness at low frequencies.*

To perform the test, you first form the material to be tested into a shield, which will cover the pickup loop that is used to detect the field inside the sample. Generally, a cylindrical form is used for the shield with a cap on one end if necessary.

Then, you must produce a homogeneous magnetic field; you can produce one by using a Helmholtz Coil System, which consists of a pair of identical coils arranged so that they have a common axis. The spacing between the coils is equal to the coils' radius (**figure**). A pickup loop is located between the coils. You can excite the Helmholtz Coils by connecting them to the power mains, either directly or through a transformer, or by connecting them to a power amplifier and associated low-frequency (eg, audio) oscillator. (To calculate the strength of the magnetic field, you simply monitor the current flowing through the coils.)

When you've established magnetic field between the coils, you measure the induced voltage in the pickup loop. Then you slip the test sample over the pickup loop and measure the induced voltage in the pickup loop. You can calculate the SE using the following equation:

$$SE = 20\log_{10}(V_1/V_2)$$

where SE is the shielding effectiveness in dB, V_1 is the induced voltage in the unshielded pickup loop, and V_2 is the induced voltage in the shielded pickup loop.

The author is a design engineer with the Austin, TX firm.

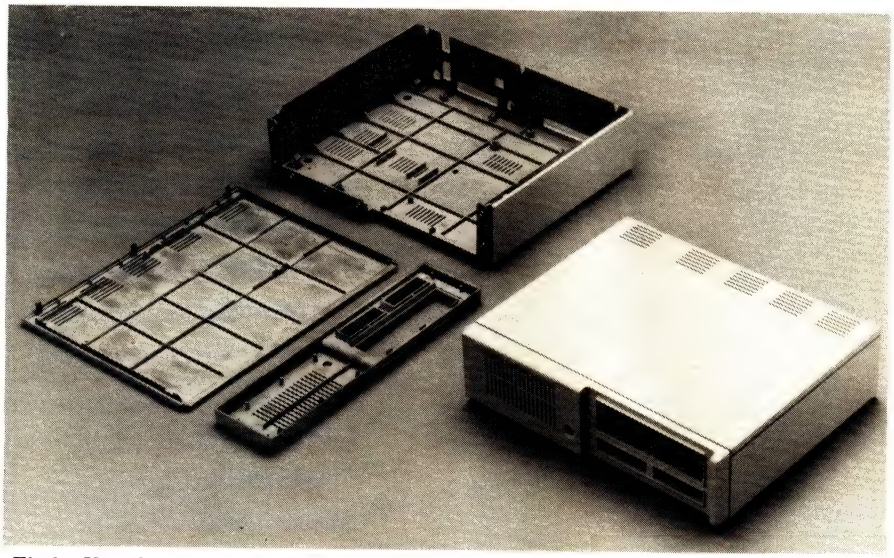


Fig 2—Use of copper and nickel in the electroless-plating process won for the IBM PCjr the American Society of Electroplated Plastics' (ASEP) Best Application award. (Photo courtesy ASEP)

conductive paints in ready-to-use or concentrated form. A 2-mil-thick coating of this paint provides an SE of 25 to 30 dB at 30 to 200 MHz.

Plated plastics emerge

Another way to add an EMI/RFI shield is to apply electroless plating, which is used with plastic components. You apply the plating by immersing the plastic in a series of chemical baths. The first bath etches the material to prepare its surface for electroless metal plating; this process allows good metal-to-plastic adhesion. Metal plating takes place in subsequent baths. Electroless nickel or copper plating coats all surfaces of an object uni-

TABLE 1—ELECTROLESS-PLATING COMPANIES

	IN-HOUSE MOLDING		PLASTICS PLATED FOR EMI							ELECTRO-LESS SHIELD		DECORATIVE FINISHES		PART-SIZE CAPABILITY				OTHER SHIELDING CAPABILITY		PLANT LOCATIONS			
	INJECTION MOLD	FOAM MOLD	POLYSTYRENE FOAM	POLYCARBONATE FOAM	ABS FOAM	MODIFIED PPO/PPE RIGID	ABS RIGID	MODIFIED PPO/PPE FOAM	POLYESTER	ELECTROLESS COPPER	ELECTROLESS NICKEL	ELECTROPLATED	PAINTED	SMALL (CONNECTORS)	MEDIUM (KEYBOARDS)	LARGE (CRTs/CABINETS)	PROTOTYPE PLATING CAPABILITY	FILLED PAINT	ZINC ARC	EAST	MID-WEST	WEST	CANADA
A-BRITE PLATING CO											•	•	•	•	•						•		
ASTRO ELECTROPLATING INC					•	•	•	•			•	•	•	•	•	•	•			•			
CHEMPLATE CORP			•	•	•	•	•	•	•	•	•	•	•	•	•	•	•					•	
CROWN CITY PLATING CO	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•				•	
DETROIT PLASTIC MOLDING CO	•	•	•		•	•	•	•		•	•	•	•	•	•	•	•	•	•		•		•
E/M LUBRICANTS INC			•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	•	•	
FCM PLASTICS, PLASTICS TECHNOLOGIES INC	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•		
GENERAL SUPER PLATING CO	•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•		•			
GENRON INC	•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•		•			
GP TECHNOLOGIES INC											•	•		•	•		•			•			
LACKS INDUSTRIES INC	•						•			•		•	•	•	•	•	•				•		
LEAR SIEGLER INC	•						•	•		•		•	•	•	•		•				•		
NI INDUSTRIES	•									•		•	•	•	•	•	•				•		
PHILLIPS PLASTICS CORP	•										•	•	•	•	•		•				•		
PLASTIC-PLATE INC	•						•	•		•	•	•	•	•	•	•	•				•		
PLASTICS HOLDINGS LTD	•			•	•		•		•	•	•	•	•	•	•	•							•
SHELLER-GLOBE CORP, HARDY DIV	•	•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•			•		
WINDSOR PLASTICS INC	•	•			•		•				•	•	•	•	•	•	•	•			•		

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formly, regardless of the object's shape. This process provides an SE ranging from 65 to 120 dB.

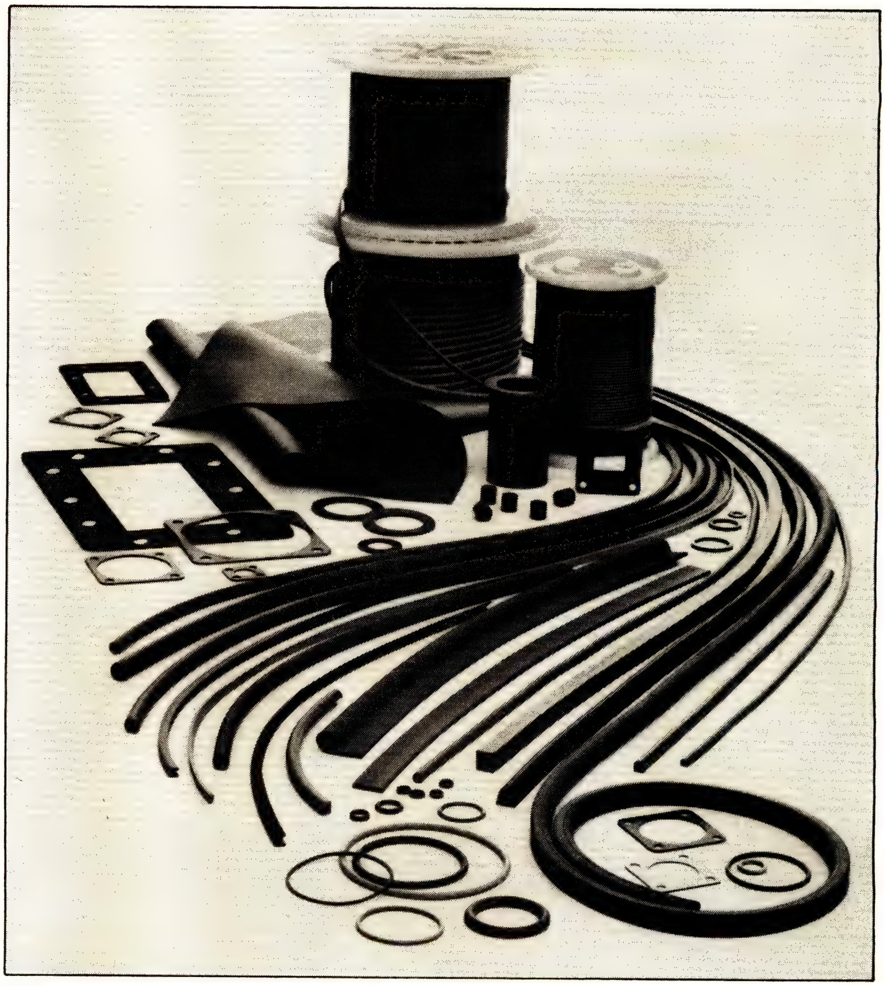
The electroless-plating process lends itself well to bulk processing; personal-computer shielding is one common application **(Fig 2). Table 1** lists some of the companies that provide electroless plating.

Fillers add shielding to plastics

A recent trend in EMI/RFI shielding calls for adding a conductive filler to various plastics. Manufacturers can mold the resulting conductive plastics to make EMI/RFI-shielded parts. This eliminates the need to handle the product again to add shielding to the material. Common conductive fillers are polyacrylonitrile (PAN) carbon fiber (CF), nickel-coated graphite fiber (NCG), stainless-steel fiber (SS), and aluminum flake (AF). To obtain the desired SE, a certain percentage of the filler must be present in the plastic. The higher the percentage of filler by weight (the filler's "loading") there is in the plastic, the higher the plastic's conductivity will be. A filler's aspect (or length-to-diameter) ratio is also critical. For a given conductivity, the higher a filler's aspect ratio is, the lower the filler's loading can be.

Stainless-steel fillers provide the best conductivity of any filler for a given percentage, but they also cost more than any other filler. On the other hand, less expensive nonmetallic fillers exhibit good mechanical properties (such as tensile strength) and can be more economical for some applications. So when you choose filler, you face tradeoffs in cost, bulk, weight, and mechanical performance (strength and stiffness). **Fig 3** and **Fig 4** compare different fillers and their weights and conductive properties.

Companies that manufacture fillers and plastics can advise you about what combination of fillers and plastics can best meet your needs. Manufacturers of metal fillers include Transmet Corp, which



Conductive elastomers *from Chomerics Inc find applications in EMI/RFI/environmental gaskets, O and D rings, and rolled stock.*

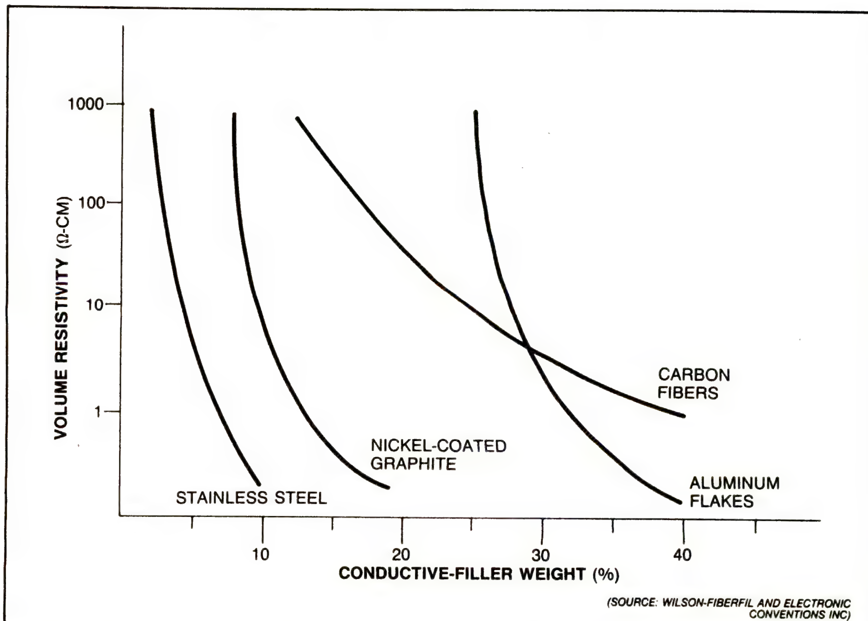


Fig 3—You can compare the percentage by weight of filler *to achieve a given conductivity. The comparison between these four fillers shows that as the percentage by weight of a filler increases, so does the plastic's conductivity.*

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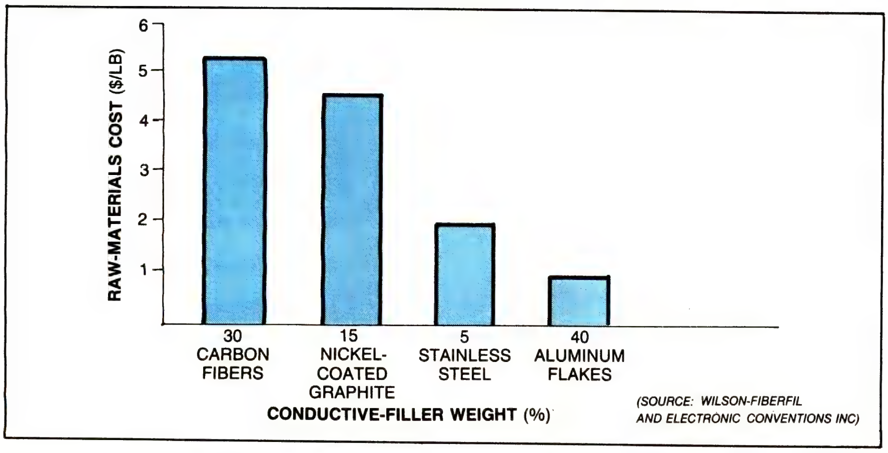

Fig 4—You can juggle a filler material's cost and its shielding performance *to choose the best material for a given application. This graph compares the raw-material cost of conductive fillers to achieve 40-dB shielding.*

ety of materials can help you plug the leaks: conductive gaskets and adhesives and metal foils and tapes.

Chomerics makes conductive-elastomer gaskets for waveguides and connectors. Acting as both RF and environmental seals, the gaskets use silver/copper, silver/aluminum, and silver/glass fillers. The silver/copper-filled gasket, Cho-seal 1215, features an SE greater than 100 dB at 1 GHz; the silver/aluminum-filled gaskets, Cho-seal 1285 and Cho-sil 1485, provide SEs greater than 90 and 70 dB, respectively, at 1 GHz. The silver/glass-

makes aluminum flakes for use in polycarbonate and ABS compounds, and Brunswick Technetics, which produces both stainless-steel and nickel-chromium fibers.

Wilson-Fiberfil manufactures a variety of conductive plastics containing nickel-coated PAN fibers, PAN fibers, aluminum flakes, and stainless-steel fibers. The company's newest filler is made of nickel-coated PAN fibers. A 15% loading of the nickel-coated PAN fibers achieves virtually the same conductivity as a 50% loading of uncoated PAN fibers. The nickel-coated-PAN/plastic compound also has a 55-dB SE—5 dB higher than the SE of the PAN-fiber-filled nylon-66. The company is currently developing other polymer systems—PPS, Peek, and ABS—that contain nickel-coated PAN fibers.

LNP Corp produces aluminum-filled polystyrenes and polycarbonates. Its EMI-X 540, a 40% aluminum-flake-filled polycarbonate, provides an SE of 35 to 40 dB from 0.5 to 1000 MHz.

Plugging the leaks

No matter how effective the shielding material you use for your enclosure or device is, ventilation holes, doors, windows, seams, and apertures for CRT screens can provide an escape route for electromagnetic emissions. Fortunately, a vari-

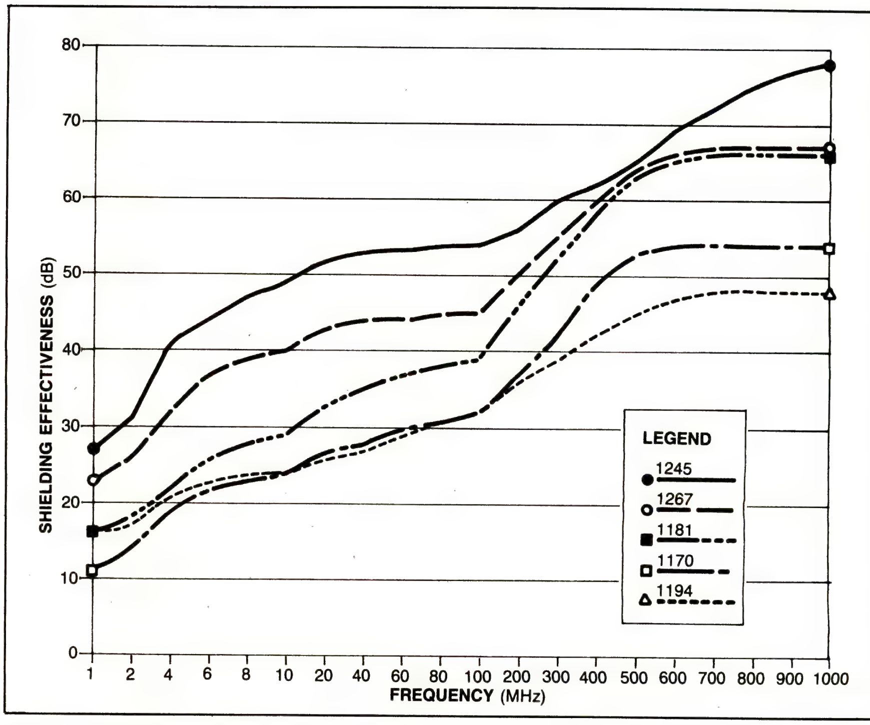

Fig 5—As these testing results demonstrate, *conductive-foil tapes from 3M suit applications from 1 to 1000 MHz.*

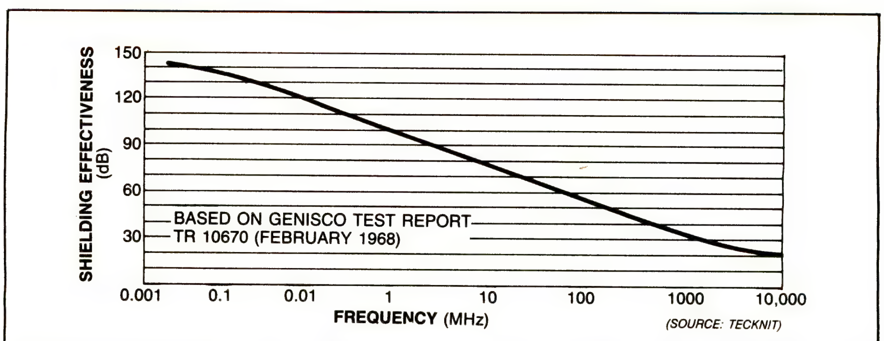

Fig 6—As this shielding effectiveness plot shows, *you can apply an electrically conductive transparent coating to one or both sides of a CRT to shield against EMI/RFI.*

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filled gasket, Cho-seal 1350, offers an SE greater than 70 dB at 1 GHz.

The company markets several other conductive-elastomer-based EMI/RFI-shielding products, including rolls of extruded gasket material, conductive-sheet stock, strain-relief bushings, O-rings, D-rings, and grounding grommets. In addition, the company sells a tape backed with a pressure-sensitive adhesive called Cho-foil. Available in rolls or custom-die-cut configurations, its conductive versions use copper or aluminum.

3M manufactures both smooth and embossed copper- and aluminum-backed shielding tapes. The tapes are used for wrapping transformer cores, shielding connectors and cables, and taping seams in enclosures. **Fig 5** compares the SE of several of the company's tapes.

Tecknit uses knitted and woven wire in the manufacture of its shielding materials. The company supplies wire-mesh gasket material, wire-mesh gaskets, and knitted-wire mesh with elastomer seals as well as clear EMI-shielded coatings and windows. Its window-shielding materials include Teckfilm, a vacuum-deposited thin metal film on a 0.13-mm polyester-film substrate. **Fig 6** shows the film's SE vs frequency.

You can use conductive cements and adhesives to bond metals, plastics, glass, and ceramics. For example, Emerson Cuming's sealant, Eccoshield VY-81, features an 80- to 90-dB SE and a 0.001-Ω/cm resistivity. It provides 105 linear feet of ⅛-in. diameter bead per pound and has a service temperature range of −65 to +400°F. Chomerics' aerospace-grade Cho-seal 1285 features SEs of 70 dB (magnetic) at 10 kHz, >120 dB (electric) at 1 MHz, and 90 dB (plane) at 10 GHz.

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For more information on the products mentioned in this article, contact the following manufacturers directly, or circle the appropriate numbers on the Information Service Retreival card.

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CIRCLE NO 45

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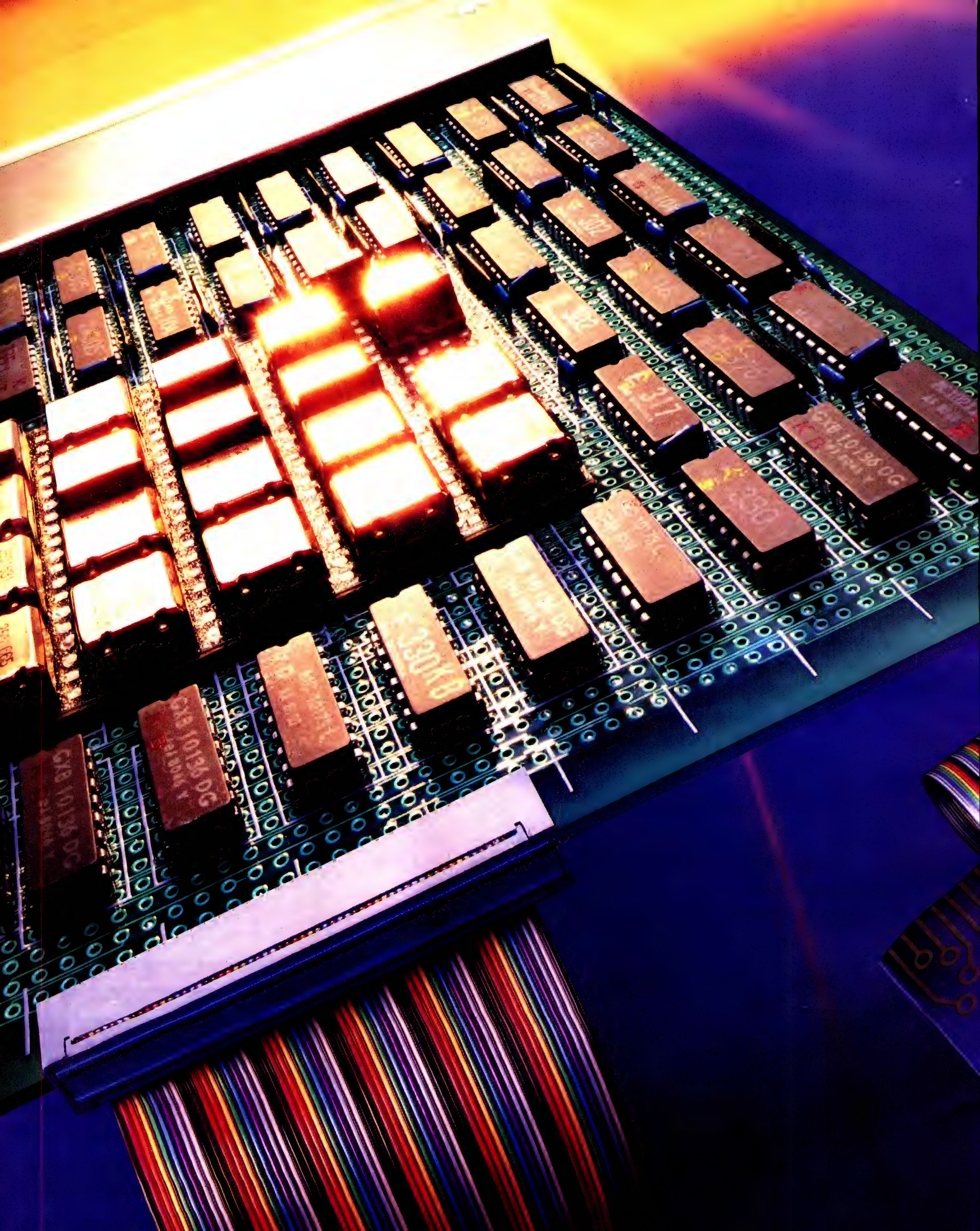

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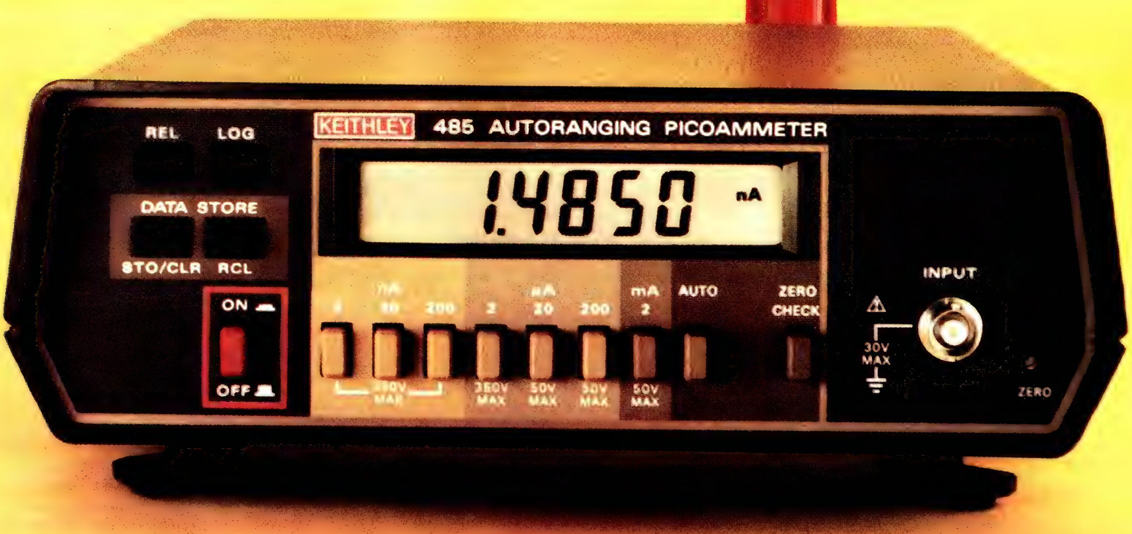


CIRCLE NO 48

First electronics videotex catalog for engineers goes on line

Videolog lets design, standards, and components engineers access current data on more than 500,000 semiconductors. It allows direct communication with manufacturers via electronic mail, and lets you reference a directory of 14,000 suppliers.

The Videolog database employs the North American Presentation Level Protocol Syntax (NAPLPS), an ANSI videotex graphics standard. NAPLPS enables personal-computer users to receive quality graphics over telephone lines. As a Videolog user, you can view full-color displays of logic and circuit diagrams, component shapes, pin-outs, and performance charts.

Detailed manufacturers' catalogs and extensive company listings provide alternative sources for components and services and let you review component-property summaries. The electronic-mail feature lets you get quick answers from suppliers to your questions about specifications, availability, and pricing. Videolog's computer-updated files help you keep up with developments in the electronics industry, lowering your risk of designing products with obsolete components or with information from out-of-date data sheets.

Manufacturers who are supplying current device specifications to Videolog include Texas Instruments, Intel, Motorola, Mostek, Hitachi, Signetics, Zilog, Monolithic Memories, Harris Semiconductor, Advanced Micro Devices, Fairchild Semiconductor, Gould-AMI, Synertek, Siliconix, RCA Solid State, Plessey, Xicor, and Electronic Design. Directories and cross-references from DATA Inc and the Harris Publishing Co are also on line.

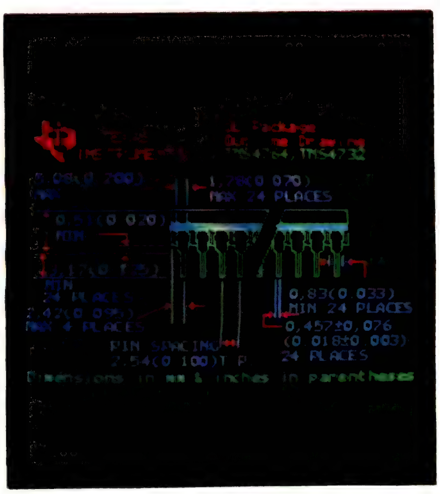
The company offers a free system-demonstration disk upon request by qualified potential users. The disk runs on PC-DOS and MS-DOS systems that have a color monitor, graphics card, and floppy-disk drive. Also available is Videologon software, which provides access to the Videolog database. Videologon is a NAPLPS terminal emulator that lets you access Videolog with your personal computer via a modem. The software, users manual, local telephone number, and ID cost $150.

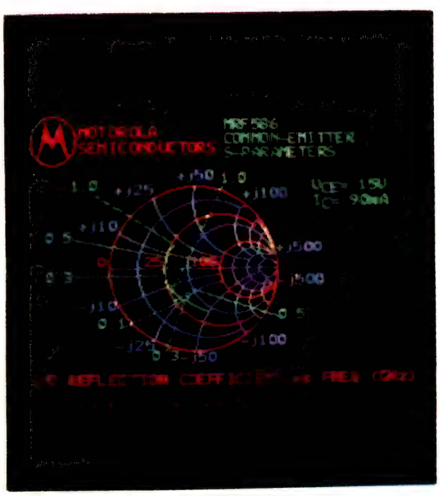
You can access the system with a local phone call, using a nationwide data network. Basic services, including data searches based on a keyword, type number, catalog, or directory, cost $15/hr. For such premium services as component property displays, functional equivalence, and parametric searches, the charge is $39/hr. In Canada, the service is available for a $10/hr network surcharge via the Datapac gateway into CompuServe.

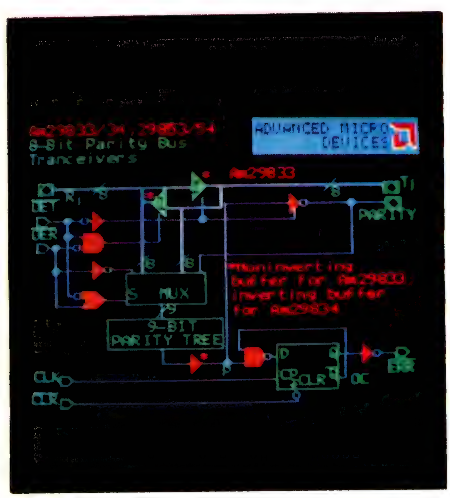
—***J D Mosley***

Videolog Communications, 50 Washington St, Norwalk, CT 06854. Phone (203) 838-5100.

Circle No 742







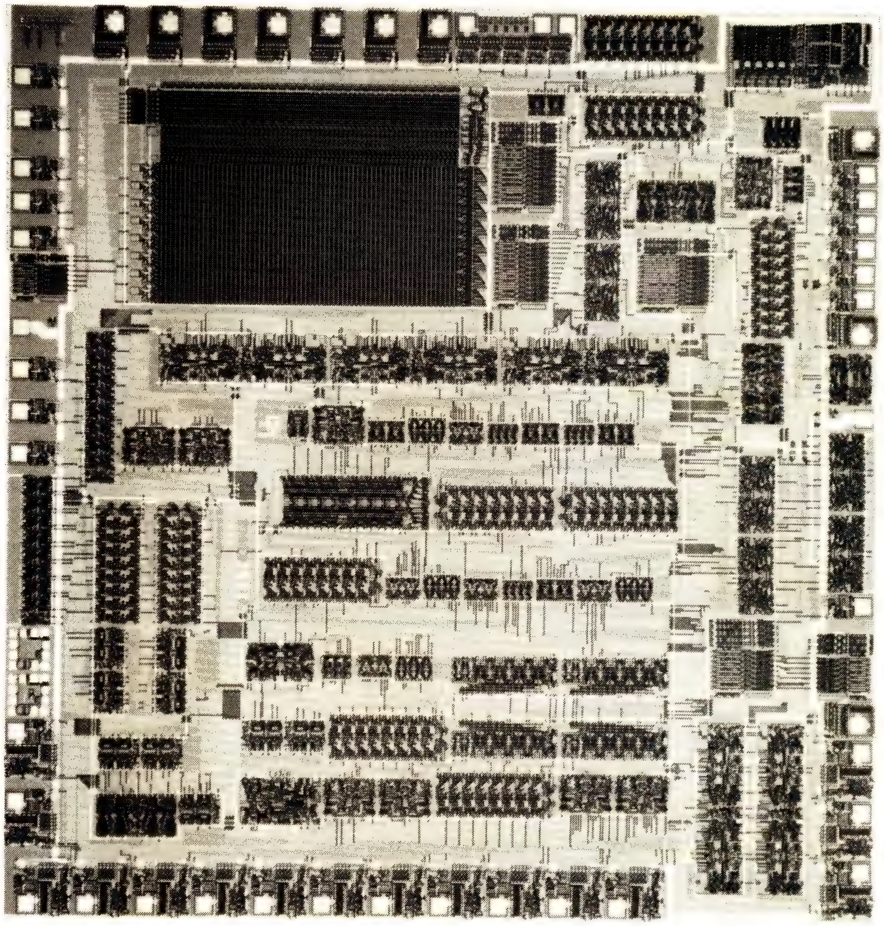
***The Videolog database** lets you access product specifications, operational parameters, and circuit designs with the speed of electronic data communications.*

PC-compatible electronic-design software simplifies standard-cell simulation

The Simulation and Analysis of Logic and Timing (Salt) program extends the range of applications for the IBM PC. Furnishing 12 logical states (including 36 internal states that resolve nodal contentions), Salt can compute total propagation delays at any time during a simulation. The program also features computation of fan-in and fan-out delays, multiple checkpoint restarts, and incremental recompilation. The package classifies transistors as unidirectional or bidirectional, determines critical paths, permits user-specified outputs, and simulates at multiple levels of the hierarchy.

To use Salt, you enter a schematic into your electronic-design workstation and extract the netlist. Salt simulates the circuit's logic and timing hierarchically. Simulations can run from the transistor level to the functional level. If you prefer, you can use a network description language to enter the data.

While the simulation program provides a library of gates and SSI and MSI components, the functional-modeling language lets you specify custom components. The system also lets you specify node decays, and the program evaluates the effect of decaying charges.



This 5-bit D/A converter, *which was designed with the Alphamap library, contains 90 logical elements, 46 I/O cells, and a 1k×18-bit ROM.*

Incorporating the Alphamap standard-cell library into the Salt system enables systems engineers without VLSI experience to lay out ICs. The Alphamap library comprises more than 80 tested, CMOS standard logic functions, which emulate 74LS and CMOS 4000 Series SSI and MSI circuits. Linear and analog cells, as well as ROM and RAM, are also available. A 3-μm Si-gate CMOS process is standard.

Typical turnaround time for fully simulated standard-cell designs is about 14 weeks. This time allows six weeks for design approval and eight weeks for prototype fabrication.

The design and development system includes functional-cell decals and layout-checking software. The layout checker estimates the final die size and the circuit's operating speed.

The Cybernet Connect communications program lets you transmit files between your workstation and a time-shared mainframe. With Cybernet, you can submit job orders and status reports, exchange data and designs, and carry out batch or interactive processing.

Although it's normally integrated with the IBM PC/XT and other PC-compatible machines, Salt, which is written in C, also runs on other minicomputers and mainframes.

Not including the PC/XT, Salt costs $7400. The Alphamap design system is priced at $3495. Tooling costs for standard cells are approximately $35,000.—***Eva Freeman***

Control Data Corp, Information Systems Design, 2500 Mission College Blvd, Santa Clara, CA 95054. Phone (800) 253-4004.

Circle No 744

Continued on pg 106

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For more information about our new mil spec fiber optic connector, or any of our other first-with-the-military multi-channel types, phone Tom Cobb at 714-660-6710. In England, call Hugh McInally at 932-47262.

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CIRCLE NO 49

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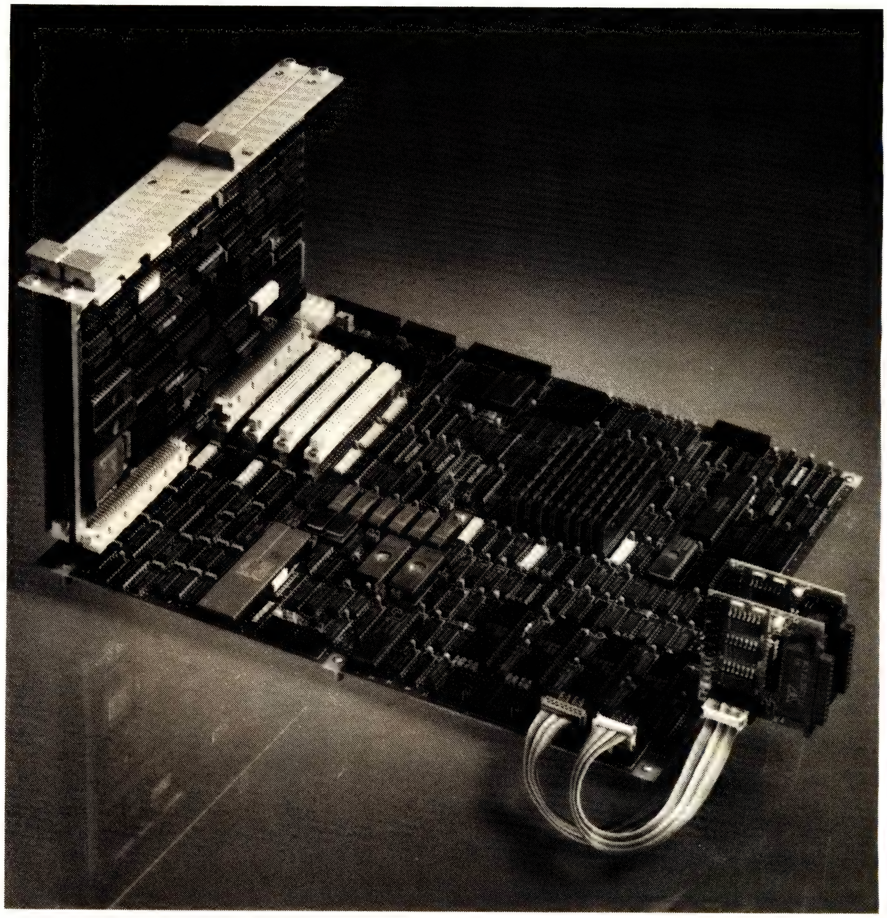
CIRCLE NO 83

Single-board 68010-based μC provides disk and I/O control, five slots

The VSF 1605 Baseboard, also called a VME system foundation, provides an integrated disk controller for rigid- and floppy-disk drives, I/O interfaces, and five VME expansion slots. The Baseboard's 68010 μP runs at 10 MHz and supports virtual memory and demand paging. The board includes a memory-management unit, RAM, ROM, programmable timers, and an 8-bit parallel port.

A second μP (68008) forms the basis of the disk controller. The integrated Winchester and floppy-disk controller mixes or matches as many as three ST506, ESDI, or ST412HP Winchester disk drives as well as four 5¼-in. floppy-disk drives. The high-level, task-oriented command-structure implementation performs DMA transfers by cycle interleaving with CPU memory cycles. The controller supports variable sector sizes ranging from 128 to 1024 bytes. Selectable on a per-port basis, the controller also offers 32-bit error checking and correction for 11-bit correction or a cyclic redundancy check.



The 68010-based VME system foundation, *Model VSF 1605, includes disk and I/O interfaces, memory with a memory-management unit, and five expansion slots.*

The standard memory configuration includes 512k bytes of zero-wait-state dynamic RAM, which can be expanded to 2M bytes. Two EPROM sockets provide as much as 64k bytes of nonvolatile storage. The memory-management unit allows 32 or 64 task areas with as many as 4096 pages that are each generally 2048 bytes long. In addition, the single-level design provides a variety of protection and status mechanisms.

The Baseboard contains one parallel and eight serial ports. Each serial port allows you to program data rate, bit format, asynchronous or synchronous operation, and bit- or byte-level protocols. The ports include individual interrupt vectors for receive, transmit, error condition, and status change. The generic TTL interfaces allow asynchronous rates as high as 19.2k bps; each requires an optional adapter module with a choice of RS-232C, RS-422, RS-423, or current-loop interfaces.

The five VME expansion slots include logic for multiple bus masters and prioritized interrupts with the onboard CPU set as the highest priority. The slots accommodate single- and double-high VME-compatible modules. In addition, the 68008 μP used for disk control can access the VME-bus memory space, which allows memory block movements without CPU intervention.

Current software offerings are the Motorola Versabug PROM-based monitor and Unix version 5.2. Because firmware controls the disk interfaces, you can modify or add disk interfaces or functions. The VSF 1605 VME system foundation costs $5995.—***Maury Wright***

Interphase Corp, 2925 Merrell Rd, Dallas, TX 75229. Phone (214) 350-9000.

Circle No 740

ANALOG DEVICES

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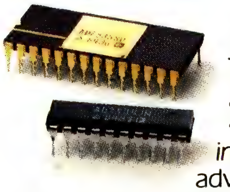

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They're the world's only 14-bit DACs that are guaranteed monotonic **over their full operating temperature range.** And thanks to an extremely tight gain error spec of just 4 LSBs, our DACs completely eliminate the need for trimming. Just plug them right into your instruments!

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What's more, the AD7534 does it all in one space-saving, 0.3″-wide, 20-pin DIP. It even incorporates µP-compatible logic on-chip for easy interfacing with an 8-bit data bus. And for designs where real estate is no problem, the 28-pin AD7535 provides faster loading speed via a 14-bit or wider bus.

Best of all, both DACs are available in quantity, off the shelf, in plastic or ceramic, today. And the price is so low that you can actually afford to upgrade your 12-bit designs to 14-bit resolution.

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CIRCLE NO 211

Solid-state electroluminescent flat-panel display is ¾ in. thick

Featuring the thinnest electroluminescent (EL) package available, the EL6648MX displays a total of 131,072 pixels. The use of custom ICs and surface-mount devices has reduced the thickness of this model by 50% compared with the earlier EL6648M.

The matrix comprises 256 rows and 512 columns. The monitor's pitch is 66.7 lines/in.; it displays 25 lines of 80 characters each. The complete package includes the EL panel, driver/control board, connector, and bezel and frame. This package's dimensions spec at $5.7 \times 10.3 \times 0.75$ in^3. The monitor weighs 16 oz. For a similar 9-in. diagonal (4×8 in.^{2}) display, a CRT consumes about 20 times as much volume.

Unlike liquid-crystal, plasma, or vacuum-fluorescent panels, EL displays use only solid-state technology, which enables the EL6648MX to withstand shocks of 100G on all axes. The EL panels aren't affected by electromagnetic fields and operate over 0 to 55°C; storage temperature ranges from −40 to +75°C.

The sturdiness of EL panels make them suitable for vehicular and aeronautical designs. Other applications include electronic test and measurement instruments, medical instrumentation, computer terminals, and process-control equipment.

The controller board converts signals from standard CRT controllers —such as vertical and horizontal sync, video data, and video clock— to the signals required by the EL panel. The display uses Texas Instruments drivers that operate from −160 to +190V, with a 45V modulation and a 60-Hz refresh rate.

Input voltages must be set at 12V. Power consumption specs at 15W. At 60 Hz, the panels emit about 25 fL of light.

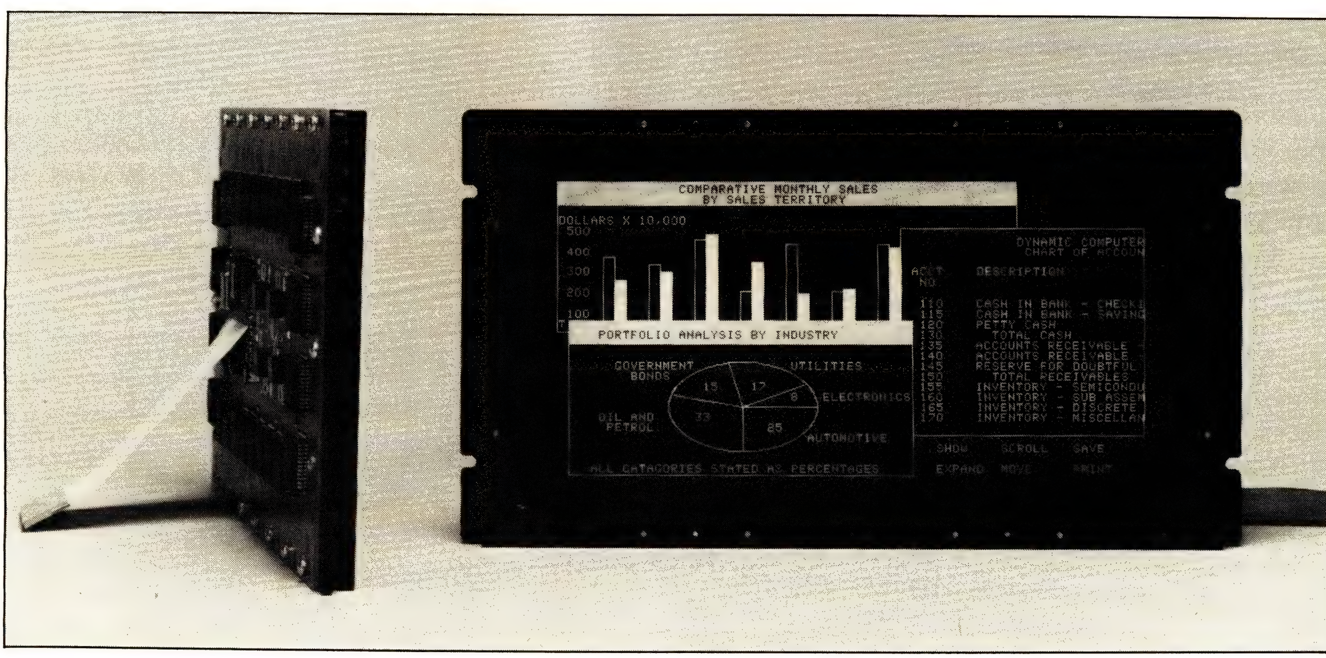
A circular polarizer increases the display's contrast. The evaporated zinc sulfide film, doped with manganese, emits a characteristic yellow-orange color, which is close to the amber now widely used in CRTs. You can view the display over angles of more than 120° with no flicker.

The EL6648MX requires one board to function. Because of the way the drivers are mounted on the controller board, failure of a driver doesn't destroy the entire monitor. The expected mean time between failures is 30,000 hrs—considerably longer than the typical 8000-hr MTBF of CRTs. $775 (1000).

—*Eva Freeman*

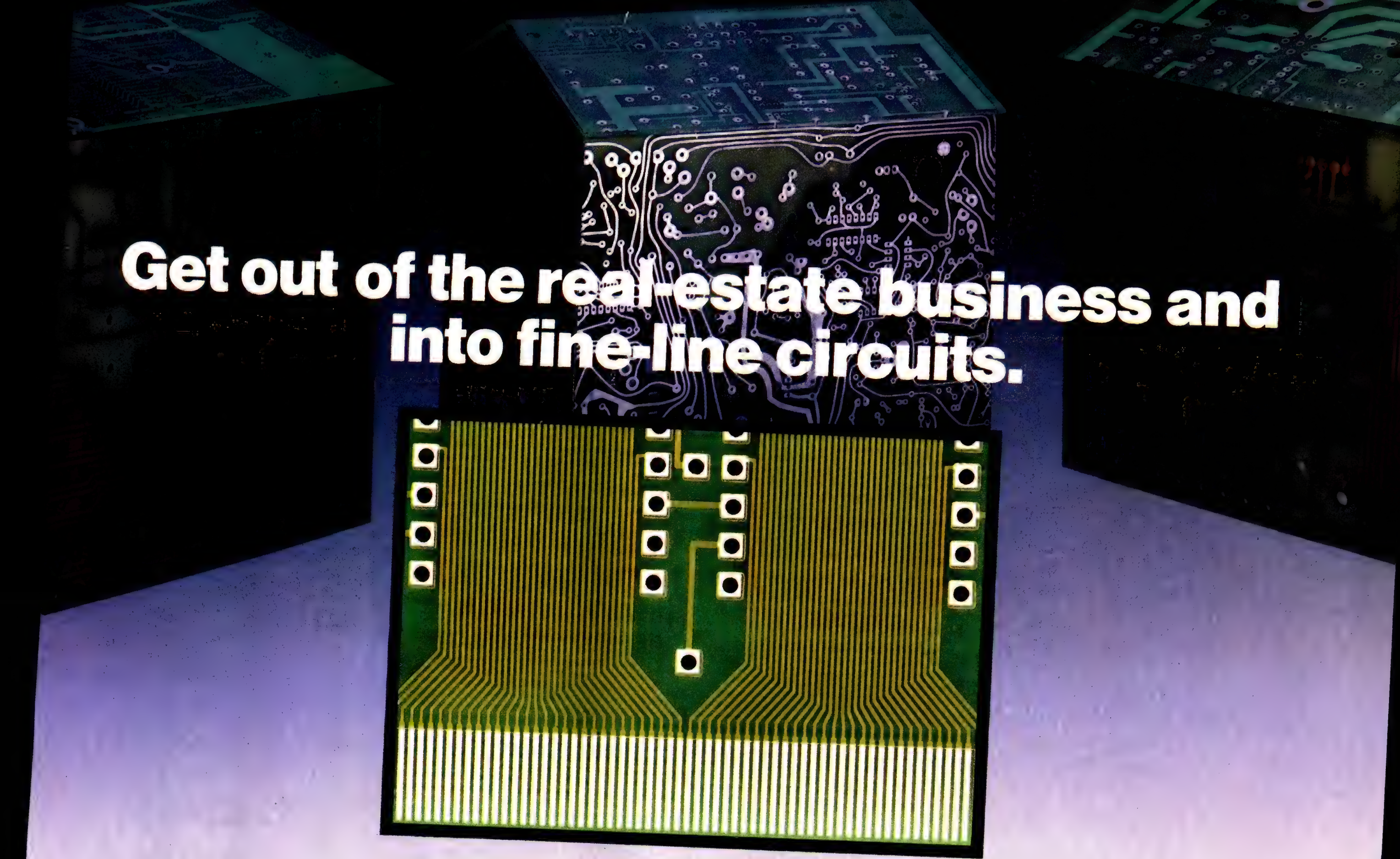
Planar Systems Inc, 1400 NW Compton Dr, Beaverton, OR 97006. Phone (503) 629-2006.

Circle No 743



The EL6648MX panel and controller board *together weigh 16 oz and measure ¾ in. thick.*

Get out of the real-estate business and into fine-line circuits.



Photocircuits' new Fine-Line Process meets the design engineer's need for high density circuits with increased performance in less real-estate. Circuits with 6-mil lines and spaces and 3 conductors through 100-mil centers are currently being produced. For a major computer company, we're delivering over 2,500 cards per week with 32 traces between 500-mil centers, as shown in the enlarged photo above.

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- *Superior electrical performance* for high speed controlled impedance circuits and minimized EMI, due to uniform and predictable fine-line conductor geometries.

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Color and B&W workstations fill high-end and low-end needs

Based on an MC68010 μP, the 2/160 Sunstation features a 19-in., 1152×900-pixel color display. For smaller applications, the 2/50 Sunstation offers workstation capabilities at a low price. Both systems work with the CAE software written for the Catalyst program.

Integrating high-resolution color graphics, the 2/160 general-purpose unit operates either in a LAN or as a stand-alone workstation.

The 2/160 has eight color planes that can simultaneously show 256 colors from a palette of over 16 million. The noninterlaced display specs a refresh rate of 66 Hz. In addition to panning in increments of one pixel, the display controller can zoom in one to 16 integer steps.

Designed with a 32-bit architecture, the MC68010 operates at 10 MHz with no wait states and can access as many as 16M bytes of virtual memory per process. The system comes in 1M-, 2M-, and 4M-byte configurations. Unix 4.2BSD is the standard operating system; Pascal, C, and FORTRAN come with the package.

The system operates either as a stand-alone workstation or in an Ethernet local-area network. The 2/160 includes a 12-slot card cage and a VME Bus. A Multibus-to-VME adapter board increases the system's versatility.

The 2/160 workstation accepts mass-storage options from 71M to 380M bytes of formatted capacity. Both ¼-in. streaming-cartridge and ½-in. start-stop tape drives are available for backup requirements. An optional hardware floating-point accelerator speeds computations.

The 2/160's display manager develops a range of user interfaces. The bit-mapped display can handle multiple windows, each displaying different icons and menus. A mouse offers an alternative to keyboard input.

The less-expensive 2/50 system also works under Unix 4.2BSD, so you can form an Ethernet LAN with the 2/50, the 2/160, and other related machines. Several diskless systems can share the disks of a 2/120 or 2/170 file server, thus lowering the cost per user. Generally, as many as 20 users can use the file server simultaneously without overloading the system.

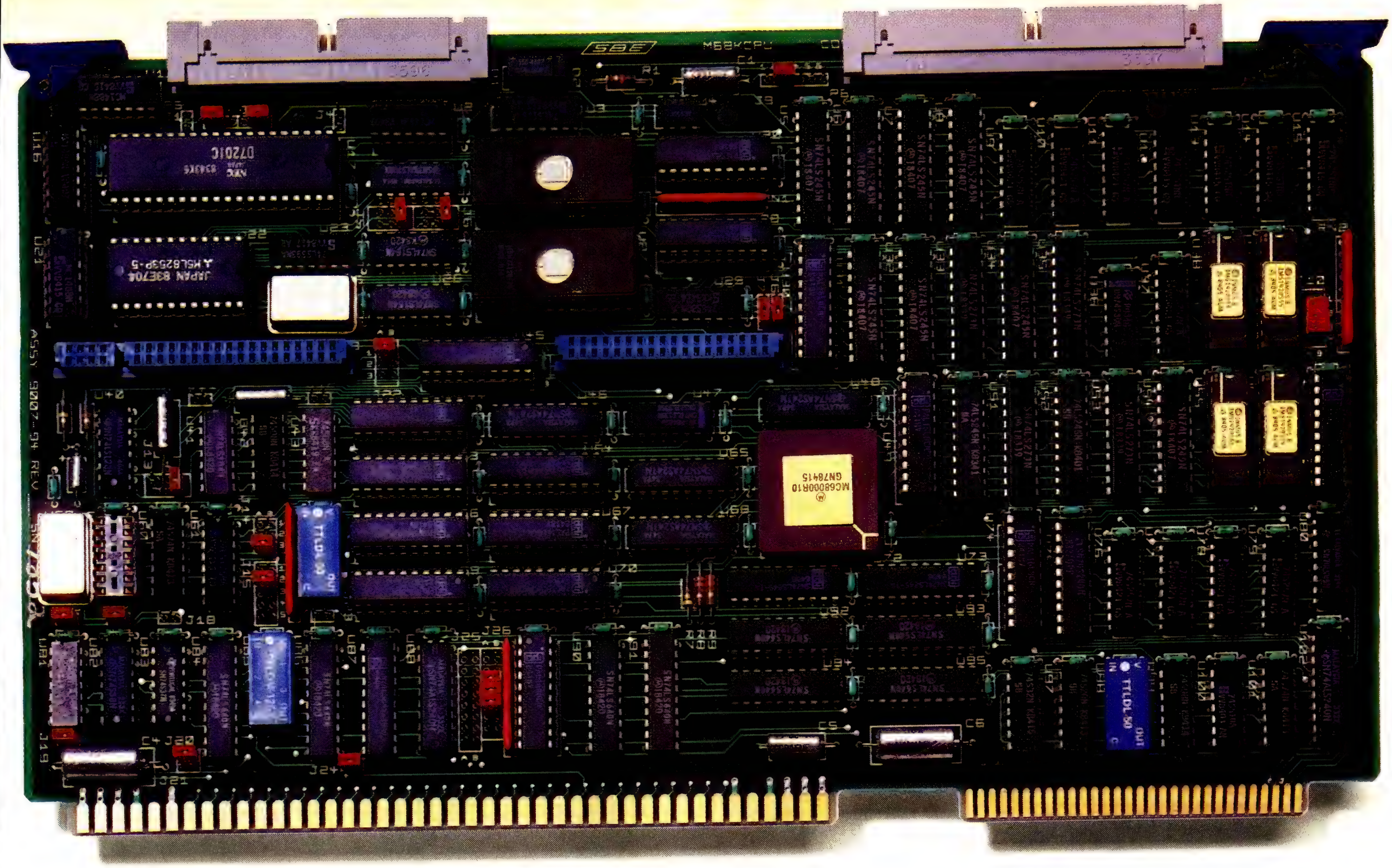
Like the 2/160, the 2/50 is based on a 32-bit architecture. The central μP is an MC68010 running at 10 MHz. The system features 16M bytes of virtual address space for each process. As with the 2/160, the standard 2/50 comes with a 1M-byte memory; you can optionally expand the memory to 4M bytes.

The 2/50 doesn't come with a card cage, however, and it has no facility for VME Bus or Multibus interfacing. Its noninterlaced, black-and-white display refreshes at 66 Hz. Bit-mapped graphics are displayed with a resolution of 1152×900 pixels. You can tilt and swivel the monitor.

With 1M-byte memories, the 2/160 costs $32,900; the 2/50 is priced at $9900.—***Eva Freeman***

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300.

Circle No 745



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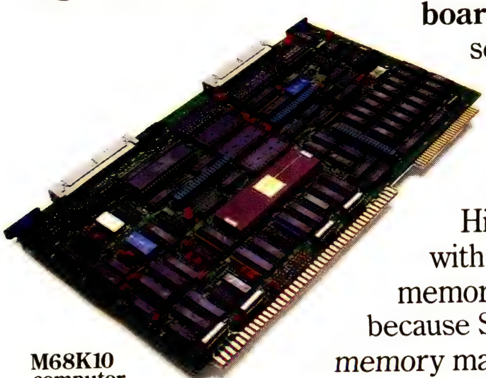

M68K10 computer

Our M68K10 runs at 10 MHz, accessing 128 KB to 1 MB RAM on the same board. This CPU is an amazingly powerful single-board computer for communications, process control, data analysis, ATE, and other systems applications. Contains up to 1 MB of dual-ported RAM accessible with no wait states. Has a 16-bit counter/timer and 24-bit parallel port right on board.

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Single-Euroboard-form board unites J11 CPU and G-64 bus

Providing the first single-Euroboard implementation of the J11-CPU chip set, the GESMPU-11 board mates the DEC processor with the G-64 bus. The processor features an on-chip memory-management unit that extends the G-64 physical-address space to 512k bytes. The board also includes a DEC-compatible serial interface and three 16-bit timers. Resident firmware provides you with microdiagnostics and an on-line debugger microprogram.

The G-64 bus offers an alternative to the STD bus and employs the single-Euroboard form factor with a DIN connector. Although it doesn't meet VME performance standards (eg, you can't achieve a 32-bit data path), the G-64 provides an economical alternative to VME. Approximately 15 European firms manufacture G-64 products, but the bus only recently hit the domestic market.

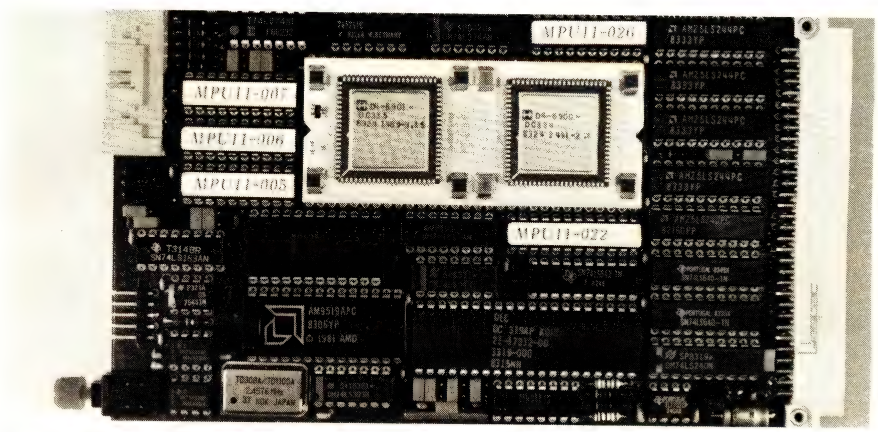
To complement the J11 hardware, the DEC facility in Munich agreed to port software for a G-64-based system. During the first quarter, offerings will include the RSX-11 operating system and Micropower Pascal. Once the operating system port is complete, application programs will easily make the DEC-to-Gespac transfer.

The 16/32-bit CPU operates at 15 MHz and in some applications exceeds PDP-11/70 performance levels. The board includes an interrupt controller capable of handling 10 interrupts. Six of the interrupts originate within the board, including one each from the three timers, two from DEC's DLART communications chip, and one from the 50/60-Hz selectable real-time clock. The final four interrupts connect directly to the G-64 bus. One of the four external interrupts can provide you with power-fail information.

The board supports serial communication from 300 to 38,400 baud. Two of the three timers operate from a 76.8-kHz clock while the remaining one employs a 50- or 60-Hz signal. Extensive use of PLAs allows the level of integration found on the GESMPU-11. The board costs $1750. The J11 chip set primarily drives the cost, so reductions will likely occur as the CPU drops in price.—***Maury Wright***

Gespac Inc, 550 E Grandview, Mesa, AZ 85203. Phone (602) 962-5559.

Circle No 741



Based on the J11 CPU chip set, *the GESMPU-11 single-Euroboard pc board brings DEC compatibility to the G-64-bus arena.*

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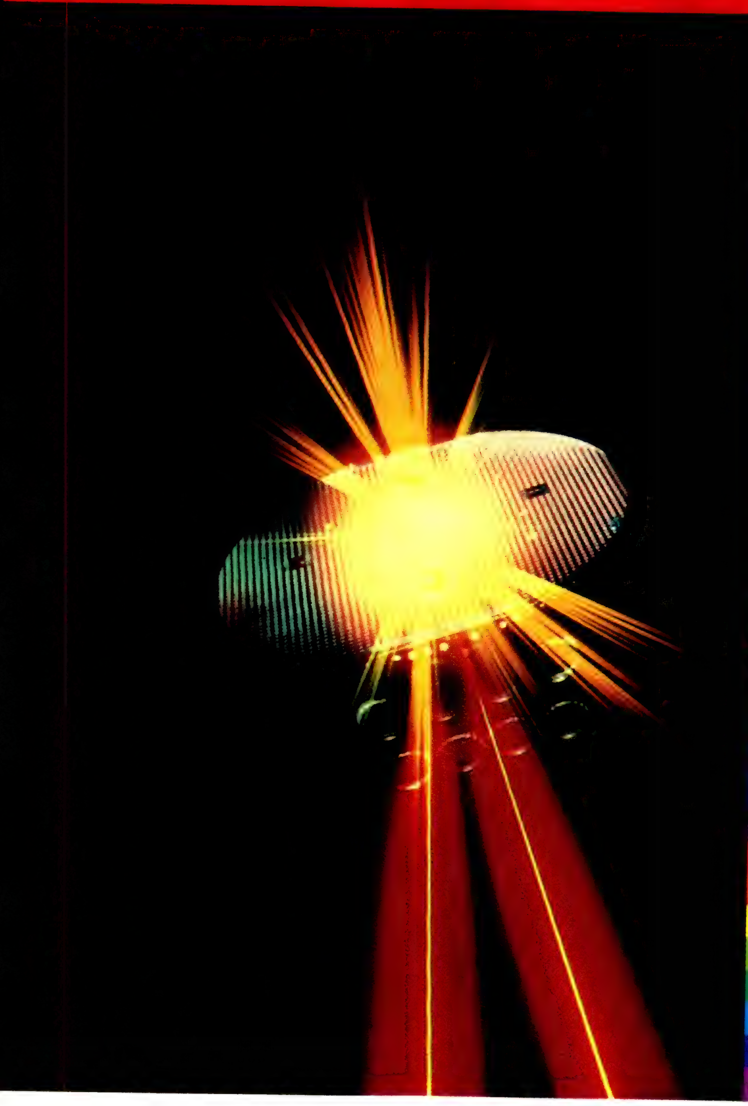

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HC/HCT10	Triple 3-Input NAND Gate
HCT20	Dual 4-Input NAND Gate
AND GATES	
HC/HCT08	Quad 2-Input AND Gate
HC/HCT11	Triple 3-Input AND Gate
INVERTERS/BUFFERS/BUS DRIVERS	
HC/HCT04	Hex Inverter
HC/HCT365*	Hex Buffer/Line Driver; 3-State
HC/HCT366*	Hex Buffer/Line Driver; 3-State; Inverting
HC/HCT367*	Hex Buffer/Line Driver; 3-State
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting
HC4049	Hex Inverting HIGH-to-LOW Level Shifter
HC4050	Hex HIGH-to-LOW Level Shifter
FLIP-FLOPS (POSITIVE-EDGE TRIGGERS)	
HC/HCT74	Dual D-Type Flip-Flop with Set and Reset
HCT173*	Quad D-Type Flip-Flop; 3-State
HC/HCT174	Hex D-Type Flip-Flop with Reset
HC/HCT175	Quad D-Type Flip-Flop with Reset
HC/HCT273	Octal D-Type Flip-Flop with Reset
HC/HCT374*	Octal D-Type Flip-Flop; 3-State
HC/HCT534*	Octal D-Type Flip-Flop; 3-State; Inverting
HCT564*	Octal D-Type Flip-Flop; 3-State; Inverting
LATCHES	
HC/HCT373*	Octal Transparent Latch; 3-State
HCT533*	Octal Transparent Latch; 3-State; Inverting
HC563*	Octal Transparent Latch; 3-State; Inverting
HC/HCT573*	Octal Transparent Latch; 3-State
SHIFT REGISTERS	
HC/HCT165	8-Bit Parallel-In/Serial-Out Shift Register
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HC/HCT161	4-Bit Binary Counter; Asynchronous Reset
HC/HCT162	BCD Decade Counter; Synchronous Reset
HC/HCT163	4-Bit Binary Counter; Synchronous Reset
COUNTERS	
HC/HCT4020	14-Stage Binary Ripple Counter
HC4024	7-Stage Binary Ripple Counter
HC/HCT4040	12-Stage Binary Ripple Counter
HC/HCT4518	Dual Synchronous BCD Counter
HC/HCT4520	Dual 4-Bit Synchronous Binary Counter
HC/HCT40102	8-Bit Synchronous BCD Down Counter
HC/HCT40103	8-Bit Binary Down Counter
MULTIPLEXERS	
HCT157	Quad 2-Input Multiplexer
HC/HCT158	Quad 2-Input Multiplexer; Inverting
HC/HCT251	8-Input Multiplexer; 3-State
HC/HCT257*	Quad 2-Input Multiplexer; 3-State
DECODERS	
HC/HCT138	3-to-8-Line Decoder/Demultiplexer; Inverting
HC/HCT139	Dual 2-to-4-Line Decoder/Demultiplexer
HC/HCT154	4-to-16-Line Decoder/Demultiplexer
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HC/HCT4514	4-to-16-Line Decoder/Demultiplexer with Input Latches
HC/HCT4515	4-to-16-Line Decoder/Demultiplexer with Input Latches
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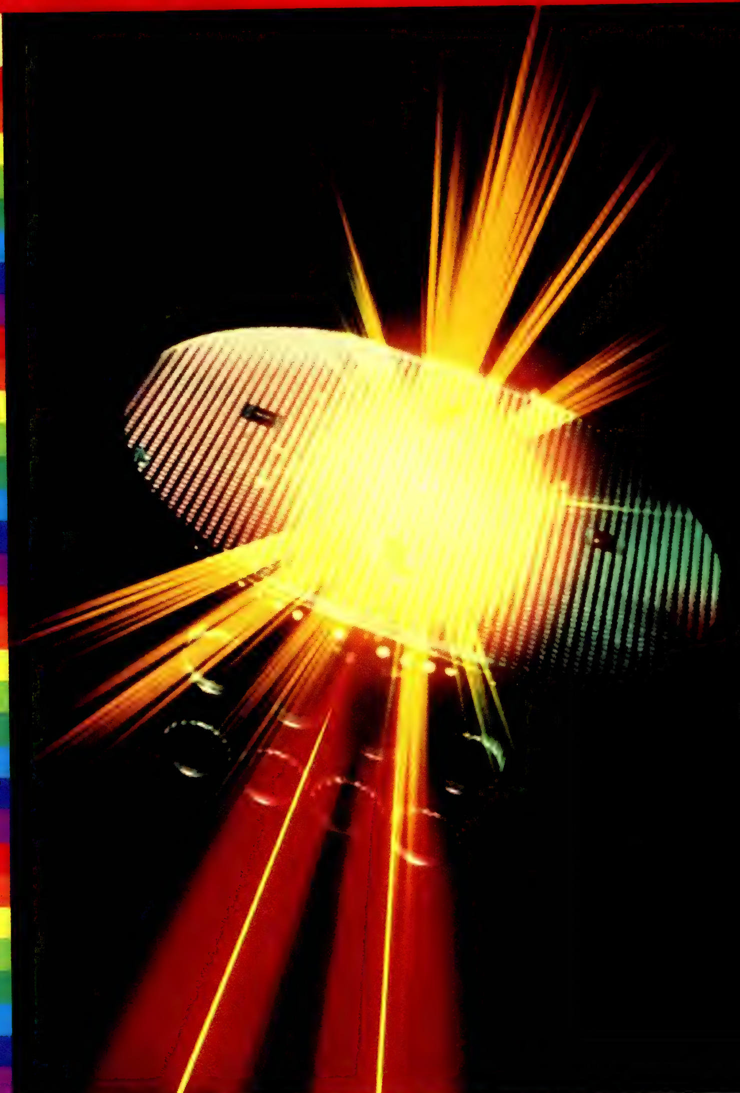

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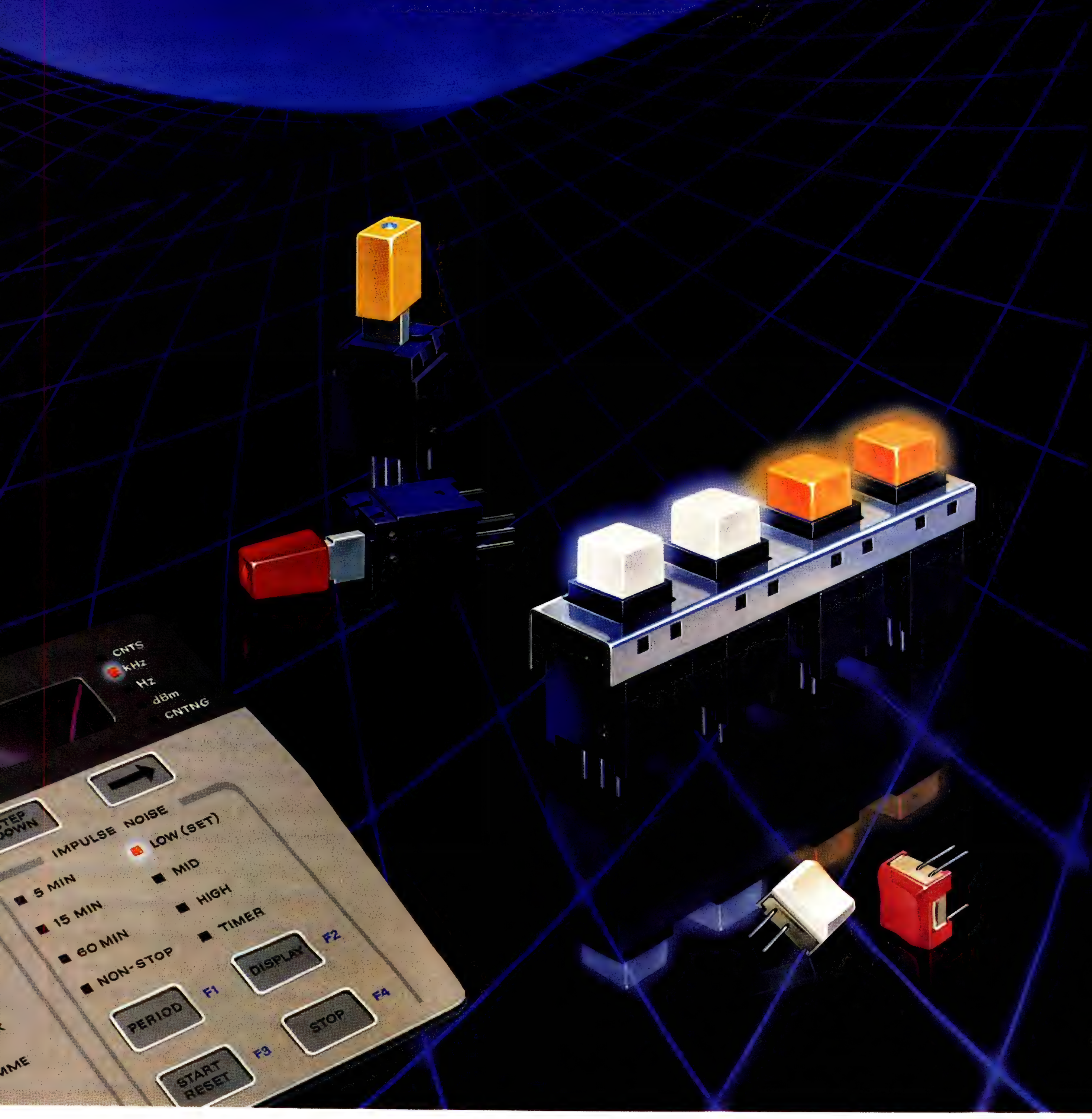

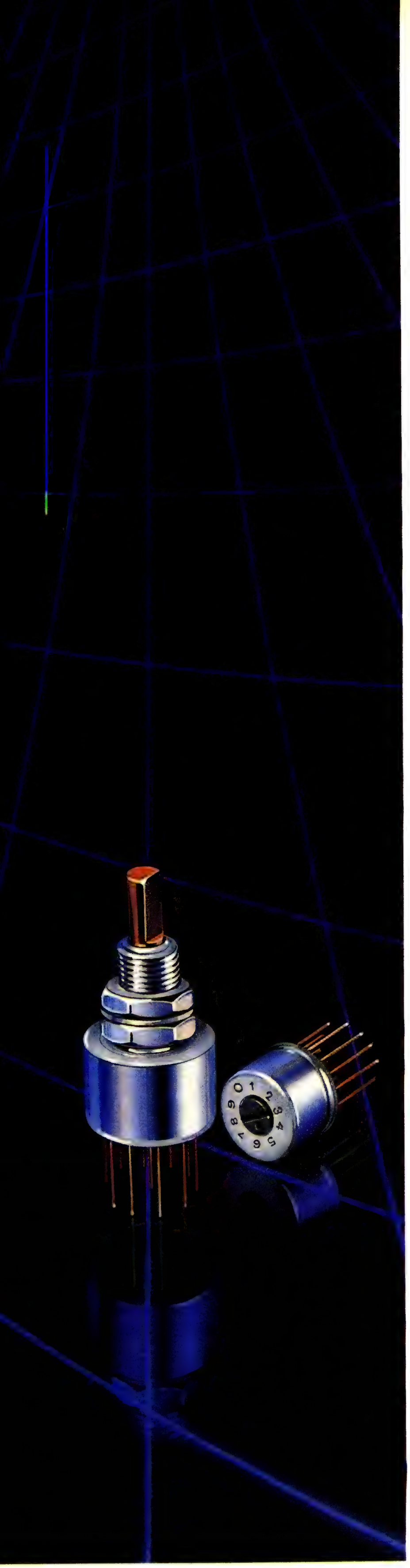

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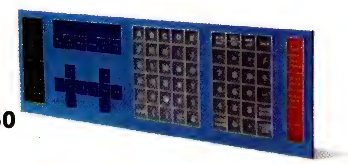

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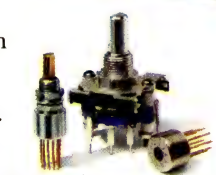

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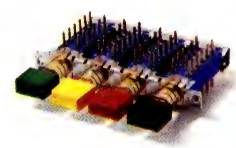

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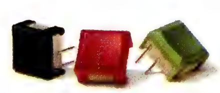

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Percent of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last months average (weeks)
TRANSFORMERS								
Toroidal	—	—	42	29	29	—	15.5	12.2
Pot-Core	—	—	50	—	50	—	17.0	15.8
Laminate (power)	30	20	50	—	—	—	4.4	13.1
CONNECTORS								
Military panel	—	—	17	17	66	—	21.2	16.1
Flat/Cable	18	29	41	6	6	—	6.4	7.2
Multi-pin circular	10	—	30	10	30	20	18.0	11.6
PC	9	27	53	—	11	—	7.6	9.3
RF/Coxial	—	—	80	20	—	—	9.6	10.8
Socket	8	50	25	17	—	—	5.7	5.4
Terminal blocks	—	60	30	10	—	—	5.2	7.4
Edge card	8	42	42	8	—	—	5.5	7.3
Subminiature	20	20	20	40	—	—	8.4	8.3
Rack & panel	—	17	66	17	—	—	8.3	9.6
Power	—	20	80	—	—	—	6.8	11.2
PRINTED CIRCUIT BOARDS								
Single sided	6	27	55	6	6	—	7.5	8.6
Double sided	—	19	69	6	6	—	8.4	8.5
Multi-layer	—	14	72	14	—	—	8.3	13.4
Prototype	9	73	18	—	—	—	2.9	6.1
RESISTORS								
Carbon film	29	35	24	12	—	—	4.5	4.8
Carbon composition	13	24	50	13	—	—	6.6	7.9
Metal film	14	33	33	20	—	—	6.5	6.2
Metal oxide	—	60	40	—	—	—	4.4	7.0
Wirewound	8	23	38	31	—	—	8.5	9.3
Potentiometers	20	27	33	20	—	—	6.4	7.3
Networks	23	—	46	31	—	—	8.6	10.6
FUSES	29	29	42	—	—	—	3.9	2.8
SWITCHES								
Pushbutton	11	23	66	—	—	—	5.7	6.8
Rotary	—	50	50	—	—	—	5.0	6.5
Rocker	—	60	40	—	—	—	4.4	7.4
Thumbwheel	—	25	62	13	—	—	7.5	11.0
Snap action	17	50	33	—	—	—	3.6	8.7
Momentary	—	50	50	—	—	—	5.0	8.0
Dual-in-line	13	50	37	—	—	—	4.0	6.3
WIRE AND CABLE								
Coaxial	10	40	40	10	—	—	5.6	6.1
Flat ribbon	27	46	27	—	—	—	3.1	5.0
Multiconductor	8	34	42	8	8	—	7.4	8.3
Hookup	46	38	16	—	—	—	2.0	3.6
Wirewrap	23	54	23	—	—	—	2.9	5.8
Power cords	34	34	24	8	—	—	3.9	5.9
Other	20	60	20	—	—	—	2.8	12.0
POWER SUPPLIES	—	34	24	34	8	—	10.1	11.8
CIRCUIT BREAKERS	—	40	30	30	—	—	8.0	10.4
HEAT SINKS	17	25	41	17	—	—	6.5	6.1
RELAYS								
General purpose	7	20	53	20	—	—	7.8	7.1
PC board	8	15	46	31	—	—	8.9	9.3
Dry reed	—	17	49	17	17	—	11.4	9.6
Mercury	—	—	50	50	—	—	12.0	9.5
Solid state	—	50	10	30	10	—	9.2	10.2
DISCRETE SEMICONDUCTORS								
Diode	11	41	37	11	—	—	5.5	9.6
Rectifier	15	39	39	7	—	—	5.0	12.7
Thyristor	11	33	33	23	—	—	7.0	9.4
FET	—	29	57	14	—	—	7.4	11.4
Zeners	14	43	43	—	—	—	4.3	9.6
INTEGRATED CIRCUITS, DIGITAL								
CMOS	—	19	13	36	19	13	16.2	20.1
TTL	—	—	27	36	27	10	18.9	19.8
LS	—	—	10	45	27	18	21.0	18.7
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	—	10	30	30	30	—	15.2	17.7
OP amplifier	—	10	30	20	40	—	16.2	12.6
Voltage regulator	7	14	29	36	14	—	12.0	14.5
MEMORY CIRCUITS								
RAM 16K	—	29	29	14	28	—	12.4	17.5
RAM 64K	—	28	18	18	36	—	14.2	16.3
RAM 256K	—	—	40	40	20	—	14.8	16.5
ROM/PROM	—	12	25	50	13	—	13.6	13.3
EPROM	—	27	27	36	10	—	11.1	14.8
EEPROM	—	12	25	50	13	—	13.6	10.4
DISPLAYS								
Panel meters	—	17	50	33	—	—	9.6	7.6
Fluorescent	—	—	100	—	—	—	8.0	9.6
Incandescent	—	—	75	25	—	—	10.0	10.5
LED	9	18	46	18	9	—	9.3	11.8
Liquid crystal	9	9	45	28	9	—	10.6	11.8
MICROPROCESSOR ICs								
8-bit	—	7	15	23	32	23	20.5	15.4
16-bit	—	18	10	27	36	9	17.6	18.3
FUNCTION PACKAGES								
Amplifier	—	20	40	20	—	20	13.0	13.9
Converter, analog to digital	—	—	80	—	—	20	12.6	16.1
Converter, digital to analog	—	—	80	—	—	20	12.6	13.7
LINE FILTERS	—	22	45	22	11	—	10.4	11.3
CAPACITORS								
Ceramic	32	16	47	5	—	—	4.9	7.9
Ceramic monolithic	20	10	50	20	—	—	7.4	10.2
Ceramic disc	20	20	50	10	—	—	6.0	6.9
Film	22	22	44	11	—	—	5.7	8.6
Electrolytic	23	31	23	23	—	—	6.1	9.0
Tantalum	29	21	29	21	—	—	6.1	8.3
INDUCTORS	—	18	64	9	9	—	9.3	14.6

Source: *Purchasing* magazine's electronic business survey

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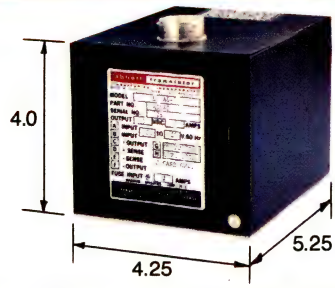

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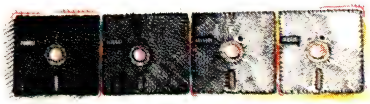

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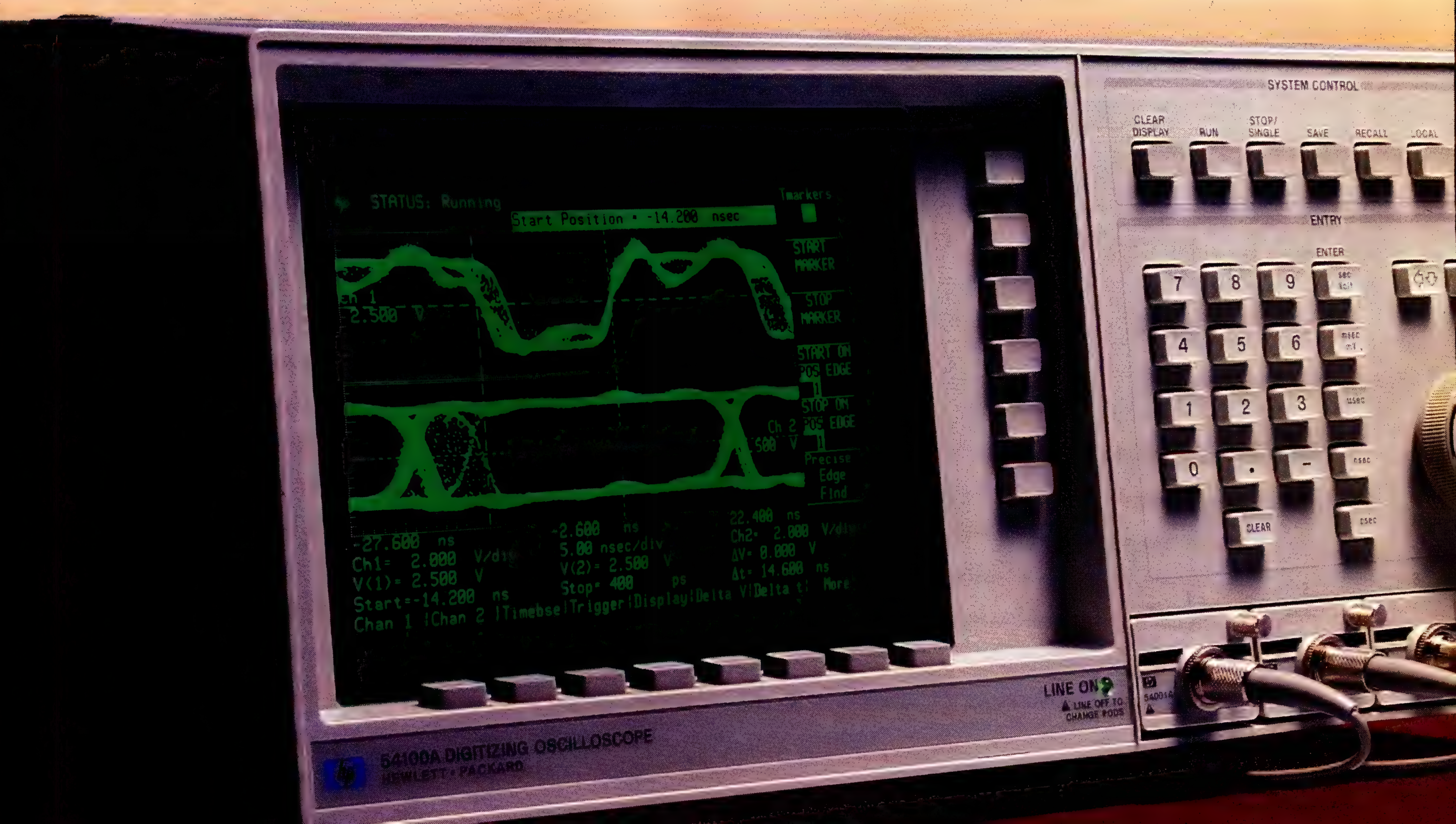

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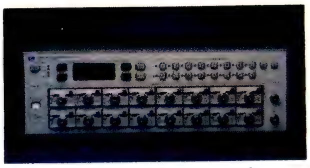

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Enhanced μPs bring new life to old devices

Updated μPs—enhanced versions of popular 8-bit devices—bear watching by OEM designers. These newer and more powerful μPs could extend the longevity of their mature predecessors.

Robert H Cushman, *Special Features Editor*

Numerous recently introduced or about-to-be-introduced updated μPs—enhanced versions of popular 8-bit devices—raise provocative questions for designers. Will these new 8-bit versions, which contain features generally associated only with 16-bit μPs, continue the impressive momentum of their popular forerunners? And will their extended capabilities let them compete with such 16-bit families as the 8086, Z8000, 68010, and 32016? If the answer to either question is yes, the new devices could extend the commercial lifetimes of their compatible predecessors.

Many enhanced versions of widely used μPs already exist (see **box,** "Enhanced μP updated versions," and **Ref 1**). Two devices scheduled for introduction in the near future are particularly noteworthy, however. The Z800 is Zilog's enhancement of the Z80; the 65SC816 is Western Design Center's enhancement of the 6502.

Neither of these enhanced devices should come as a surprise to OEM designers. Both have existed—at least on paper—for two or three years and perhaps longer. Now is a good time for a serious look at them, though, because they should be available soon. In fact, EDN has obtained a flawed preliminary 816 chip, which it's using for special projects, and WDC sources say perfect chips will exist by the time this article appears (see **Box,** "What does it take to design a μP?"). Zilog sources say the Z800 is well along in layout and expect to have prototypes by early spring.

What constitutes a μP's popularity?

Continuing popularity for the Z80 and the 6502 has encouraged the development of similar—but enhanced—devices. One measure of μP popularity is hardware sales volume. **Fig 1,** which illustrates market shares for several μPs, shows that the Z80 is steadily increasing its share (even though it's a 10-year-old design). According to Zilog, approximately 28 million units are sold annually, including units from alternate sources.

The 6502 has had some ups and downs in sales volume, because it has depended on a small number of computer-game and home-computer makers (Atari, Apple, and Commodore, for example) for its high-volume use. With the advent of new CMOS versions, however, the 6502 has broadened its user base to

It's only natural: Established μPs are hatching enhanced devices *that may survive for a season or thrive in an environment that readily adapts to the advanced features they bring. (Photo by Imagination; courtesy Zilog Corp)*


Z80

Enhanced 8-bit μPs contain features of typical 16-bit devices and may challenge them for many applications.

include low-volume industrial-controller applications. Consequently, despite setbacks in the computer-game market, like that experienced by Atari in 1983, sales of the 6502 still exceed 10 million units per year.

The popularity of a μP isn't measured solely by sales volume. More and more, popularity is tied to a device's software momentum—ie, to the development software that supports the μP—and the greatest contributor to this momentum is the software associated with popular personal computers that are based on the device. For the Z80, this is CP/M software; for the 6502, it's software for mass-produced home computers, particularly Apple II computers running the DOS operating system.

Even if your application is an embedded industrial controller and makes no use of CP/M or Apple-DOS software, don't underestimate the significance of this software: The momentum it creates for the Z80 and the 6502 assures your customers that these μPs will be available as spare parts for years to come.

User suggestions help define new chips

The mature Z80 and 6502, of which the Z800 and the 65SC816 are logical extensions, should therefore continue to be produced for a long time, particularly if the new updated versions become popular. To help ensure the success of these new versions, Zilog and WDC solicited comments and advice from leading users of the parent Z80 and 6502 devices. Even so, both companies say they later received complaints when they couldn't incorporate all of the suggested improvements.

Many complaints about the 816, such as the lack of

Enhanced μP updated versions

Enhanced versions of widely used μPs are abundant. EDN's latest annual μP/μC chip directory **(Ref 1)** lists numerous examples.

New forms of the Z80, for example, include the NEC 7800 family. Although most members of the family aren't code-compatible with the Z80, they boast an impressive array of enhancements, including as much as 8k bytes of on-chip ROM, 256 bytes of RAM, eight 8-bit A/D channels, and 16-bit multiply and divide instructions. One Z80 enhancement, National's CMOS NSC800, is code-compatible with the Z80, but it uses the Intel 8085 bus rather than the Zilog bus.

Updated versions of the 6502 include the Mitsubishi Series 740 family and the Zymos Zycomp-4, a pared-down 4-bit 6502 that's used as a core μP in semicustom applications. Single-chip CMOS and NMOS versions—mostly designed by Western Design Center but made by Rockwell, NCR, and GTE—also exist. All these enhancements of the 6502 and the previously mentioned enhancements of the Z80 are much less extensive than those of the Z800 and 65SC816.

There are also many versions of the 8080 and the 6800, the grandparents of the Z800 and 65SC816, respectively. Intel developed its present 8086 family from the 8080, although not with strict architectural compatibility; it retained only as much of the 8080 flavor as was deemed necessary to move its 8080 customer base to the 8086. Intel has also created downward and upward enhancements of the 8086—the 8088, the 80186, and the 80286—and it's proceeding to the 32-bit 80386.

Meanwhile, one of the most intriguing enhancements of the 8086 is the new V Series from Japan's NEC. The numbering scheme for V Series models differs from 8086 family numbering, but NEC Electronics USA president Keiske Yawata indicates that the series directly attacks Intel's 8086 markets. An interesting conjecture is whether the V Series will be as formidable an opponent of the 8086 as Zilog's Z80 was of the 8080.

Enrichments of enhancements

Another μP maker, Motorola, has expanded its original 6800 (the inspiration for the 6502) into a diverse assortment of μPs and μCs. The μPs for multiple-chip applications, the 6802 and the 6809, have been moderately successful. The single-chip 6800s, the 6801 and the 6805, have been very successful—so much so that Hitachi, a second source for the devices, is enhancing them further. Hitachi's 6301 and 6305 have been a thorn in Motorola's side; Motorola little expected a licensed second source to create enhanced versions that compete for its customers.

Sarv Thakur, marketing man-

multiply and divide operations, resulted from the attempt to keep the chip size small and the architecture simple—factors that WDC's president and owner William D Mensch Jr felt had contributed to the 6502's success. Zilog designers, on the other hand, were more willing to let the Z80's die size grow; they reasoned that the increased die size, larger than that of Intel's 8080 μP, hadn't hindered the Z80 in its competition with the 8080. Federico Faggin, one of the designers of the Z80, once told EDN (in an interview conducted in the mid-1970s) that it was very important for the Z80 to outperform the 8080, perhaps because he knew it would later be competing with the fairly modest 8085, Intel's updated version of its 8080.

At the same time, Chuck Peddle, the leader of the 6502 design team, told EDN that his goal was to produce the smallest possible chip for the lowest introductory price. The company introduced the 6502 in 1975 at a price of $20, an extremely low price at that time.

As a result of these different philosophies, the Z800 and the 816 are very different devices. The NMOS Z800 has almost all the features any Z80 user could ever hope for, but its initial version will have a rather large die (well over 300×300 mils), despite Zilog's use of 2.5-μm geometry and the Z800's efficient layout. The 816, on the other hand, has some obvious deficiencies, but its initial, 3-μm version will occupy an area ($277\times162=44{,}874$ mils^2) less than half that expected for the Z800, even though the 816 is fabricated in CMOS.

Plans for both devices call for the usual 20% shrinkages, probably within the first year, and for redesigns with process design-rule scaling thereafter. The Z800

ager for μPs at Hitachi, emphasizes that there was nothing accidental about the company's introduction of the enhanced devices: "They represent a major thrust of our strategy. We have issued proprietary CMOS enhancements of every Motorola 680X-family NMOS part we are licensed to second source.

"Besides being in low-power CMOS and having microampere-level power-down modes, our enhancements incorporate other features," he says. "For example, our 6301Y0 version of the 6801 incorporates one of the largest on-chip program ROMs—16k bytes—of any 1-chip device. Our 63L05F1 version of the 6805 incorporates on-chip LCD drivers as well as an 8-bit A/D converter. Some instructions for bit manipulation and bit test are added. Also," he adds, " we have tried to make our CMOS devices faster than the NMOS predecessors, and we have achieved 2-MHz, 0.5-μsec minimum instruction cycle times."

The problem with such enhancements is that, when you add features like new instructions, your new device may no longer be compatible with its predecessor, causing potential users to shy away from it. As an indication of users' wariness, consider that many early Z80 applications used just the 8080 instructions in order to maintain at least software compatibility with the Intel device.

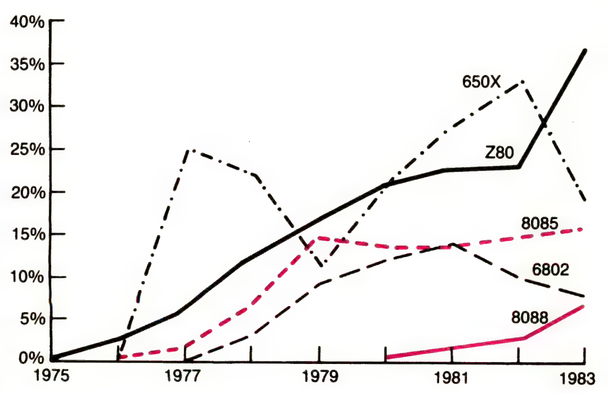
Once the enhancements themselves find a second source, however, the problem of compatibility becomes less significant. In fact, many enhancements approximate industry standards more than the original parts ever did (eg, the Z80 and the 6502). Still, there is no guarantee that such second sourcing will occur. That's the risk the user takes: A μP's enhancement may be intended to solve an immediate marketing problem, or it may result in an established, reliable device.

Currently, Hitachi is looking for a second source for its 630X devices, and the company expects to find one soon. Meanwhile, Motorola has countered with its new 68HC11, which the company says marks the beginning of a whole new family and not just a minor enhancement of existing parts (though it's based on object-code compatibility with the 10-year-old 6800). Hitachi's Thakur admits that the 68HC11 goes beyond any of the 630X enhancements, but he remarks, "It perhaps goes too far and overshoots the majority of market needs." EDN would not be surprised if some negotiations, directed toward resolving the conflicts between the 680X and the 630X devices, were now under way between Motorola and Hitachi.

A microprocessor's popularity relies in part on hardware sales volume and in part on software developments for computers based on the device.

should shrink to less than 300 mils on a side; the target is 280×280 mils. The 816's size should decrease to less than the equivalent of 200 mils on a side; the target is 224×133 mils. For the chips to reach their promised speeds—25 MHz for the Z800 and 15 to 20 MHz or more for the 816—additional shrinkages toward 1.5-μm geometries will be necessary.

As sizes decrease, so will prices. Although the Z800 will probably start in the $30 to $40 range, it will come down to the $10 to $20 range, according to a Zilog source. Similarly, though the 816 is starting out at $37.39 in quantities of 1000 ($22.26 for the 802 version, which addresses only 64k bytes of memory), it should come down to the $5 to $10 range as volumes increase. By comparison, current volume prices for the Z80 and the 6502 (NMOS) are $3 and $2, respectively. Typical prices for popular 16-bit μPs range from $15 to $25 in quantities of 100.



(SOURCE: DATAQUEST INC, AUGUST, 1984)

Fig 1—Market shares for 8-bit μPs tell much of the popularity story. *The Z80 has seen a steady rise in its share of 8-bit volume, and now it's the most popular. The 6502 has had its ups and downs, but there are still substantial volumes. Both processors have been more successful than their predecessors.*

So much for the background of these updated versions. Consider now the devices' features: Both are object-code compatible with their predecessors; you can configure the Z800 and the 816 to run operating systems and application programs developed for their respective predecessors. In fact, EDN has been experimenting with the 65SC802 version of the 816 in the 6502 socket of a Rockwell Aim single-board computer. The 816 itself isn't pin-compatible with the 6502, nor is the Z800 pin-compatible with the Z80. It may be possible to achieve plug-in compatibility with simple adapter cards.

Z800: A leap into the 16-bit world

The Z800 design represents an ambitious enhancement. As shown by plots of the Z800's expected performance **(Fig 2)**, Zilog is trying to catapult the Z800 into the 16-bit world. In some respects—especially when operating from cache—the Z800 may outperform

What does it take to design a μP?

μP design requirements can vary widely. Western Design Center says it took 1.2 man years to design and lay out the 65SC816 chip, and we estimate that it's taking Zilog 10 to 30 man years to complete the Z800.

WDC's president, William D Mensch Jr, says he and his sister Kathryn Mensch, WDC's layout manager, completed the 816 design in seven months in 1983. "We do it all with only four engineers," Mensch says of his 6-year-old, 20-person company, located in Mesa, AZ. "And only two of us, vice-president E Ray Hirt and myself, have had prior μP and IC design experience." (EDN first encountered Mensch and Hirt in 1975 when they were part of Chuck Peddle's design team for the 6502 at MOS Technology. All members of that team had previously been with Motorola on the original 6800 project.)

Mensch elaborates: "The secret of our rapid progress on the 816 and on the dozens of other chips—CMOS 6502s and associated support chips—is that we don't put any more manpower on a job than it needs. Then people don't get in each other's way. What you really need is one or two key people who know what they are doing and other people who are trained to carry out the details."

Lorenz Hittel, a long-term fan of the 6502, concurs: "Mensch's firm is a marvel of simplicity. It's also a bit of a family operation; his wife, Dolores, formerly an elementary school teacher, has conducted training classes that have turned people with no

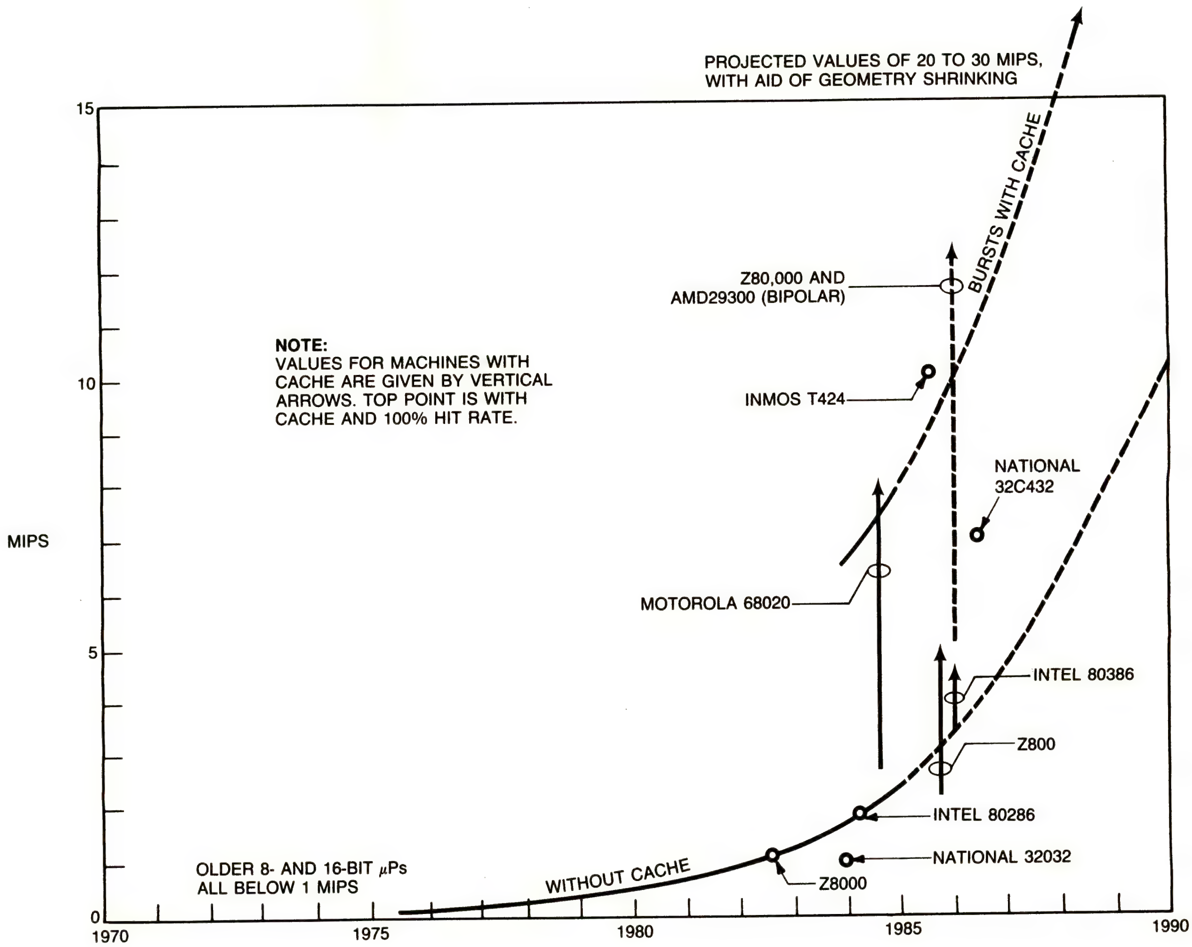


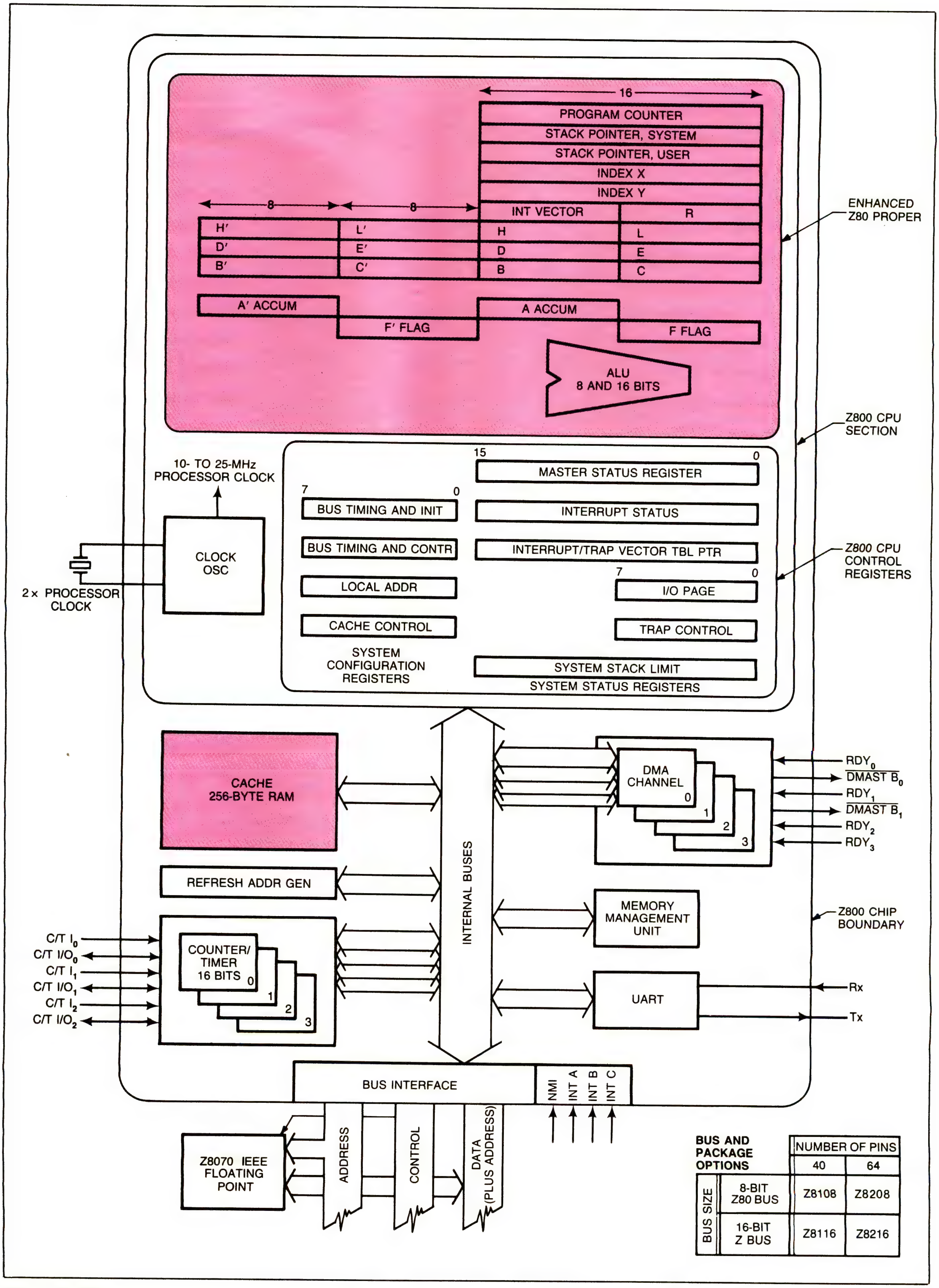
Fig 2—Vendors of 16- and 32-bit μPs characterize μP performance in MIPS *(millions of instructions per second). This graph plots various vendor's MIPS rates against introduction dates or estimates of arrival times for the first silicon implementation. All devices show basically the same performance on the MIPS-vs-time curve, except those with caches. You'll generally find that vendors who don't have devices in silicon are comparing their μPs with the oldest existing models from their competitors.*

previous experience into IC layout craftsmen." Hittel helped Chuck Peddle formulate some of the original 6502 specifications and has helped Mensch select features for the 816.

Zilog is sensitive about complaints that the Z800 will be 2½ years late at the promised mid-1985 availability date. A source at the company attributes the delay to an unrealistic original availability date set by the firm's marketing department.

Now, according to the source, the Z800 is on schedule and will meet its target of first silicon by early spring. Furthermore, the company says that the Z800 won't be delayed by three other chips that are under development: the 32-bit Z80,000, the Z8070 math coprocessor (which the Z800 can use), and the ZS8 "super" updated version of the Z80 1-chip device. Each project has a separate design team, so delays on one project won't affect other projects.

As for Mensch's claim of a 7-month turnaround time for the 816, Zilog's rebuttal is that that time was just for the design, which was then presumably sent out to neighboring GTE for a silicon-foundry rendition, while at Zilog, the design team has to do the whole job on a chip that's much more complex. Debugging the 816 has taken one year past the design completion. We hope it won't take Zilog that long, since it would put the actual availability of the Z800 into 1986.



		NUMBER OF PINS	
		40	64
BUS SIZE	8-BIT Z80 BUS	Z8108	Z8208
	16-BIT Z BUS	Z8116	Z8216

Fig 3—The Z800 has more than just an enhanced Z80 on its chip. *It has many of the support-chip functions commonly used with larger Z80 applications. Among these peripheral functions is a sophisticated on-chip cache. The enhanced Z80 at the top of the chip retains the familiar Z80 registers and adds a second stack pointer.*

Designers' philosophies differ: Some enhance their μPs by packing a multitude of features on chip. Others retain the simplicity of the original device's architecture.

Zilog's own Z8000, a 16-bit device that has earned a reputation as a fast real-time processor.

The Z800 is a pipelined CPU: It can fetch one instruction while executing another. A diagram of the chip layout (**Fig 3**) shows why the device is so capable. Note that an enhanced Z80 is only part of what's on the Z800 chip. There's also a 256-byte RAM that can be used either as a sophisticated cache or as part of regular memory space, a memory-management unit that can handle 16M bytes of external memory, four DMA channels that can disengage the CPU from the bus and control high-speed data transfers among peripherals and memory, four 16-bit counter/timers, and a UART serial port. There's also an address-refresh control unit with a 10-bit refresh counter; the Z80's counter has only seven bits.

On first examination of the enhancements to the Z80 CPU, the register set looks pretty familiar. It still consists of double banks of 8080-like registers that can be alternately selected for rapid context switching. The set also includes the index registers that were added in the Z80 enhancement of the 8080.

In addition, two other registers are available. Of lesser importance is the old R register, used on the Z80

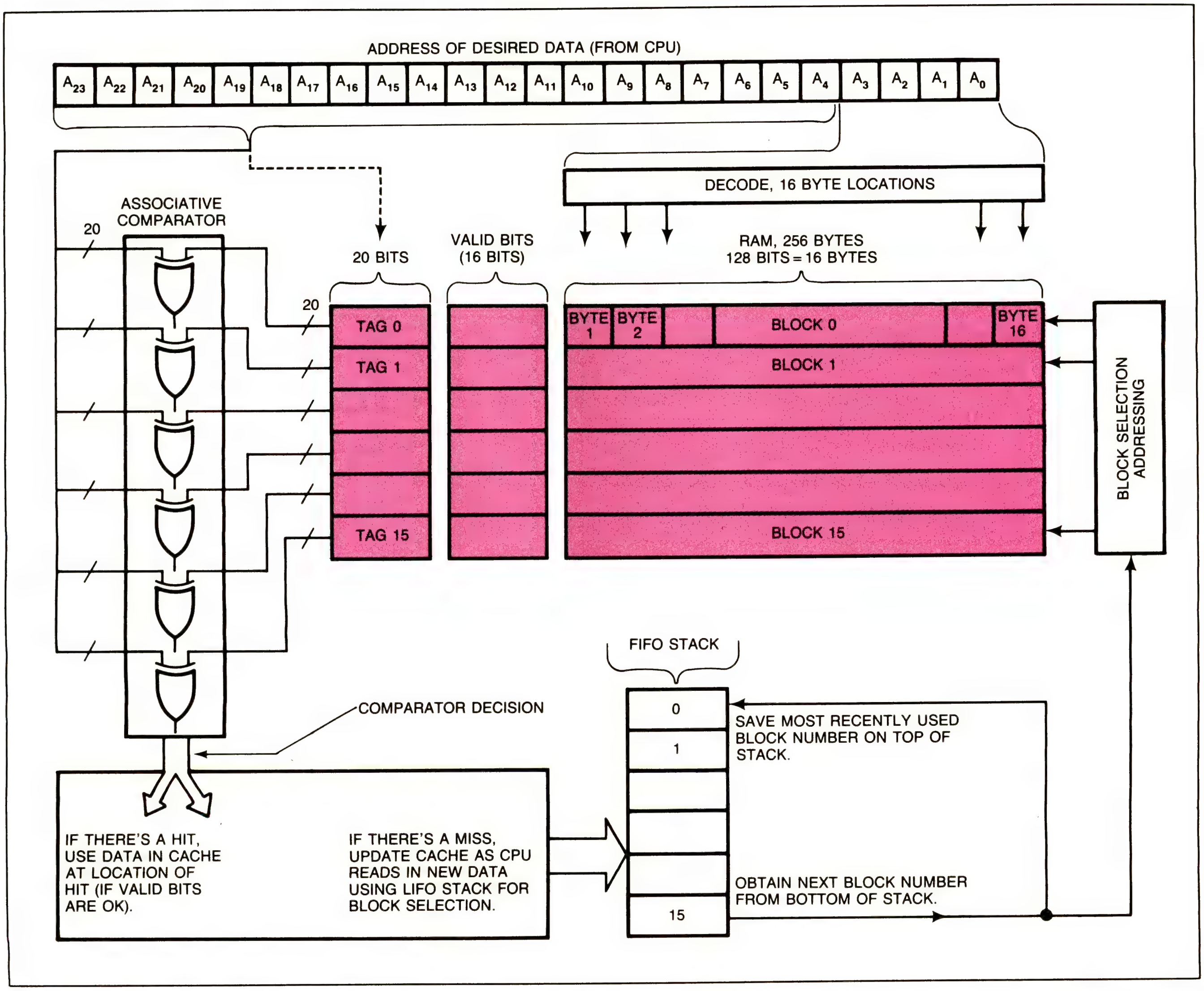


***Fig 4—The Z800 cache is essentially a 256-byte RAM** that can operate as a high-speed cache or as a RAM located (via software) in regular memory space. The cache is divided into 16 blocks of 16 bytes each, and each block has its own Tag and Valid bits, which are used to determine whether a desired data or instruction address is in the cache.*

as a memory-refresh counter. Because the Z800's refresh unit is separate from the CPU, this R register is available as a user-accessible register.

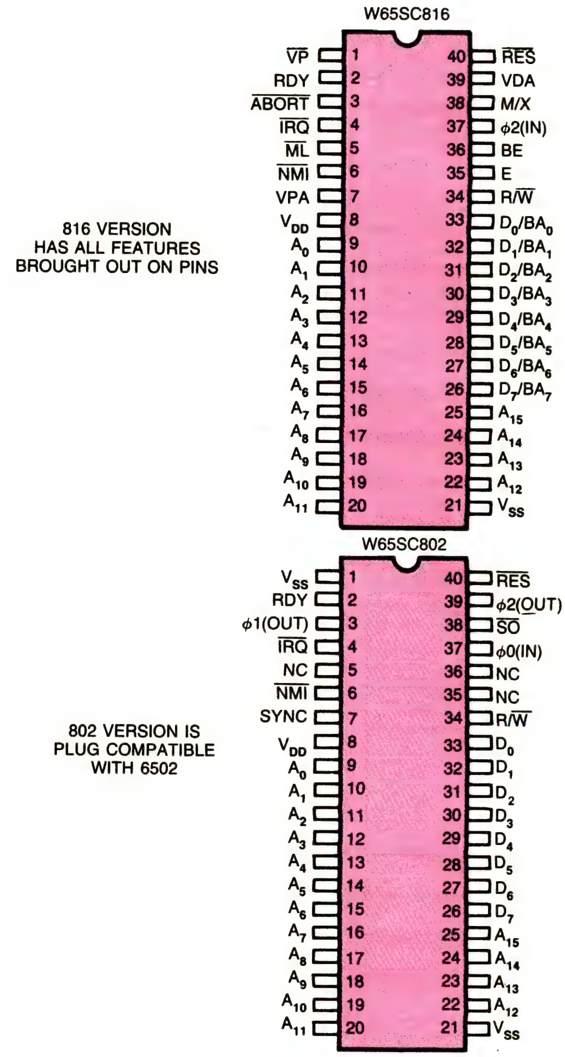
Of much greater importance is the Z800's additional 16-bit stack pointer. The presence of this register allows the Z800 to have a system-mode stack pointer and a separate user-mode stack pointer. Through this use of dual pointers, the Z800 provides a protected system level that can be made accessible only to the operating system. This facility allows OEMs to create multiuser computers more easily.

The controls that put the Z800 into system or user mode—and that also permit many other hardware and software configuration choices—are embodied in the bits of a new set of registers called CPU control registers. An operating system can access these registers upon power up when the Z800 is in the system mode. By manipulating bits in the registers, the operating system can set up the Z800 in several alternative ways before turning the system over to the user. From the variety of labels on these control registers and the number of bits they contain (most of which are allocated), you can see the extent of the choices for Z800 configurations. They go well beyond the choices on other 8-bit devices and are on a par with the features of some of the most advanced 32-bit μPs.

Caches epitomize sophistication

Cache memory and its control form the best example of large-computer sophistication in the Z800. The privileged Load Control instruction controls bits in the cache control register, and this gives you the option of selecting instructions, data, or both for fast access (ie, for true cache operation) or of merely using the cache as part of regular RAM. The cache itself **(Fig 4)** consists of a 256-byte static RAM divided into 16 blocks of 16 bytes each. Each block is associated with a Tag segment that contains the top 20 bits of the addresses of the data that is cached in the block.

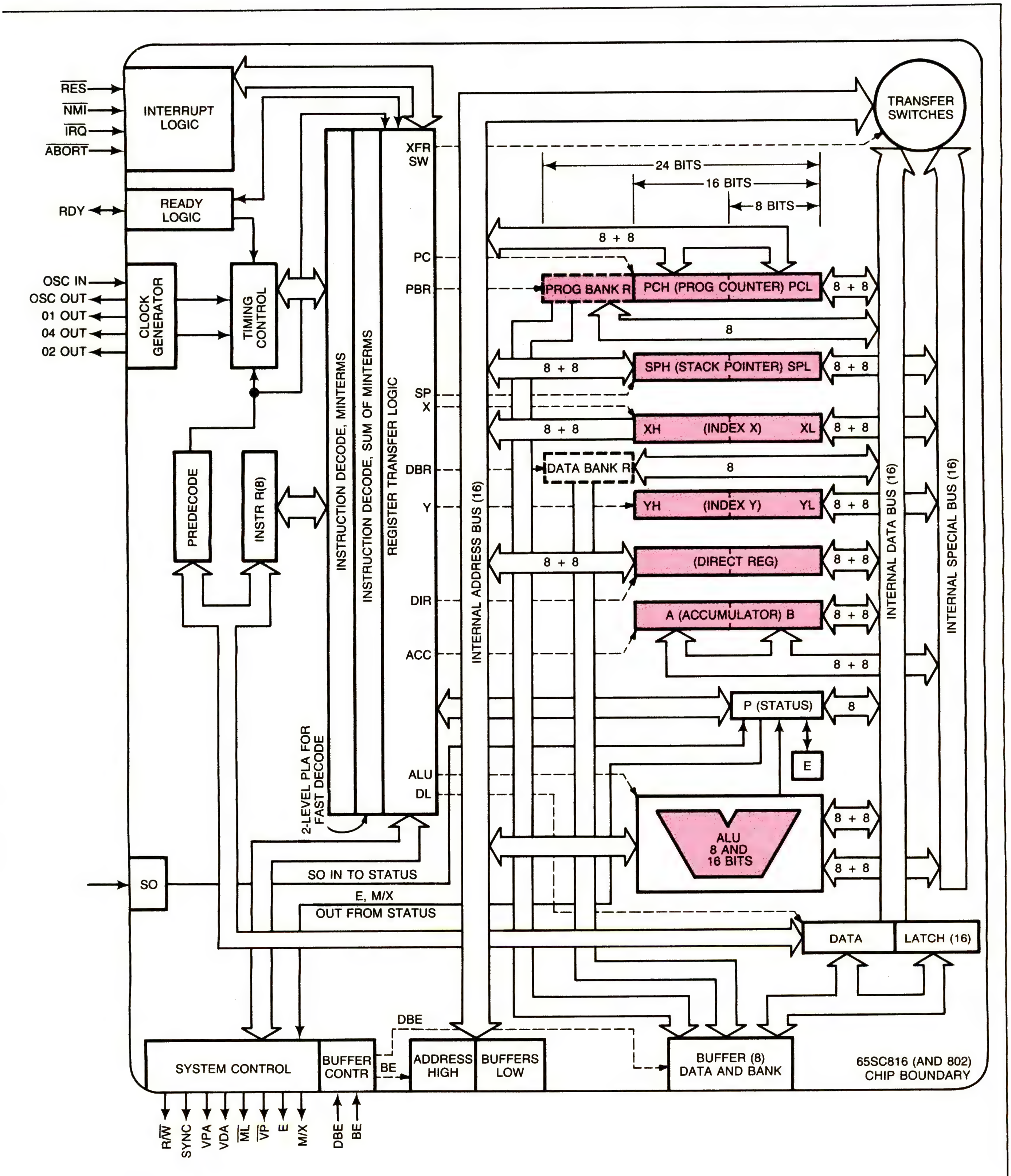
When the CPU begins a fetch cycle, it compares the top 20 address bits of the desired data with the address bits held in the Tags. All bits of all Tags are compared simultaneously with the corresponding address bits via



NOTES:
1. A SINGLE CHIP SERVES FOR 816 AND 802 VERSIONS. DIFFERENCE IS IN PACKAGE PINOUTS.
2. FOR OBJECT-CODE COMPATIBILITY WITH 6502, THE OP-CODE FIELD REMAINS EIGHT BITS. BECAUSE MOST OF THE 256 OP-CODE COMBINATIONS WERE USED IN THE 6502 AND 65SC02, FEW COMBINATIONS WERE LEFT FOR ENHANCEMENT. THEREFORE, ONLY MINIMAL INSTRUCTIONS COULD BE ADDED TO NEW HARDWARE FEATURES.
3. BANK REGISTERS ARE SHOWN IN DASHED LINES BECAUSE IN SOME CASES BANK-ADDRESS VALUES COME FROM OPERAND FIELDS OF THE INSTRUCTIONS. THE TWO INDEX REGISTERS SHARE ONE DATA-BANK REGISTER.
4. THE 816 HAS NEW OUTPUTS:
   - VECTOR PULL (VP)—INDICATES INTERRUPTS OR VECTORS ON BUS.
   - MEMORY LOCK (ML)—INDICATES NEED TO DEFER BUS ARBITRATION DURING READ-MODIFY-WRITE.
   - VALID PROGRAM ADDRESS (VPA) AND VALID DATA ADDRESS (VDA)—INDICATE μP'S USE OF EXTERNAL BUSES.
   - E AND M/X—STATUS BITS INDICATING INTERNAL MODE.
   - ABORT—ALLOWS YOU TO ABORT INSTRUCTIONS WITHOUT ALTERING CPU REGISTERS. VECTORS PROGRAM TO RETRY.
   - BUS ENABLE (BE)—TURNS BUS DRIVERS ON AND OFF.

Fig 5—The 65SC816 looks like the older Synertek 6516 "pseudo-16" that never got built. *In the 816, 8-bit bank registers extend the architecture to 24-bit addressing for handling a 16M-byte memory space. The 816 doesn't have the Z800's on-chip cache and memory-management unit on chip, but it provides controls so designers can implement these desirable functions externally.*

To invoke the power of large computers, some enhanced µPs are implementing caches for fast access to commonly used data and instructions.



Exclusive-OR Logic. Also, Valid bits are checked to see if the desired byte (specified by the lower four address bits, which are decoded into 16 bits) is valid.

If the desired data is found in the cache (a hit), it's immediately read into the CPU, and no external memory cycle is needed. If the desired data is not in the cache (a miss), then the CPU must go to external memory.

When data is read from external memory, it's also copied into the cache one or two bytes at a time. The cache block in which external data is stored is determined by a least recently used algorithm, which is implemented by the **Fig 4** FIFO stack, which stores data corresponding to each valid block. The number of the block with the oldest data appears at the bottom of the stack, and the external data is stored in that block; then the block's number is placed at the top of the stack to signify that it's the most recently updated block. If there is a Tag hit but a Valid-bit miss, new data will be located in the proper byte in the block.

The CPU can retrieve an instruction or data about three times more quickly from cache than from external memory. As μP speeds increase relative to the access times of economical RAMs, the value of a cache becomes more apparent. Allowing high performance with ordinary 100- to 150-nsec dynamic RAMs, the cache eliminates the need to use expensive bipolar RAMs with 50-nsec or less access times.

A cache is most valuable when a pipelined CPU like the Z800 is repeatedly executing a time-critical loop that's so small it can be completely contained in a cache. In this situation, a Z800 could achieve rates as high as 5 million instructions per second (MIPS) when running at its projected 25-MHz internal clock rate.

Constructing a high-performance cache isn't easy. Ideally, a cache's address Tag and Valid bits should be compared with the desired data address simultaneous-

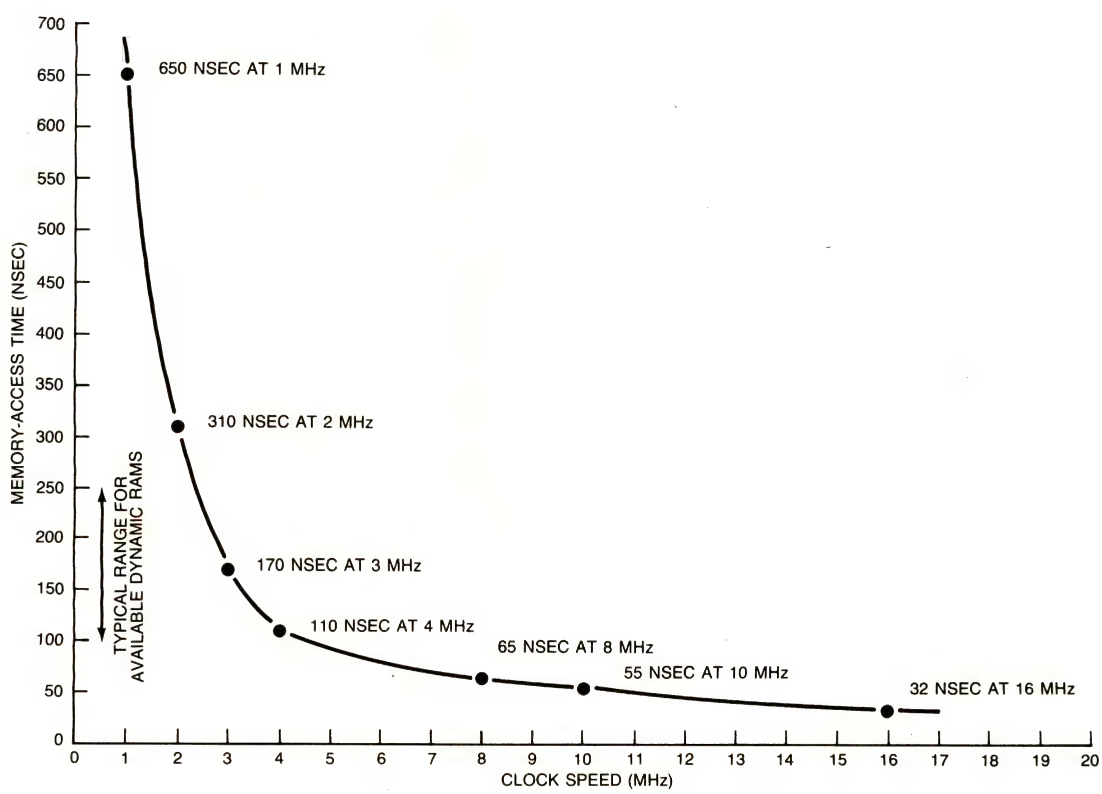


Fig 6—The problem of finding fast, reasonably priced memories *for enhanced μPs like the 65SC816 is becoming more severe, especially when one considers that users now are demanding large amounts of RAM, ROM, and I/O. Beyond 4 MHz the designer can no longer use moderately priced memories. At the 8- and 15-MHz clock speeds expected of future 816s, the system designer is forced to use increasingly expensive memories with 65-, 55-, and 35-nsec access times. This is why designers are now exploring schemes like cache and virtual memory.*

A small cache may not be adequate. A large cache may not be possible to realize in an enhanced 8-bit μP.

ly, and the contents of the cache should be updated efficiently. Some simpler cache implementations use an indexing comparison scheme, but Zilog implements an associative (content-addressable) comparison of the Tag and Valid bits. The implementation adds two transistors to each of the 6-transistor memory cells, so that an Exclusive-OR function is available at each cell. The Tag and Valid bits then can be compared to the bits of the desired memory address.

Zilog's competitors argue that a 256-byte cache isn't large enough to warrant such sophistication. David S Mothersole, the designer of the similar-sized, instruction-only cache in Motorola's 32-bit 68020, claims that his simpler scheme works just as well. Robert Freund, a National Semiconductor software expert who's studying caches for the next generation of 32000s, sees little value in small caches. Freund claims that, except for caches of 4k bytes or more (the size of caches used in mainframes), the hit rates are too low.

What **Fig 3**'s diagram doesn't show are all the new instructions and addressing modes for the Z80 and Z800 register sets. In the Z800, Zilog has made extensive use of the 16-bit registers formed by the HL, DE, and BC register pairs—registers that existed in earlier μPs but were never fully utilized.

In the early 8008 and 8080, an 8-bit accumulator-based architecture accomplished 64k-byte addressing from registers by using the HL, DE, and BC register pairs as 16-bit pointers. Arithmetic and logical operations were supposed to occur mostly in the 8-bit accumulator via the usual addressing schemes of accumulator-based machines. In the later Z, added index registers improved the addressing, and programmers began to use increasingly the 16-bit HL, DE, and BC pairs for limited arithmetic operations.

Now, in the Z800, most enhancements of the instruction set and addressing modes have been directed toward more use of register pairs for 16-bit arithmetic. Most notably, the pairs are used for 16×16-bit multiplication (as fast as 1 μsec at a 25-MHz bus rate) and for 32×16-bit division.

As a result, the Z800 architecture is a mixed bag. Half the operations (the more mundane) still involve just the old 8-bit accumulator of the original 8080 architecture. The remaining, more sophisticated operations use the 16-bit register pairs. Legions of programmers familiar with the 8080 and Z80 will probably love the Z800 because it will help them do what they've been struggling to do for many years, namely, perform 16-bit type operations. Other programmers, used to a more regular and consistent architecture like that of Zilog's Z8000, may find it undesirable. Compiler writers in particular might find it difficult to work with, but the large, guaranteed market created by Z80 software momentum may force programmers to work with the Z800 architecture at any rate.

65SC816: Elegance with gaps

The Z800 and the 65SC816 are impressive in the way their enhancements accentuate the different personalities of their predecessors. The Z80, with its three full 16-bit pointers and separate I/O space option, has always been a comprehensive, multifeatured device, but it makes extensive use of registers and an accumulator. The 6502, on the other hand, has always been an elegant device with a simple, classic architecture, but its omissions have restricted it to fewer applications.

It appears that the forthcoming Z800 will have an even greater split in its personality; users may wonder whether it's an accumulator- or register-based machine. The 65SC816 will retain the elegant architecture of its predecessor as it adds the enhancements, but it will still lack the Z800's comprehensiveness.

What is probably most important to the 816 is the degree to which its enhancements elevate the 6502 architecture into a form more suitable for high-level languages. Compiler writers have often said that the 6502 has one of the worst possible architectures for high-level languages. They point out that, although there are many interpreters for the 6502, there are few compilers.

The 816, however, is much better for high-level languages, says programmer Mike Westerfield of The Byte Works (Albuquerque, NM). Westerfield, who became interested in the 6502 after years of working on IBM and Cray mainframes, is the author of the 6502 ORCA/M macroassembler, which he has recently extended so that it can crossassemble 816 code.

As seen in the programmer's model for the 816 (**Fig 5**), most of the 6502's 8-bit registers have been lengthened to 16 bits in the 816. In addition, new bank registers have been appended to extend the program counter and index registers to 24 bits for full 16M-byte addressing. The registers have also been given additional addressing modes and instructions.

The bank registers that provide the upper eight bits of the new 24-bit addressing are awkward in some ways and hence impose one of the unavoidable penalties for upwardly compatible enhancement. The registers enforce a segmentation of the 16M-byte memory space

μP enhancements reflect the personalities of their predecessors in terms of features and architectures.

into 64k-byte banks, and although a new long addressing mode can make these bank boundaries transparent for data movements, there are restrictions on program branching.

The zero-page addressing mode (always the 6502's most valuable asset, because it made up for the 6502's lack of CPU registers by providing fast access to 256 memory positions) appears to be successfully enhanced in the 816. A new Direct register allows multiple zero pages to go anywhere in the first 64k bytes of memory. These pages allow rapid context switching, much as the work spaces in the Texas Instruments 9900 μP do but without, WDC claims, the 9900's notoriously slow operation.

Programmers like well-supported stack pointers

The 816 enhancement most often praised by programmers is the addition of new addressing modes for the stack pointer. Although there's still only one stack pointer (not two as in the Z800 and recent 16-bit machines), the 816 now has relative and relative-indirect-indexed modes. Programmers use these modes for efficient passing of parameters to and from subroutines. There is a software way of making it appear that the 816 has dual stack pointers.

The 816 also has a block-move instruction, as the Z80 has had all along. Ironically, some 6502 proponents who used to belittle the Z80's block move now enthusiastically laud the same instruction on the 816. They say it speeds operation of assemblers, compilers, and many application programs.

There appear to be two deficiencies in the 816, however: the lack of multiply and divide instructions and an external data bus that's only eight bits wide. The lack of multiply and divide instructions is something about which most of the first users of the 816 complain. With many competing μPs having these instructions, it's difficult to score well on number-crunching benchmarks without them.

Mensch counters the complaints by pointing out that the company had the foresight to include a coprocessor instruction and that it plans to develop a combined floating-point and integer math coprocessor chip (part number 864). The coprocessor might actually be integrated on the CPU chip. As for the 8-bit data bus coming off the chip (the internal bus is 16 bits wide), Mensch says that the 6502 architecture uses almost every machine cycle for memory access and thus compensates for the limitations. He adds, "We have a 4:1 bus-usage speed advantage over the competition—like the 8086 and 68000—and thus we can make our 8-bit bus work as fast as others can a 32-bit bus." Neverthe-

For more information . . .

For more information on the microprocessors described in this article, contact the following manufacturers directly, or circle the appropriate numbers on the Information Retrieval Service card. Also, keep in mind that there are second sources for many of these μPs. **Ref 1** provides information regarding those second sources.

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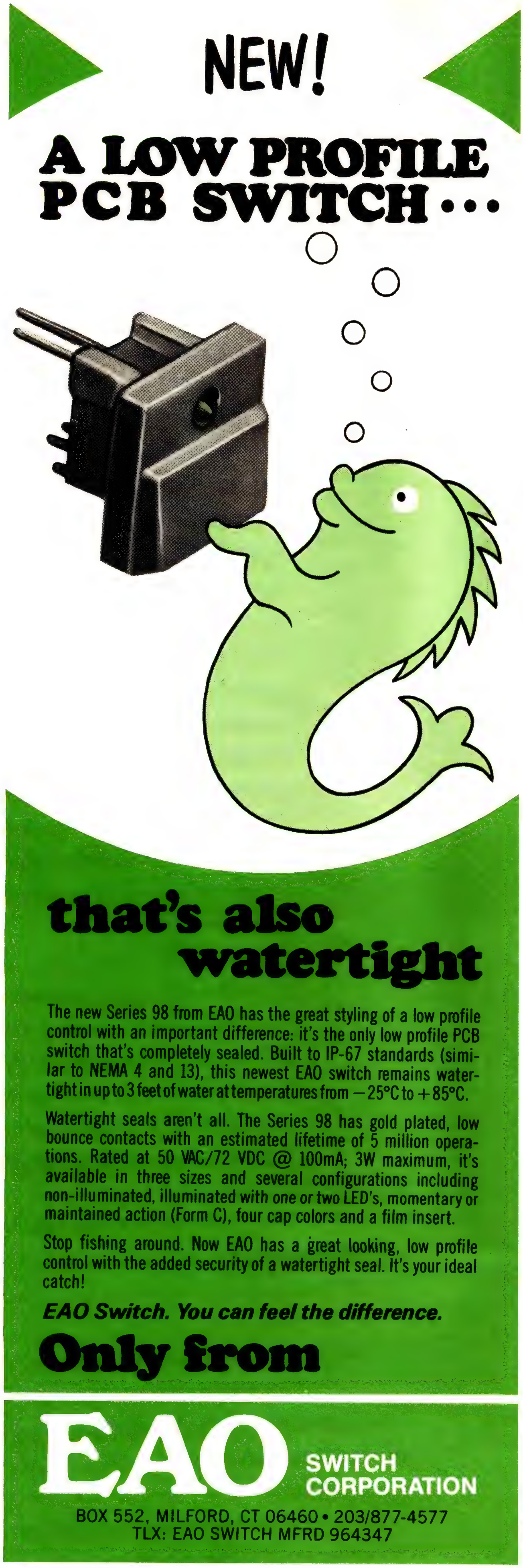

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New registers and instructions increase versatility. Beware of bus limitations and the lack of desirable functions, however.

less, some observers believe that the 6502 architecture's continuous bus usage might be a disadvantage, especially in applications that must accommodate DMA.

Controls provide system features

As noted, comparison of the Zilog and WDC devices reveals a sharp contrast between the Z800's comprehension with so many features implemented on chip and the 816's simplicity. The 816 does, however, provide controls that allow you to implement advanced system features externally. Although there are only four new control lines, WDC believes they are sufficient for implementing cache and virtual memories as well as for adding coprocessors.

For example, the 816's Abort input allows you to stop the 816 without altering internal registers and then vector the 816 to a memory location where a memory-repair routine begins. The Valid Program Address and Valid Data Address outputs round out the controls needed to implement cache and virtual memories. These signals occur early in the processor's machine cycle and thus can be used as advanced memory-enable signals to relax memory-access-time requirements, which have become difficult to fulfill at reasonable prices (**Fig 6**).

Finally, the Vector Pull output overcomes the 816's lack of interrupt vectoring. It indicates when the 816 puts a vector address on the bus, and it allows external modification or prioritizing of interrupts.

It remains to be seen whether these enhanced 8-bit μPs will find enough applications to establish them as reliable μP families. Success will depend on their compatibility with popular operating systems and, as noted, the development of software for computer systems that use the devices. **EDN**

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1. Cushman, Robert H, "EDN Eleventh Annual μP/μC Chip Directory," *EDN*, November 15, 1984, pg 164.
2. "Z800 Manual," unpublished manual from Zilog Corp, Campbell, CA.
3. *W65SC816 Advanced Information Data Sheet*, Western Design Center, Mesa, AZ, 1984.

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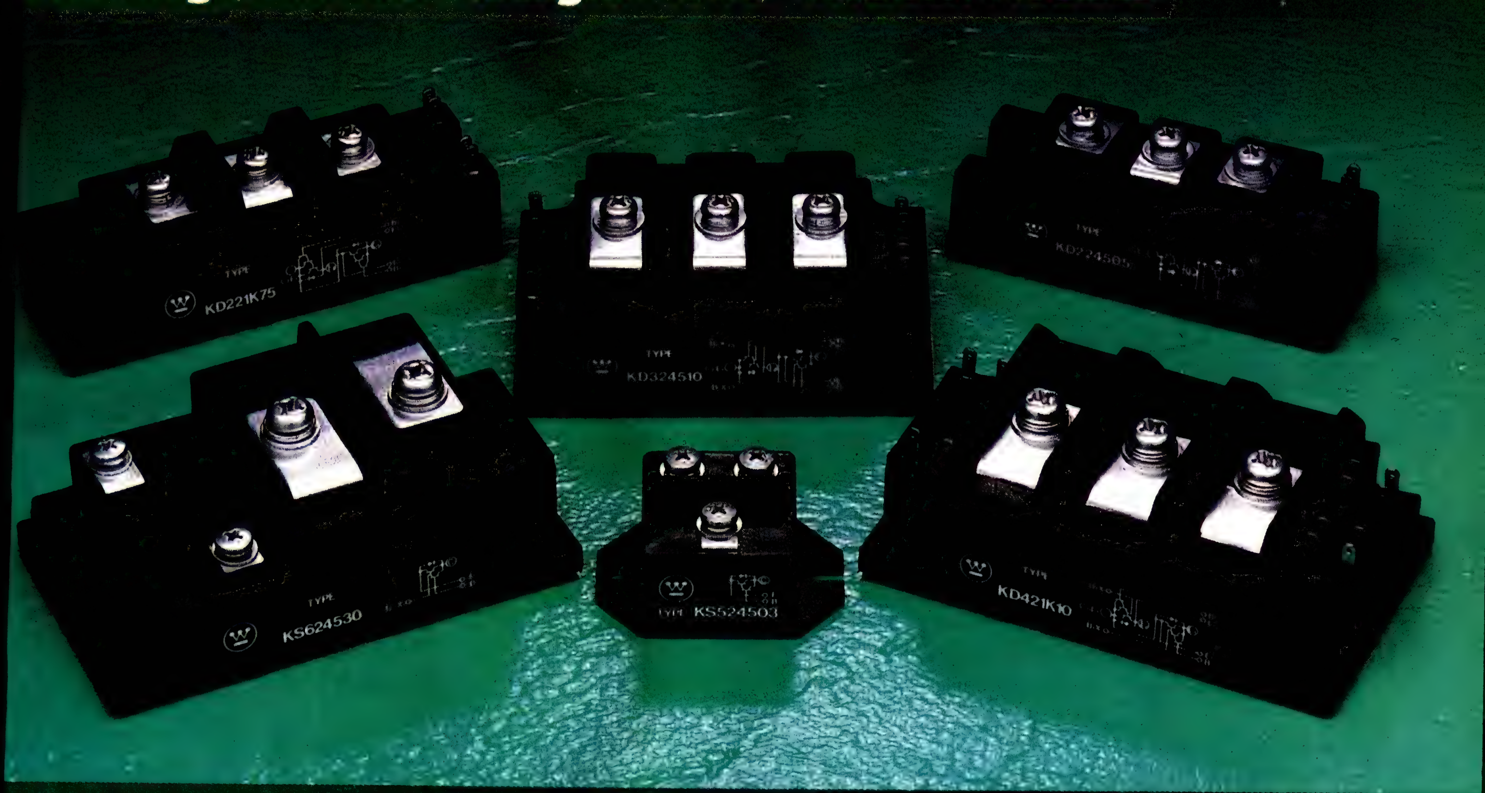

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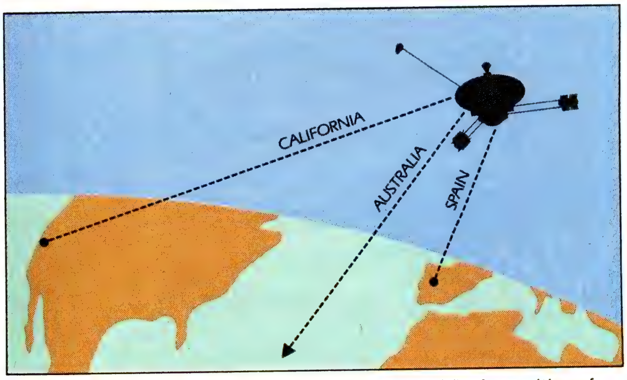

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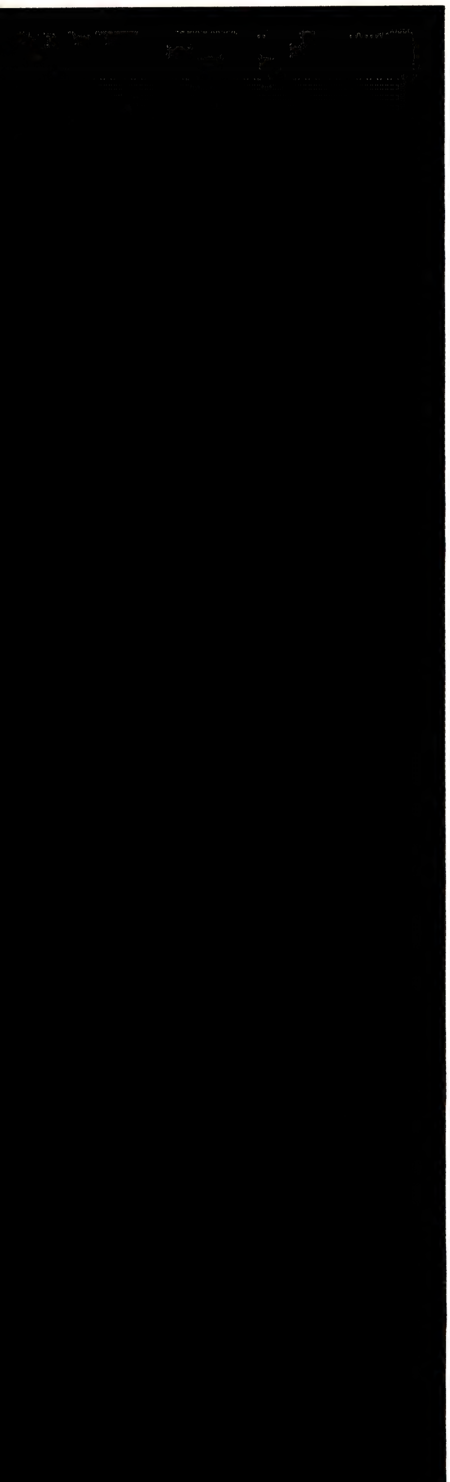

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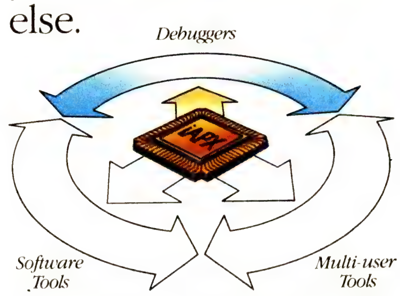

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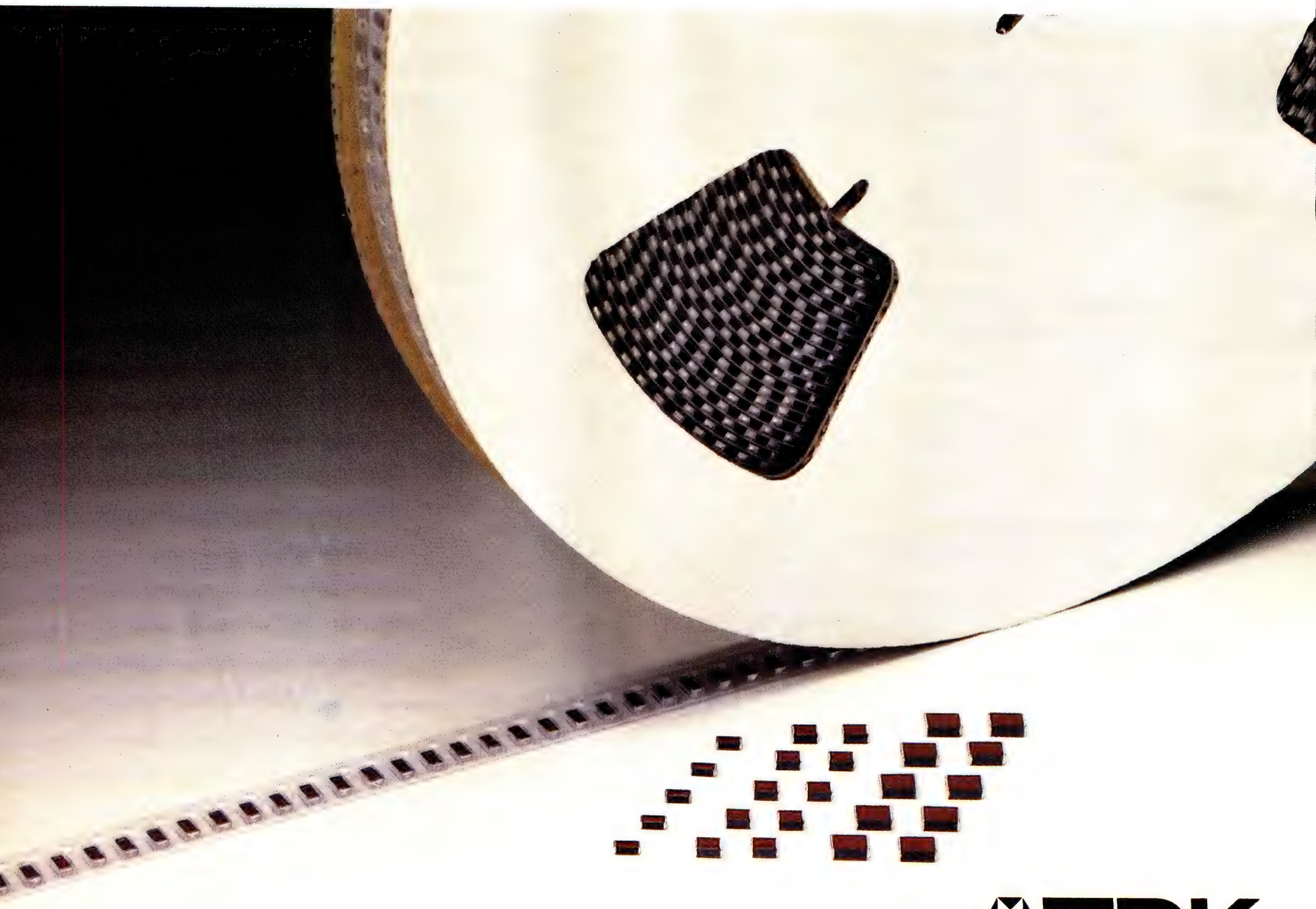

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Compiler-based software and PLDs improve logic design

Programmable logic devices allow you to complete a design faster than you can using SSI devices or custom ICs, and PLD implementations take up less space than do SSI-based circuits. Moreover, easy-to-use compiler-based languages that don't require you to understand PLD architectures make PLDs increasingly attractive for logic designs.

Bob Osann, *Assisted Technology*

Circuits that incorporate programmable logic devices (PLDs) take up less board space than do SSI-based implementations and require less design time than do custom-IC or SSI-based versions. But until recently, the PLDs' unusual architecture and lack of software support made designers hesitant to use the devices, despite the advantages they offer. Compiler-based software, however, is simplifying PLD use; this high-level software makes it unnecessary for you to be concerned with the PLDs' internal details when implementing logic functions with the devices.

This first article in this 3-part series, which is aimed at first-time PLD users, discusses basic PLD architecture and shows you how to replace two simple logic designs with PLDs using a compiler-based PLD design language. Part 2 will show you how to replace more complicated combinatorial and registered-TTL designs with PLDs. Part 3 will introduce the state-machine concept and show you how to implement a logic design directly, without ever developing a gate-level description of the system.

Although the PLD approach lets you go from logic function to PLD circuit without conceiving a gate-level description, when designers decide to use PLDs, they usually have either completed TTL designs that they want to shrink or else gate-level descriptions of circuits they don't want to implement in discrete logic. Therefore, the first two articles in this series target converting existing designs.

Why use a PLD?

For one-of-a-kind designs, prototypes, or small production runs, designers have traditionally taken the discrete approach. Discrete designs are easy to modify and inexpensive to manufacture in small quantities, and you can complete them more quickly than you can complete custom or semicustom designs. For production runs over 500, designers have typically chosen the semicustom and custom routes and sacrificed short design cycles and ease of modification to reduce manufacturing costs.

PLDs bridge the gap between bulky discrete designs and long custom-IC design cycles. On the one hand, PLD designs are easier to modify than SSI-based ones

A PLD approach allows designers to go from a logic function to a PLD-based circuit without conceiving a gate-level description.

and use much less space. Moreover, depending on the application, they can cost less than SSI-based implementations for even small production runs. And on the other hand, although custom ICs can prove more economical than PLDs for large production runs, PLD design cycles are much shorter. So, if you need to get a small, inexpensive design to market quickly and can't wait for a completed custom design, PLDs can provide you with a quick stand-in until your custom design is completed.

In general, the PLD architecture contains a fixed logic array made of AND gates—whose outputs feed OR gates—and a programming matrix. The programming matrix is made up of fuses that you blow with a programming device. By blowing the appropriate fuses, you can achieve any AND/OR product or combination. **Fig 1** shows the PAL-type and FPLA-type architectures. The total number of terms that you can generate is limited only by the size of the matrix.

Because you can represent any logical function as the logical sum of product terms, you can realize any logical function using a PLD. A product term consists of any combination of input variables or their complements ANDed together. A logical sum is any combination of

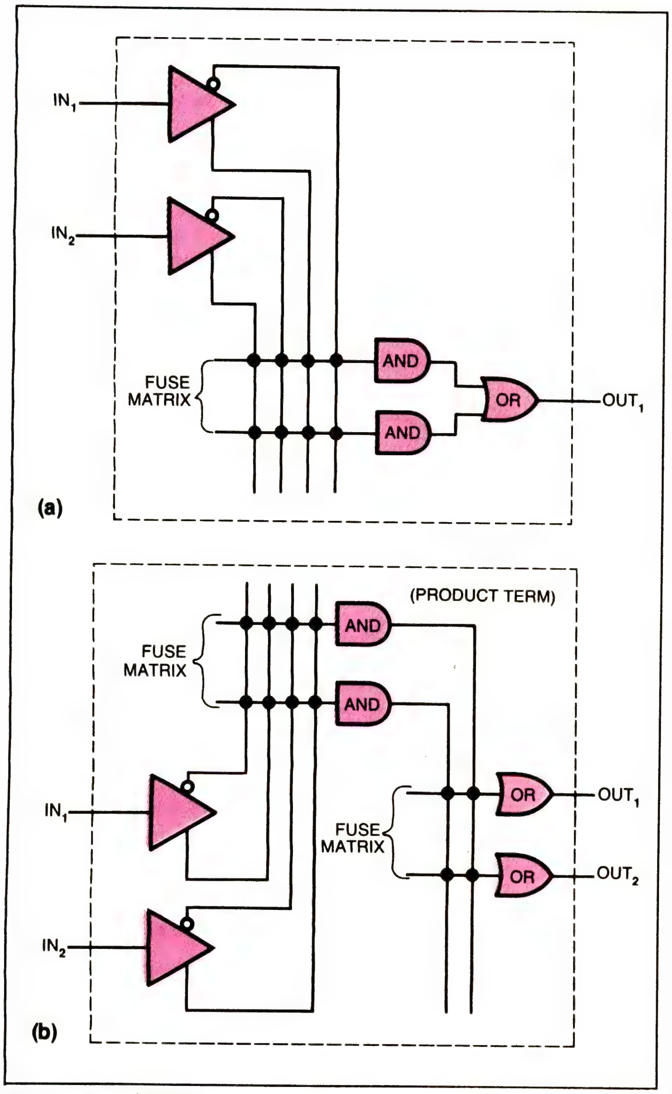

***Fig 1—Typical PLDs use one of two general architectures** to permit implementation of a wide range of logic functions. PAL-type devices **(a)** prove easier to use, but FPLAs **(b)** provide more flexibility by allowing two levels of programmability.*

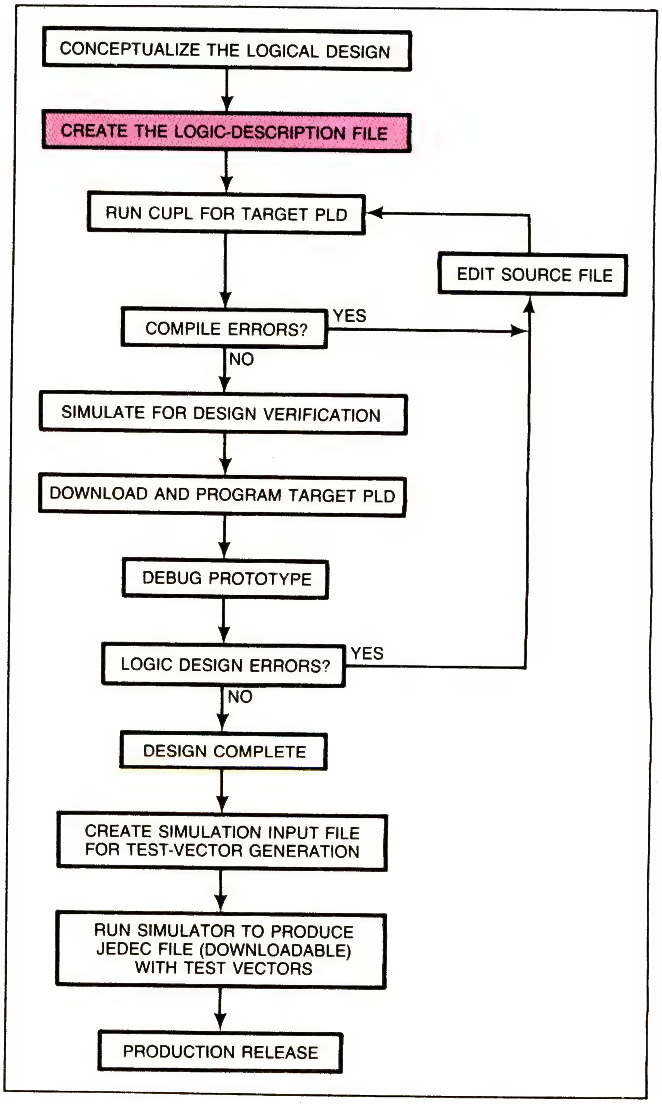

***Fig 2—PLDs greatly simplify logic design.** After you complete the logic-description file, the PLD software automatically compiles the data for downloading to a programming device.*

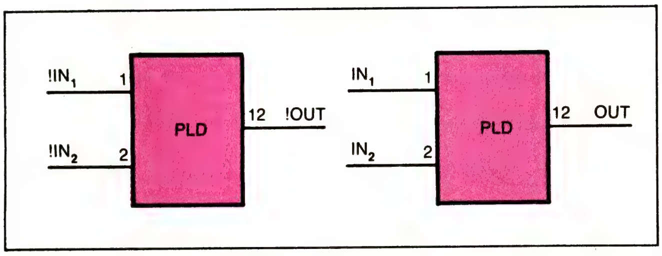

Fig 3—When using CUPL, you can always write your logic equations in positive logic, regardless of the actual polarity of the signals entering the device. For example, the two cases illustrated above both yield the same logic equation: $OUT=IN_1\&IN_2$.

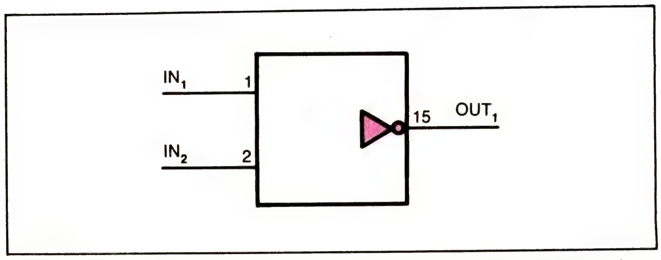

Fig 4—Some PLD devices use an inverting output buffer. *As a result, to accommodate applications that demand an active-high output signal, the compiler often must generate extra product terms that might make the design too big for the target PLD.*

product terms ORed together. Using De Morgan's theorems,

$$\overline{(AB)}=\overline{A}+\overline{B}\text{, and}$$

$$\overline{(A+B)}=\overline{A}\,\overline{B}.$$

Then, using the distributive property,

$$A(B+C)=\overline{A}+\overline{B}\text{, and}$$

$$(A+B)(C+D)=AC+AD+BC+BD.$$

The PLD software determines the best form of the equation that will fit into a PLD, which uses a general architecture to permit implementation of a wide range of functions. The software should allow you to think in terms of logical functions rather than gates. The better the software, the more you can abstract from the details of discrete design and attend to system concerns.

Once you've decided to use a PLD approach, you'll need to choose the software development support for that device. You can use two basic types of software: assembler-based software and compiler-based software **(Ref 1).** Assembler-based software is supplied by the PLD manufacturer; it typically supports only that manufacturer's devices. If you buy PLDs in large quantity, you can usually get the software for well under $100. An alternative to assembler-based software is the compiler-based software sold by Data I/O and Assisted Technology. Compiler-based software supports almost all PLD devices and programmers; typical prices range from $750 for a version that runs on CP/M-based systems to $2695 for a version that runs on VAX/VMS systems.

Although compiler-based software is more expensive, it will make your PLD design task easier. Capabilities such as symbolic signal representation and macro substitution make it easier for you to formulate and enter your logic equations. These improvements allow you to formulate your design at a higher conceptual level; that is, you can think in terms of systems instead of individual circuits.

Fig 2 illustrates the PLD design process using Assisted Technology's CUPL language. (The Abel language, developed by Data I/O, could also be used to demonstrate the techniques involved.)

The CUPL syntax

Before you can design with CUPL, you have to learn the syntax. CUPL's operators, which were chosen largely from the C programming language, are as follows:

&=logical AND
#=logical OR
$=logical exclusive-OR
!=logical negation.

You can place comments anywhere within a CUPL logic specification by using the symbol /* for "start comment" and the symbol */ for "end comment." You can also nest parentheses to any level, as in this example: OUT=!((A&B)&(C#(D&E))).

To facilitate clear documentation, CUPL allows you to use symbolic names of arbitrary length (the first 31 characters must be unique). Symbolic names can represent pin variable names, internal device nodes, intermediate variables, bit-field representations, and symbolic constants. To further improve clarity, you can use the underscore character—

RAM_PARITY_INT_EN.

When you're converting an existing design, CUPL allows you to give symbolic names to internal nodes within your design. For example, for flip-flops connected to the pin PIN_VAR, you would name the node as follows:

- D-type flip-flop—PIN_VAR.D=Expression

The PLD architecture contains a fixed logic array made of a programming matrix and AND gates whose outputs feed OR gates.

- JK-type flip-flop—PIN_VAR.J=Expression, PIN_VAR.K=Expression
- RS-type flip-flop—PIN_VAR.R=Expression, PIN_VAR.S=Expression.

For 3-state-device enable signals connected to a pin, you would write:

- PIN_VAR.OE=Expression
- [PIN_VAR LIST].OE=Expression,

as in [DATA7..0].OE=Expression. If you're leaving the 3-state device enabled, you don't have to write an equation for it.

Handling signal polarities

One issue that often confuses first-time PLD users is the representation of signal polarities. In CUPL, you can always write equations in positive logic, regardless of the polarity of the signals entering the device. Because all signals entering the PLD are buffered, you have access to both the true and complement versions of the input signal for your logic equations. **Fig 3** illustrates two simple cases. For each case—if you were using the PLD as an AND gate—you would write the same logic equation: OUT=IN_1&IN_2.

The specification of signal polarities is complicated by the inverting-output architecture of, for instance, 20-pin PAL devices (**Fig 4**). If you need an active-low output polarity, this doesn't create a problem. In this case, the compiler has to implement only one P (product) term. However, if you need an active-high output signal, the compiler must apply De Morgan's theorem,

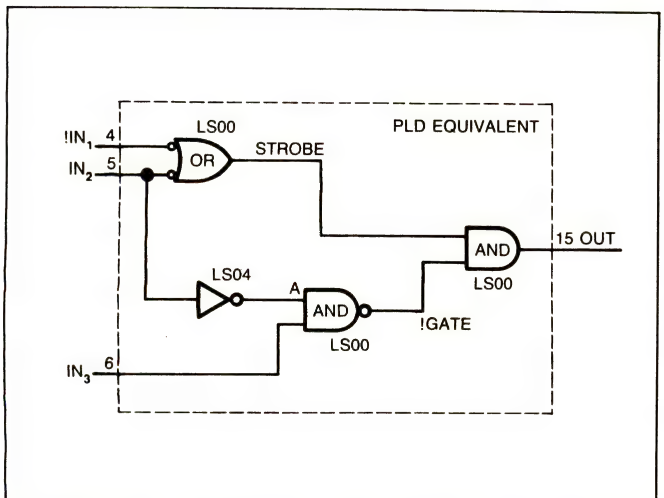

Fig 5—With CUPL, you can often replace a TTL design without understanding its function. *You just name the pins and nodes, combine them according to gate relationships in the circuit, and the software does the rest.*

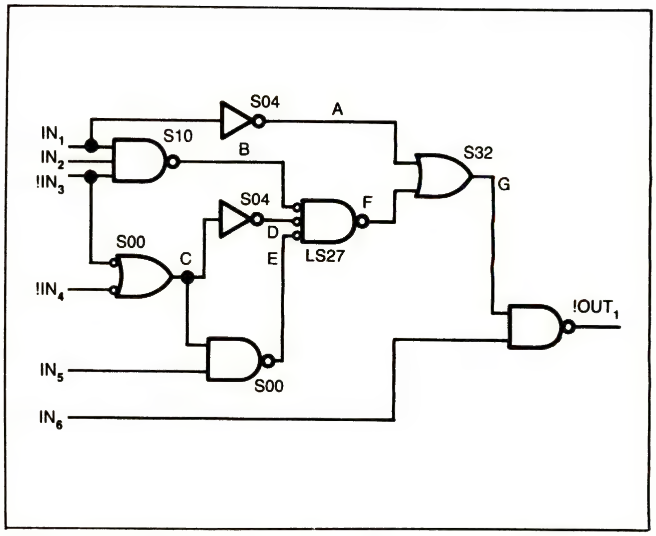

Fig 6—Reduced propagation delays *are one of the benefits of using PLDs. A PLD implementation of the circuit shown here has, on the average, half the propagation delay of the discrete implementation.*

and !OUT_1=!(IN_1&IN_2) becomes !IN_1#!IN_2. Note that this equation contains two product terms. The additional space the compiler requires reduces the probability that the compiler will be able to fit the logic function into the target PLD.

CUPL can eliminate this problem for PLD devices that have programmable output polarities. CUPL automatically chooses the output polarity that will result in the fewest number of P terms.

Reduce keystrokes

One of CUPL's (and Abel's) major advantages is macro substitution, the ability to use a single variable name to represent a complex logical equation. For example, if you define "INT_VAR" as "A&B#C," the compiler will insert A&B#C every time it encounters INT_VAR.

Because macro substitution lets you use fewer keystrokes to write equations, it saves time and reduces the probability that you'll make input errors. By using macro substitution, you can write your logic specification in a hierarchical fashion, breaking complex equations into more manageable and readable pieces.

The logic description

The heart of CUPL is the logic-description file (LDF), which contains your logic equations, pin declarations, intermediate variables, and documentation describing the device's function. You must complete the LDF to prepare your logic equations for downloading to

a programming device. **Table 1** shows the format for a CUPL LDF that was written for a memory decoder.

The following example shows you how to complete the logic equation, pin declaration, and intermediate variable portions of an LDF for the design in **Fig 5**. First, you write the pin declarations using the same names and signal polarities that appear on your schematic. Next, you name the output of each gate in the schematic. In the example, STROBE, A, and !GATE are the intermediate variables. Using the intermediate variable definitions, you then write an equation for the output:

$$\text{PIN } 4 = !IN_1$$
$$\text{PIN } 5 = IN_2$$
$$\text{PIN } 6 = IN_3$$
$$\text{PIN } 15 = OUT$$
$$A = !IN_2$$
$$STROBE = !(!IN_1)\#!IN_2; \; /^*!(!IN_1) = IN_1{}^*1$$
$$!GATE = !(A\&IN_3)$$
$$OUT = STROBE\&!GATE.$$

The following expressions show this strategy applied to the more complicated design in **Fig 6**:

$$A = !IN_1$$
$$B = !(IN_1\&IN_2\&!IN_3)$$
$$C = !(!IN_3)\#!(!IN_4)$$
$$D = !C$$
$$E = !(C\&IN_5)$$
$$F = !B\&!D\&!E$$
$$G = A\#F$$
$$!OUT = (G\&IN_6).$$

The design in **Fig 6** illustrates another advantage of using PLDs instead of discrete logic. The propagation delay in the PLD implementation is often less than that in the discrete design. The discrete design for this circuit requires at least three TTL packages and has five levels of delay. The total delay time is 50 nsec (five levels times 10 nsec/level) for LS packages and 26 nsec (4×4 nsec+10 nsec) for a combination of LS and Schottky TTL packages. In an equivalent PLD circuit, the maximum delay is 25 nsec; typical delay is only 15 nsec.

TABLE 1—SOURCE SPECIFICATION FILE FORMAT

FUNCTION	DESCRIPTION
PART NO 900 16487 NAME MEMDEC DATE 07/18/84 REV 03 DESIGNER OSANN COMPANY ATI ASSEMBLY PC-RAM LOCATION 417	HEADER INFORMATION: IDENTIFIES THE PARTICULAR LOGIC SOURCE FILE
THIS DEVICE DECODES ADDRESSES FOR THE DYNAMIC RAM AND PROVIDES THE RAS STROBES AS WELL AS A SIGNAL THAT INITIATES CAS.	TITLE BLOCK: DESCRIBES IN PLAIN TERMS WHAT THIS DEVICE DOES.
ALLOWABLE TARGET DEVICE TYPES: PAL 16L8, 825153, EP300.	DEVICE MENU: LISTS ALL TARGET DEVICE TYPES THAT MAY BE USED.
INPUTS:	PIN DECLARATIONS:
PIN [1..6] = [A 19..14]	CPU ADDRESS BUS
PIN [7, 8] = ! [MEMW, MEMR]	MEMORY DATA STROBES
PIN 9 = ! REF_ADR_EN	INDICATES REFRESH CYCLE IN PROGRESS
PIN 11 = ! REF_RAS	STROBE FOR RAS-ONLY REFRESH
PIN 13 = ALT_LOC	PLACE MEMORY IN ALTERNATE RANGE
OUTPUTS:	
PIN [19..16] = ! [RAS 3..0]	RAM ROW ADDRESS STROBES
PIN 14 = ! CAS_INIT	ENABLE CAS STROBES
DECLARATIONS AND INTERMEDIATE VARIABLE DEFINITIONS:	WRITE EQUATIONS FOR BIT-FIELD DECLARATIONS AND INTERMEDIATE VARIABLES WHICH WILL BE SUBSTITUTED LATER USING MACRO-SUBSTITUTION:
FIELD MEMADR = [A19..A14]	MEMORY ADDRESS
MEM REQ = MEMW # MEMR	MEMORY REQUEST
LOGIC EQUATIONS:	WRITE EQUATIONS FOR OUTPUTS IN TERMS OF INPUTS AND FEEDBACK AS IN: OUTPUT = INPUT 1 & FEEDBACK 1 # INPUT 2 & FEEDBACK 2 # INPUTS N & FEEDBACK N

FUNCTION	DESCRIPTION
RAS 3 = MEMREQ & ! REF_ADR_EN &	
(! ALT_LOC & MEMADR: [0C000...0FFFF]	PRIMARY RANGE
# ALT_LOC & MEMADR: [FC000...FFFFF)	ALTERNATE RANGE
# REF_ADR_EN & REF_RAS	REFRESH CYCLE
RAS 2 = MEMREQ & ! REF_ADR_EN &	
(! ALT_LOC & MEMADR: [08000...0BFFF]	PRIMARY RANGE
# ALT_LOC & MEMADR: [F8000...FBFFF)	ALTERNATE RANGE
# REF_ADR_EN & REF_RAS	REFRESH CYCLE
RAS 1 = MEMREQ & ! REF_ADR_EN &	
(! ALT_LOC & MEMADR: [04000...07FFF]	PRIMARY RANGE
# ALT_LOC & MEMADR: [F4000...F7FFF)	ALTERNATE RANGE
# REF_ADR_EN & REF_RAS	REFRESH CYCLE
RAS 0 = MEMREQ & ! REF_ADR_EN &	
(! ALT_LOC & MEMADR: [00000...03FFF]	PRIMARY RANGE
# ALT_LOC & MEMADR: [F0000...F3FFF)	ALTERNATE RANGE
# REF_ADR_EN & REF_RAS	REFRESH CYCLE
CAS_INIT = MEMREQ & ! REF_ADR_EN &	
(! ALT_LOC & MEMADR: [00000...0FFFF]	PRIMARY RANGE
# ALT_LOC & MEMADR: [F0000...FFFFF)	ALTERNATE RANGE

Registered PLDs

Some of the more complicated types of PLDs use flip-flops in their output stages to store information. Most of these PLDs provide integral feedback paths. The simplest registered PLDs contain D-type flip-flops, which transfer the signal at their D input to their Q output after one clock pulse (more specifically, after the application of a positive-going leading edge). The equations for the flip-flop in **Fig 7** are

```
OUTPUT.D=G&INPUT /*UPDATE WITH INPUT*/
         #!G&OUTPUT; /*MAINTAIN CURRENT OUTPUT*/
                     /*VIA INTERNAL FEEDBACK DATA*/.
```

For simple registered designs, you can often model

Compiler-based software for PLD design includes such features as symbolic signal representation and macro substitution.

the circuit with a timing diagram. Using the timing diagram, you can write your logic equations easily. In the **Fig 8** timing diagram for a D-type flip-flop, $INPUT_2$ initiates the input pulse, and $INPUT_1$ terminates the output pulse. The pin declarations are

PIN 3=!$INPUT_1$
PIN 6=!$INPUT_2$
PIN 1=CLOCK
PIN 14=OUTPUT,

and the corresponding logic equations are

```
OUTPUT.D=!OUTPUT&INPUT 2 /*SET FF*/
         # OUTPUT&!INPUT 1; /* KEEP FF SET*/
                            /* UNTIL INPUT 1*/
                            /*GOES ACTIVE*/.
```

These equations demonstrate one method for using the smallest possible number of product terms to keep a D flip-flop set for several clock cycles. Here, the flip-flop's output is fed back until some condition is met that again enables the flip-flop.

If the registered PLD contained JK flip-flops, the expressions would be

OUTPUT.J=$INPUT_2$; /* SET FF*/
OUTPUT.K=$INPUT_1$; /* RESET FF*/.

To handle more complicated sequential designs, you can model your circuit as a multiple-flip-flop system that uses a common clock. (Virtually all currently available registered PLDs use common clocks for their flip-flops.) For example, to convert TTL designs that use cascaded flip-flops (in which the outputs of some flip-flops are used to clock other flip-flops), you must find the originating clock in the circuit, which is usually

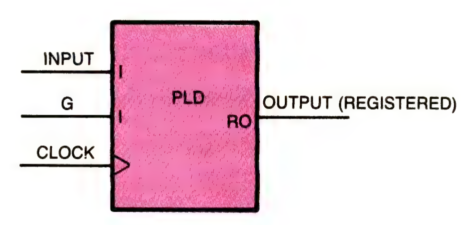

***Fig 7—Some PLDs use registered outputs** to introduce storage elements into their architecture.*

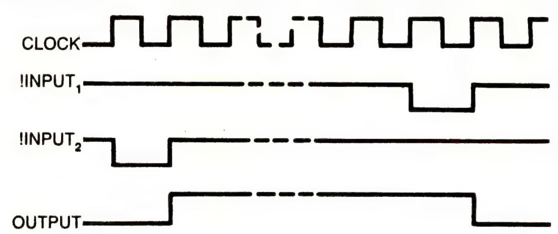

***Fig 8—Converting logic designs to PLDs is easy** once you've completed a timing diagram for your circuit. This one represents operation of a D-type flip-flop.*

TABLE 2—CUPL OPTION FLAGS

A	PRODUCE YOUR_FILE_NAME.ABS FOR LATER USE BY CSIM.
L	PRODUCE YOUR_FILE_NAME.LST WITH LINE NUMBERS AND ERROR MESSAGES.
I	PRODUCE YOUR_FILE_NAME.HL DOWN-LOADABLE HL FORMAT FILE FOR IFL.
H	PRODUCE YOUR_FILE_NAME.HEX MMI PAL ASCII-HEX FORMAT FILE.
F	PRODUCE YOUR_FILE_NAME.DOC WITH FUSE MAP FILE.
X	PRODUCE YOUR_FILE_NAME.DOC WITH FULLY EXPANDED EQUATIONS.
G	PROGRAM SECURITY FUSE.
R	DISABLE GLOBAL PRODUCT-TERM MERGING. (FPLA DEVICES).
M0	PERFORM NO LOGIC MINIMIZATION.
M1	PERFORM LOCAL LOGIC MINIMIZATION.
M2	PERFORM LOGIC MINIMIZATION UNTIL EQUATIONS FIT IN TARGET DEVICE.
M3	PERFORM FULL LOGIC MINIMIZATION.
D	DEACTIVATE UNUSED OR-TERMS. (INCREASES SPEED IN FPLAs).
U	SET ALTERNATE SEARCH PATH FOR PLD DEVICE DATABASE.
J	PRODUCE YOUR_FILE_NAME. JED, THE JEDEC FORMAT DOWNLOADABLE FILE
S	AUTOMATICALLY RUN CSIM AFTER RUNNING CUPL

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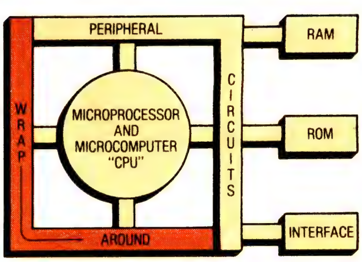
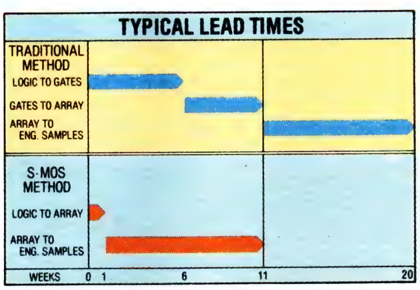


The S-MOS system



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Compiler-supported symbolic names can represent pin variable names, internal device nodes, intermediate variables, bit-field representations, and symbolic constants.

the highest-frequency source in the circuit. In most cases, the timing skew from one flip-flop output to the next is tolerable.

The TTL circuit in **Fig 9** contains an LS161 counter whose output is decoded in an LS138. The decoded output sets and resets flip-flops at various points in the timing cycle. The timing diagram in **Fig 10** is based on the assumption that the clock rate is sufficiently high that the propagation delays from SYSCLK to OUT_1 and OUT_2 are not significant. If you were to implement this design in a PLD, the pinout would look like the one shown in **Fig 11.** Outputs Q_0 and Q_1 were added to make all eight time slots in the circuit's cycle a unique combination of the four outputs. Adding Q_0 and Q_1 results in a timing sequence like the one in **Fig 12.**

You can now write the logic equations by noting, for each output, each place in the timing cycle where the output reads high (the flip-flop is set). For example, OUT_1 is set during time slots 2, 3, and 4. (The equation for the D input should include representations of time slots 1, 2, and 3; these time slots occur immediately before the flip-flop is set.) For time slots 1 through 3, you can now write

$OUT_1.D = !OUT_1\&!OUT_2\&Q_0\&!Q_1$ /*TIME SLOT 1*/
$\#OUT_1\&!OUT_2\&!Q_0\&!Q_1$ /*TIME SLOT 2*/
$\#OUT_1\&!OUT_2\&Q_0\&!Q_1$ /*TIME SLOT 3*/.

Writing these equations is easier if you first define each time slot in terms of the register outputs that are fed back into the programmable array:

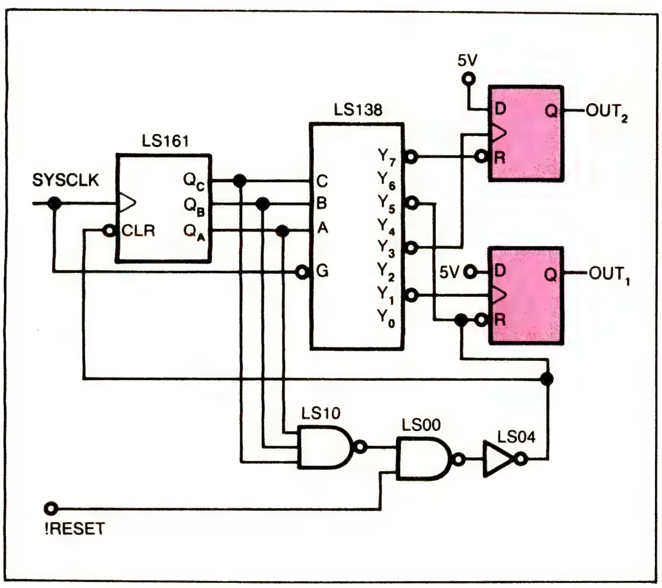


***Fig 9—When converting complex sequential designs to PLDs,** you can model your circuit as a group of flip-flops driven by a common clock.*

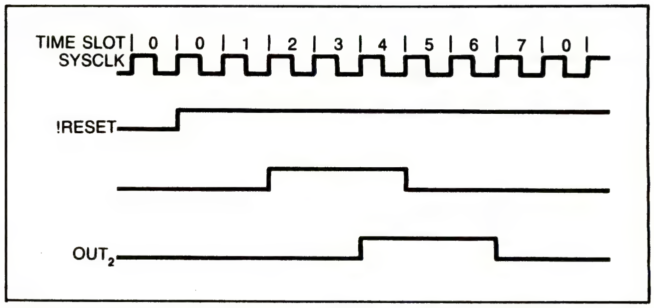


***Fig 10—This timing diagram** is based on the assumption that the **Fig 9** circuit uses a clock rate that is not significantly affected by propagation delays from SYSCLK to OUT_1 and OUT_2.*

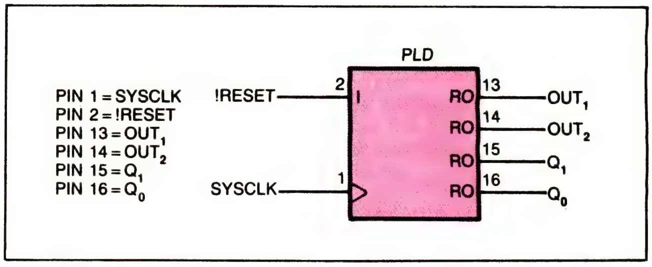


***Fig 11—Adding outputs Q_0 and Q_1** of this PLD implementation of the **Fig 9** circuit makes each of the eight intervals in the **Fig 12** timing cycle a unique combination of the circuit's four outputs.*

$TS_0 = !OUT_1\&!OUT_2\&!Q_0\&!Q_1;$ /*TIME SLOT 0*/
$TS_1 = !OUT_1\&!OUT_2\&Q_0\&!Q_1;$ /*TIME SLOT 1*/
$TS_2 = OUT_1\&!OUT_2\&!Q_0\&!Q_1;$ /*TIME SLOT 2*/
$TS_3 = OUT_1\&!OUT_2\&Q_0\&!Q_1;$ /*TIME SLOT 3*/
$TS_4 = OUT_1\&OUT_2\&!Q_0\&!Q_1;$ /*TIME SLOT 4*/
$TS_5 = !OUT_1\&OUT_2\&!Q_0\&!Q_1;$ /*TIME SLOT 5*/
$TS_6 = !OUT_1\&OUT_2\&Q_0\&!Q_1;$ /*TIME SLOT 6*/

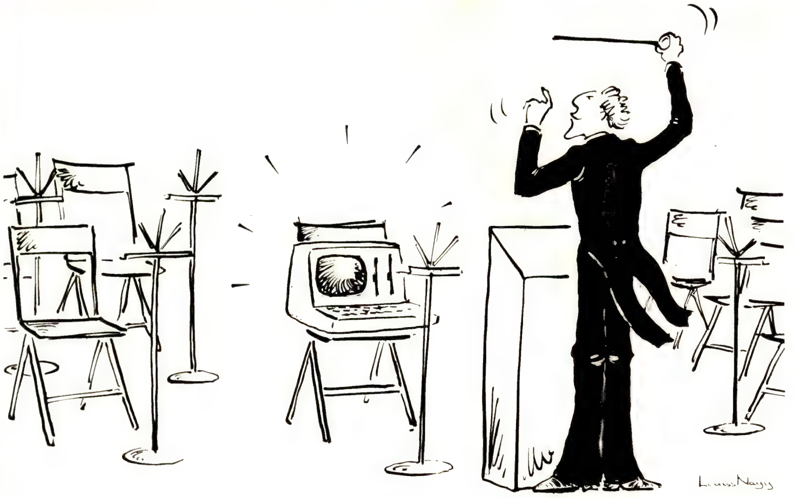
You can now write the equations for the four registered outputs in terms of TS_0 through TS_6 (TS_7 is not needed); CUPL performs the following substitutions:

$$OUT_1.D = TS_1\#TS_2\#TS_3$$
$$OUT_2.D = TS_3\#TS_4\#TS_5$$
$$Q_0.D = TS_0\#TS_2\#TS_5$$
$$Q_1.D = TS_6.$$

Running CUPL

Once you've completed the LDF, you're ready to compile the LDF for downloading to the PLD programmer. To compile the file, you type an expression that follows this format:

CUPL [FLAGS] TARGET_DEVICE_CODE YOUR_FILE_NAME.



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Model 7228 Advanced Programmer — Supports all PROM types listed. Super-fast "adaptive" programming algorithm programs 2764 in 1.1 minutes.

Model 7128 Standard Programmer — Lower-cost version of 7228. Supports all PROM types except "A" versions of 2764 and 27128. Standard programming algorithm programs 2764 in 6.8 minutes.

Avocet Cross-assembler	Target Microprocessor	CP/M-80	CP/M-86 IBM PC, MSDOS**
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XASM18	1802/1805	200.00	250.00
XASM48	8048/8041	200.00	250.00
XASM51	8051	200.00	250.00
XASM65	6502/65C02	200.00	250.00
XASM68	6800/01, 6301	200.00	250.00
XASM75	NEC 7500	500.00	500.00
XASM85	8085	250.00	250.00
XASM400	COP400	300.00	300.00
XASMF8	F8/3870	300.00	300.00
XASMZ8	Z8	200.00	250.00
XASMZ80	Z80	250.00	250.00
XMAC682 *NEW*	68200	595.00	595.00
XMAC68K *NEW*	68000/68010	595.00	595.00

Model 7956 and 7956-SA Gang Programmers — Similar features to 7228, but program as many as 8 EPROMS at once. 7956-SA stand-alone version copies from a master EPROM. 7956 lab version has all features of stand-alone plus RS-232 interface.

EPROM: 2758, 2716, 2732, 2732A, 2764, 2764A, 27128, 27128A, 27256, 2508, 2516, 2532, 2564, 68764, 68766, 5133, 5143. **CMOS:** 27C16, 27C32, 27C64, MC6716. **EEPROM:** 5213, X2816A, 48016, I2816A, 5213H. **MPU (w/adaptor):** 8748, 8748H, 8749, 8749H, 8741, 8742, 8751, 8755.

7228	**Advanced Programmer**	**$ 549**
7128	**Standard Programmer**	**429**
7956	**Laboratory Gang Programmer**	**1099**
7956-SA	**Stand-Alone Gang Programmer**	**879**
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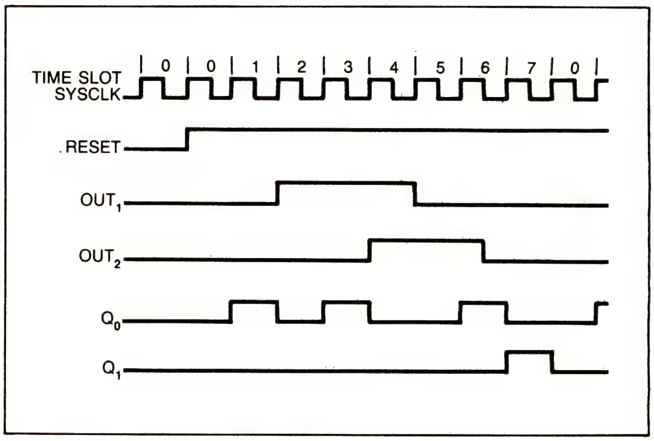

Fig 12—Once you've rewritten the Fig 10 timing diagrams *to reflect the PLD configuration in* ***Fig 11,*** *you can write a set of logic equations for implementing the PLD design.*

For example, the sequence CUPL -J -A P16L8 RAMCNTRL compiles the source file for a RAM controller that is targeted for a PAL16L8. The J and A symbols are chosen from a table of CUPL option flags (**Table 2**). In this case, the compiler produces a JEDEC file and an absolute-format file to be used later by CUPL's simulator, CSIM (**Ref 1**). The resulting compiled code is downloaded to the programmer, which then blows the appropriate fuses in the PLD.

The designs discussed thus far are simple but useful for describing the PLD design process. The next two articles will extend the discussion to more advanced designs, and finally, to the state-machine approach.

EDN

Reference

Marrin, K, "Programmable logic devices gain software support," *EDN*, February 9, 1984, pg 67.

Author's biography

Bob Osann is president and chief executive officer of Assisted Technology Inc (Sunnyvale, CA). He received his BSEE from Cornell University and was previously employed at Millennium Systems Inc (Santa Clara, CA). His hobbies include sports cars, airplanes, and music.

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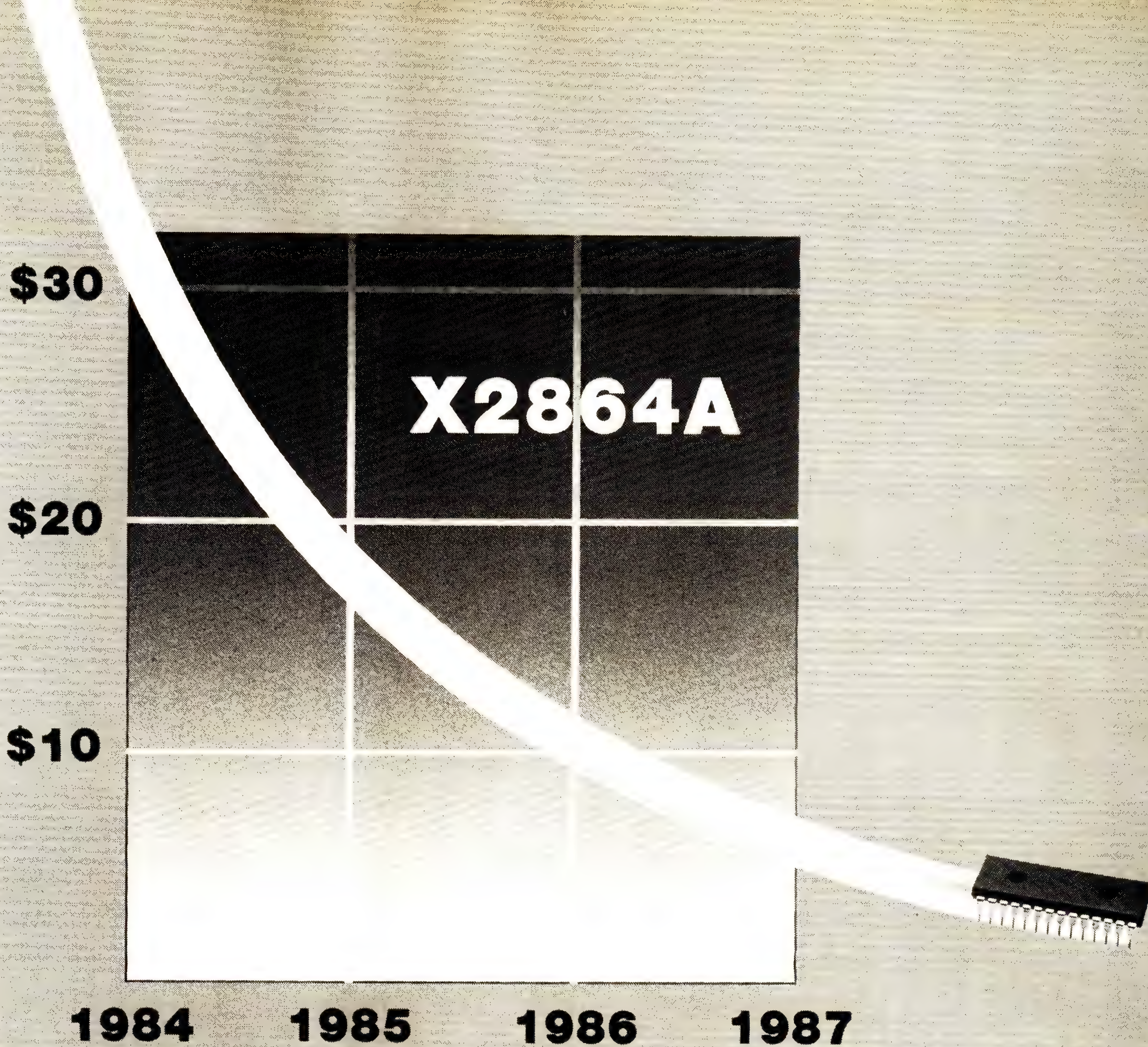

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CIRCLE NO 141

EEPROM standards and reliability: an interim report

EEPROMs exhibit a bewildering array of features, and no two manufacturers spec their parts the same way. But standards for specs and features may be emerging. This article presents Xicor's views on this vital topic, along with rebuttals from all major EEPROM makers except AMD, which declined to comment.

Richard Orlando, *Xicor Inc*

Although EEPROMs have traditionally lacked standardization, standards are beginning to emerge. You can expect most EEPROMs to offer such features as 5V-only, self-timed, and automatic erase-before-write operation as well as improved inadvertent-write-protection schemes and standardized reliability specifications.

This trend contrasts with the situation that existed in 1983, when it appeared that major EEPROM makers like Xicor, Intel, and Seeq were diverging in terms of the features they offered on 16k-bit EEPROMs, rather than converging on a 16k-bit-EEPROM standard. Unresolved issues involved pinout configurations as well as functions like self-timed operation.

Now, when many new 16k-bit devices are being offered by a variety of manufacturers, the X2816A has become the de facto industry standard. *(Ed Note: Not surprisingly, this view, as well as others that the author presents, isn't shared by other EEPROM makers; see, for example, the rebuttals from Intel and NCR.)* More important, a standard feature set for EEPROMs has evolved: A standard EEPROM is now a 5V-only, latched, self-timed device.

The evolution of a standard feature set for 16k-bit EEPROMs has helped to pave the way for standardization at the 64k-bit level. In mid-1983, three major vendors announced 64k-bit EEPROMs. Although these devices all featured 5V operation, the similarities ended there. Inmos's 3630 offered address and data latches but not self-timed write operation (a feature that many engineers had found desirable in 16k-bit devices). Seeq's 52B33 was another latched device that had no self-timing function. Unfortunately for designers looking for multiple-sourced parts, this device was incompatible with the Inmos device because the companies used different control signals to latch addresses and data.

Xicor introduced the 64k-bit X2864A as an extension of its 16k-bit X2816A; the newer Xicor device included not only latched and self-timed operation, but the $\overline{\text{Data}}$-polling function and page-mode-write operation.

Now, many vendors have introduced 64k-bit EEPROMs, and a look at these devices' specs suggests the emergence of the following standard feature set:

- 5V-only operation
- address and data latches
- self-timed write operation
- automatic erase-before-write operation
- page-mode-write capability
- write-cycle-completion notification

A standard feature set for EEPROMs has evolved: A standard EEPROM is now a 5V-only, latched, self-timed device.

FEATURES OF 64k-BIT EEPROMs

	INMOS 3630	SEEQ 52883	HITACHI 48064	AMD 2864	INTEL I	XICOR 2864A	EXEL XL2864A	EXEL 48C64	SEEQ 28C64
5V OPERATION	•	•	•	•	•	•	•	•	•
ADDRESS AND DATA LATCHES	•	•	•	•	•	•	•	•	•
SELF-TIMED WRITE				•	•	•	•	•	•
AUTOERASE BEFORE WRITE				•	•	•	•	•	•
PAGE-MODE WRITE	•				•	•	•	•	•
ENHANCED WRITE PROTECTION					•	•	•	•	•
READY/$\overline{\text{BUSY}}$				•	•		•	•	•
$\overline{\text{DATA}}$ POLLING					•	•	•	•	
CMOS								•	•
1M-CYCLE ENDURANCE									•
1-mSEC BYTE WRITE									•

NOTE: HIGHLIGHTED PORTION OF TABLE, PREPARED BY XICOR, ILLUSTRATES THAT FIRM'S VIEW OF EEPROM STANDARDS; ITS 2864A OFFERS ALL THE HIGHLIGHTED FEATURES EXCEPT READY/$\overline{\text{BUSY}}$, WHICH THE FIRM DOESN'T INCLUDE BECAUSE OF PACKAGING AND PAGE-MODE-OPERATION CONSIDERATIONS. THE TABLE'S RIGHT-HAND COLUMN AND BOTTOM THREE ROWS WERE ADDED BY SEEQ TO ILLUSTRATE THE FEATURES OF ITS 28C64 CMOS EEPROM.

- improved inadvertent-write-protection schemes
- standardized reliability specifications.

The **table** illustrates the similarities among various manufacturers' 64k-bit products. Roman numerals designate parts that don't as yet have part numbers.

5V operation cuts circuitry requirements

Although 5V-only operation is now typical, many of the older devices required you to provide an additional high-level voltage (more than 15V) for EEPROM programming. On-chip charge pumps eliminated the need for an external high-voltage supply. Unfortunately, the advent of 5V-programmable EEPROMs also introduced a major application problem for engineers. Because the devices require only 5V to perform a write operation, you must take special care when designing a system to ensure that the devices won't receive the signals for a write operation during power up and power down. Otherwise, corruption of EEPROM data could result.

However, the address and data latches on the new EEPROMs solve a major problem that exists in the older EEPROMs. If an EEPROM doesn't have on-board latches (some EEPROMs don't), you must provide external components for this purpose. The only alternative is to freeze the system's bus during the entire write interval, which seriously degrades system performance. Performance is degraded because the system microprocessor must hold the address and data valid during the write cycle, which for an EEPROM is relatively long—1 to 10 msec.

The self-timed write feature also reduces the amount of supervision that external circuitry must provide to

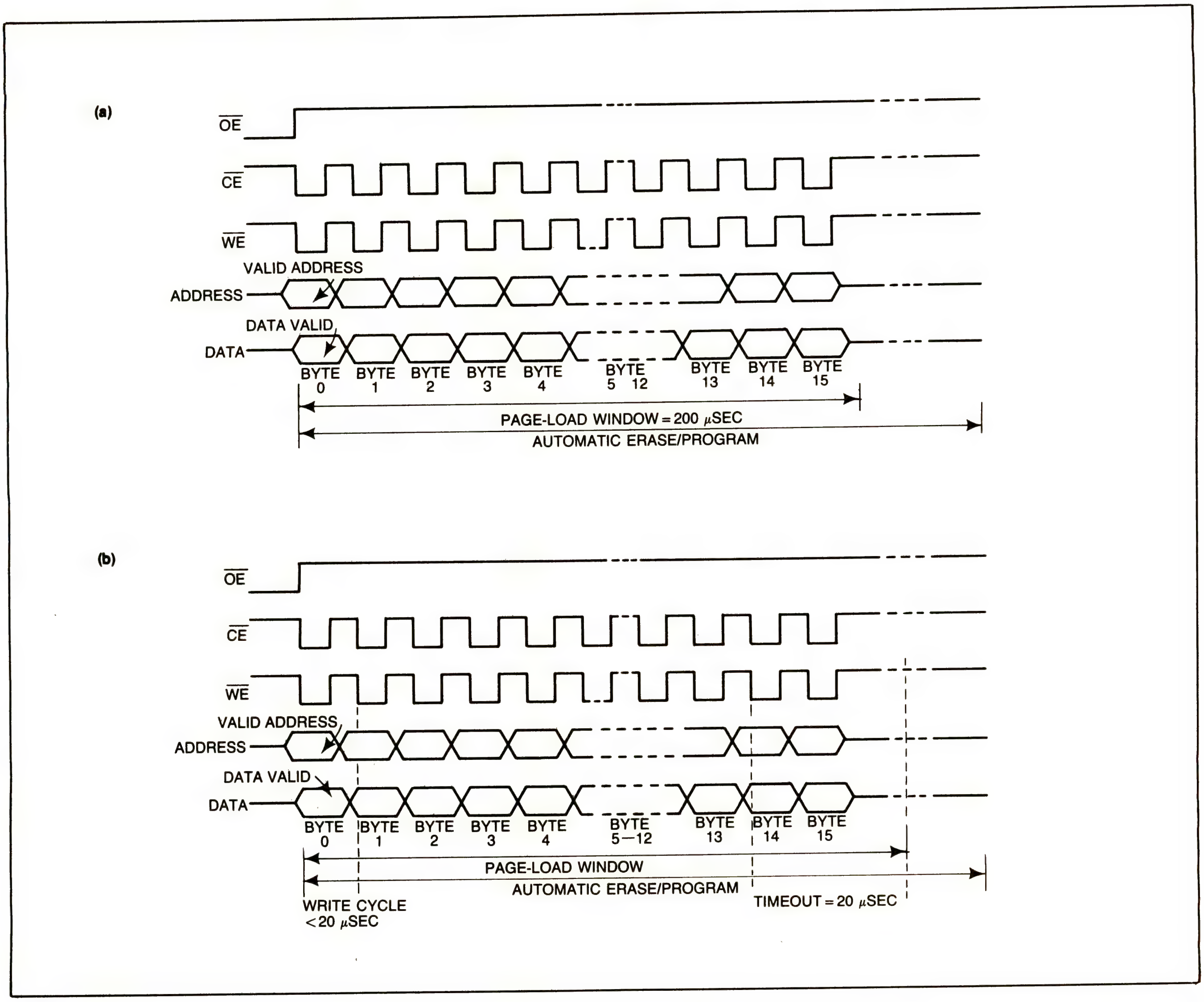


Fig 1—Two schemes for page-mode write *differ in the length of the time window allowed for writing. Part **a**'s window stays open for 200 µsec, allowing you to write to as many bytes as you wish as many times as you wish. Part **b**'s window is only 20 µsec long; if you don't continue to write to the chip, the window closes. This scheme proves advantageous when you're updating just a few bytes on a memory page.*

the EEPROM during the write operation. On-chip timers, instead of the processor, tell the EEPROM when to start and when to stop the nonvolatile write operation. These timers can be optimized for a particular device to minimize the write-cycle time without jeopardizing the device's endurance. (The endurance spec is the number of times you can write to an EEPROM bit cell without significantly degrading its data-retention capability.)

An EEPROM's internal construction resembles that of an EPROM; the write operation requires that a bit be erased before it can be written to. To write arbitrary data to a byte, you must first erase the byte to set all bits to the erased state (all ones in most cases). In the past, EEPROMs required you either to precondition the byte to be written with a byte-erase operation or to erase the chip before writing.

In an effort to make their EEPROMs look more like writable memories than like EPROMs, manufacturers designed the automatic erase-before-write feature into their self-timed chips. If the address and data are already latched onto such a chip, then the chip can

Text continues on pg 164

NCR: Xicor's specs are not standard

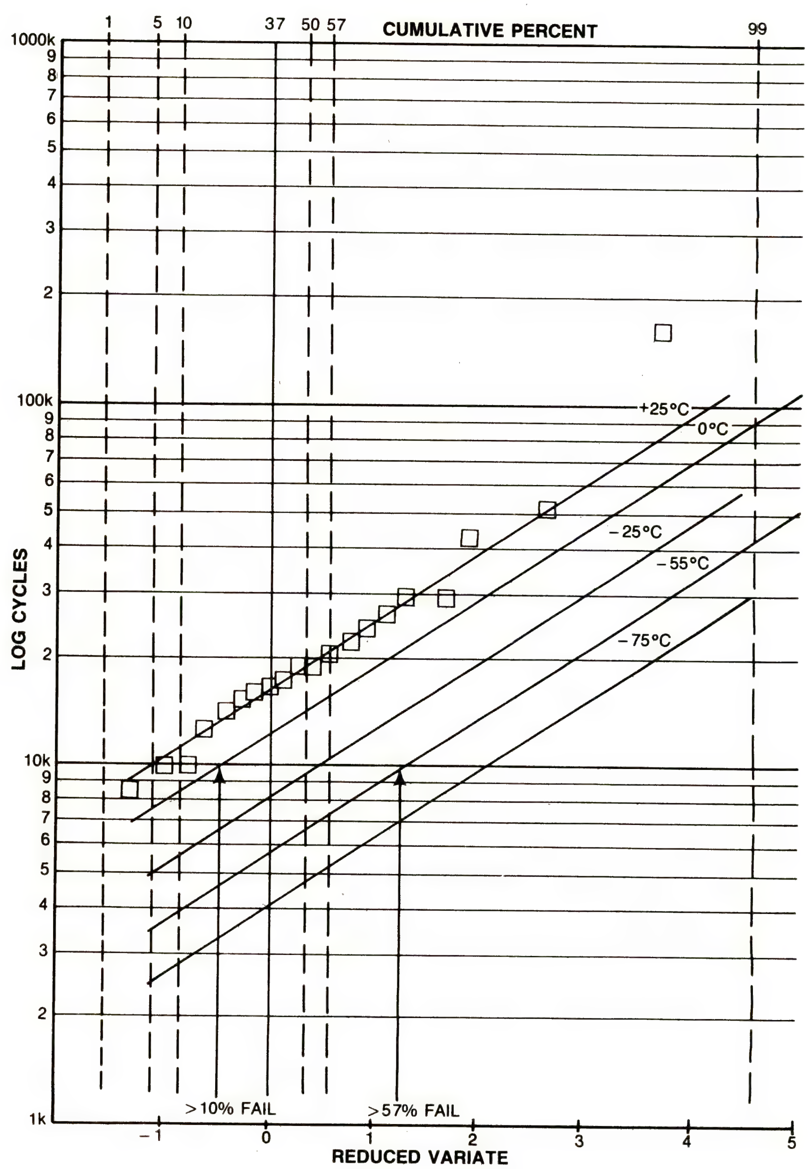
Jim Globig,
NCR Microelectronics

NCR agrees with Xicor that 5V operation, address and data latches, page-mode operation, and improved inadvertent-write-protection schemes should be part of a standard EEPROM feature set. But the features that Xicor cites concerning the transparent write cycle are not and should not be standardized; they are part of only Xicor's "emerging standard," not of the industry standard.

Although such features make EEPROMs easier to use, they do not give you the flexibility to specify any endurance/retention levels other than the values given on the data sheet (if indeed such values appear on the data sheet at all). In contrast, the SNOS process, which has achieved well over 100,000 erase/write cycles on NCR's 52832 or 52864 EEPROMs, lets you make tradeoffs between the endurance and retention offered by a single device, a feature that many floating-gate devices do not offer.

Other points that Xicor makes also require clarification or correction. For instance, Xicor states that the only way to decrease an EEPROM's programming interval is to increase the tunneling voltages. Not true. One of the more obvious solutions is to change the composition or the thickness of the dielectric or storage medium.

In addition, Xicor's reliability specs and data are not typical of those of other manufacturers.



Taking the data from Fig 3a (25°C) *and extrapolating to 0, −25, −55, and −75°C reveals poor performance for the characterized parts at the low end of the commercial, industrial, and military temperature ranges.*

Xicor doesn't specify retention time on any of its nonvolatile devices. And you shouldn't assume that when retention time isn't specified, it's infinite.

Moreover, even when retention time *is* specified, you shouldn't assume that the spec

holds for the ten-thousandth erase/write cycle. An important question you should ask is whether the retention time is specified after the first erase/write cycle or after 1000, 5000, or 10,000 erase/write cycles.

Unlike Xicor, NCR specifies 10-year retention after 10,000 erase/write cycles on every EEPROM it sells. NCR tests the retention time of each of its nonvolatile memory devices by using its memory-margining procedure, a procedure that any customer can perform.

Xicor also employs a nonstandard method of specifying endurance. Xicor states that the meaning of its endurance specification is that less than 5% of any lot of its nonvolatile memories will have an endurance of fewer than 10,000 cycles. However, an important point has been omitted. Xicor's "Reliability Report #504" (RR504) states: "What a Xicor endurance specification means is that for any lot of memories shipped, fewer than 5% of the units will cease to cycle before the specified limit when cycled at room temperature and at the maximum frequency allowed by the specification."

In contrast, the meaning of an NCR endurance specification is no different from that of any other specification—including retention time—on its data sheets. That is, the outgoing average quality level (AQL) of NCR products is consistently better than 0.5% (this includes endurance and retention failures), which is better by more than a factor of ten than the specs resulting from Xicor's definition of an endurance specification. And NCR specifies endurance and retention over the full temperature range of the device—not just at 25°C.

Curiously, in Xicor's extreme-value plots (**Fig 3** in the main text), the endurance curves become very flat at the lower endurance points. NCR thinks that the shape of the curve in **Fig 3c** is more typical of an actual endurance curve.

Furthermore, Xicor states that increasing the cycling period by a factor of 1000 can increase the worst-case endurance by a factor of three and that increasing the device temperature to 50°C will double the endurance of typical devices. Xicor also states that if you operate your system at 50°C and extend the cycling period to greater than 1 minute, you will further decrease typical failure rate to 0.001%. But few designs could afford such constraints.

Xicor's RR504, which contains **Figs 3b** and **3c**, states that these figures "lack vertical scales because they are intended to show general tendencies." The following analysis may reveal the real reason the endurance scales on **Figs 3b** and **3c** were omitted, and it also may reveal some startling inadequacies in Xicor's floating-gate process.

The accompanying **figure**, based on the best-case data of **Fig 3a,** illustrates the degradation of endurance because of temperature that Xicor describes. It shows that at 0°C (the low end of the commercial temperature range), four Xicor nonvolatile RAMs out of 20 will not meet the 10,000-cycle endurance specification (a 20% failure rate). At −40°C (the lower end of the industrial temperature range), approximately 60% of the devices will not meet the standard endurance specification. Finally, at −55°C, approximately 75% of Xicor's devices will not meet the standard endurance specification for nonvolatile memories. NCR believes that selling lots of devices that exhibit the nonvolatile-device endurance characteristics described by Xicor will have serious consequences on other nonvolatile-device manufacturers.

NCR encourages current and potential nonvolatile memory users to examine the "SNOS Non-Volatile Memory Reliability" report found in its 1985 Data Book, for which quarterly updates will be available.

Finally, note that NCR has not only announced its 52864 64k-bit EEPROM but is also delivering it. The 52864 is one of the few devices available that operates over the full military temperature range.

The author is a principal applications engineer for NCR Microelectronics, Miamisburg, OH.

The self-timed write feature reduces the amount of supervision that external circuitry must provide to the EEPROM during write operations.

automatically erase the byte to be written before the programming cycle begins. This makes the write operation analogous to writing to a RAM, except that the device will be unavailable for subsequent reads or writes for the 1- to 10-msec write-cycle time.

The EEPROM manufacturers have addressed this long write period in a variety of ways. The Inmos 3630 lets you make tradeoffs between write-cycle time and data retention to allow for a very fast write operation (several hundred microseconds) but a short retention interval. Other manufacturers, most notably Seeq, have tried to reduce the required interval for programming and still maintain a long data-retention interval. The only way to do this is to increase the tunneling voltages, which can overstress the tunneling oxide and thereby cause endurance problems because of oxide breakdown or excessive electron trapping in the oxide.

Another way to reduce the overall write time for the system is to employ a page-mode-write mode. This mode lets you write many bytes into the device for a single device-programming cycle. Although page sizes range from 16 to 32 bytes depending on the manufacturer, the page-mode-write feature is either available from or being developed by most EEPROM manufacturers.

The savings in program time for a 64k-bit EEPROM with the page-mode-write capability can be significant. For example, if you rewrite a 64k-bit EEPROM that has a 10-msec write time one byte at a time, it would take more than 80 sec to write to the entire device. If you use the page mode with the same programming cycle, the entire device typically could be rewritten in just over 2 sec (5 sec max), assuming a page is 16 bytes. All automatic-page-write implementations let you write single bytes and partial or full pages without

Intel: Xicor parts don't define standards

Donald Knowlton, *Intel*

Although Intel agrees with Xicor that a healthy move toward standardization is occuring in the EEPROM industry, Intel disagrees on the details of the final standard. The firm believes that the 64k-bit EEPROM is probably the first EEPROM that will see any meaningful level of standardization.

Meanwhile, despite Xicor's claims, there is no de facto standard in the current 16k market. Indeed, the lack of 16k standards has actually confused engineers and held back EEPROM growth.

Differences between the Xicor 2816A and the Intel 2817A illustrate the lack of standardization at the 16k-bit level. Both parts are sold in high volumes, but they are not pin compatible, and both are second sourced.

One of the key differences between these 16k-bit devices is the end-of-write indication scheme: Ready/$\overline{\text{Busy}}$ vs $\overline{\text{Data}}$ polling. At the 64k level, neither technique has an advantage in page-mode operation. Rather, the issue is the timing of the indicator—whether the indicator is a $\overline{\text{Data}}$-polling or a Ready/$\overline{\text{Busy}}$ signal.

If an engineer designs a circuit that blindly accepts an end-of-write indicator immediately after writing each byte, either indication scheme will give an erroneous end-of-write signal in some cases. Knowing this, you can set a software timer to check the indicator only when the indicator will be guaranteed to be valid. This must be done for both $\overline{\text{Data}}$-polling and Ready/$\overline{\text{Busy}}$ devices.

In large EEPROM arrays, a Ready/$\overline{\text{Busy}}$ pin is superior to $\overline{\text{Data}}$ polling. The memories in the array can be ORed together, making it unnecessary to poll each device separately. In addition, the processor can process a Ready/$\overline{\text{Busy}}$ signal as an interrupt input, which saves the time $\overline{\text{Data}}$-polling devices require to fetch previous data, negate it, and compare it to current memory output.

Finally, in addition to upward compatibility, you should also consider downward compatibility. The 64k-bit devices with both a Ready/$\overline{\text{Busy}}$ pin and $\overline{\text{Data}}$ polling can be upwardly and downwardly compatible in some configurations. A 28-pin, 64k-bit EEPROM with both modes is fully hardware compatible with the 16k-bit 2817A's Ready/$\overline{\text{Busy}}$ signal. With a single jumper, it is also fully compatible with a 28-pin, 256k-bit device. You can use a single-board design in 16k- to 256k-bit devices. In contrast, when Xicor moves from the 16k-bit level to the 64k-bit level, it must move from from a 24-pin to a 28-pin socket.

The author is strategic business segment marketing manager for Intel, Folsom, CA.

Hitachi: Standards aren't everything

Carol Cooke
Hitachi America Ltd

Unfortunately for the multitude of designs waiting on back burners (and for many niche-market users who are still waiting for volume commitments for full-featured 64k-bit parts), the so-called emerging standard features are expensive, unnecessary, and unavailable for the preponderance of potential users. The prohibitive manufacturing costs for devices with these features, combined with the absence of reliable sources of supply, have stifled EEPROM market growth.

Cell-design and process considerations are more important to the EEPROM market. These factors address the problems involved in building higher-density devices more realistically than does pin-out juggling. Improved NMOS deeper-well cell designs, for example, should facilitate the manufacture of higher-density NMOS and CMOS EEPROMs.

Hitachi's new HN58064P 8k×8-bit EEPROM, which is being introduced now, is a 5V, fully latched device made by an MNOS process with NMOS cells and fault-tolerant lateral conductivity. The device's cost is commensurate with that of a 64k-bit static RAM, and it will soon be readily available in production volumes.

The author is a senior product marketing engineer for nonvolatile memories at Hitachi America Ltd, San Jose, CA.

changing the bytes that aren't updated.

Fig 1a shows one implementation of the page-mode-write feature. Upon receipt of a write signal, the EEPROM latches the most significant address line presented to it and begins internally timing a 200-μsec page-load window. During this window, the system can write to any of the bytes on the same page any number of times. Once the 200-μsec timer expires, the device writes into the EEPROM the bytes that were updated during the window.

Fig 1b shows a second implementation of the feature. Here, the first write cycle sets the page and starts a timer. But now, the timer runs for only 20 μsec. If another write operation isn't performed before the 20-μsec timer expires, the chip closes the page-load window and performs the write operation. The device will not close the page-load window (up to a practical limit) as long as you perform writes continuously within 20 μsec of each other. This method reduces the write time for partial pages because the page-load window is open long enough to get only the bytes to be written.

Page-mode write suits EEPROM testing

Manufacturers haven't incorporated the page-mode-write feature into the new generation of EEPROMs only to benefit users. They've put the feature in to reduce EEPROM test time as well. Although the devices were originally envisioned as EPROM replacements, the writable nature of the EEPROMs suits them to applications in which they get used more as RAMs than as EEPROMs. But because of an EEPROM's long write cycle, it is virtually impossible to duplicate all of the typical RAM tests on an EEPROM. For example, if a firm were to subject a 16k-bit EEPROM to the same tests that it performs on a 16k-bit RAM, testing a single EEPROM would take more than 1½ hours. So, manufacturers are making devices easier to test by providing mass-mode programming (in which a single command can set a device to all ones or all zeros) and page-mode-write operation.

The actual write-cycle time of self-timed EEPROMs varies from device to device. The time varies within the same device as well, because of external application-dependent characteristics such as temperature. This variation forces manufacturers to specify write-time intervals that no device can exceed. As a result, the maximum write times specified for EEPROMs are usually much longer than their typical write times.

It's advantageous in many applications to use the actual write time of a device rather than the specified maximum, so you need some means of determining when the internal write cycle is completed. One of the two methods of determining this may become standard. The first, introduced on the 16k-bit Intel 2817, uses a Ready/$\overline{\text{Busy}}$ signal. This signal goes low (indicating "busy") when a write cycle is initiated, and it stays low until the write cycle is completed. The second approach, $\overline{\text{Data}}$ polling, first appeared on the Xicor X2864A. With this method, any attempt to read from any location of the device while it's performing its

To make their EEPROMs look more like writable memories than like EPROMs, manufacturers designed an automatic erase-before-write feature into their chips.

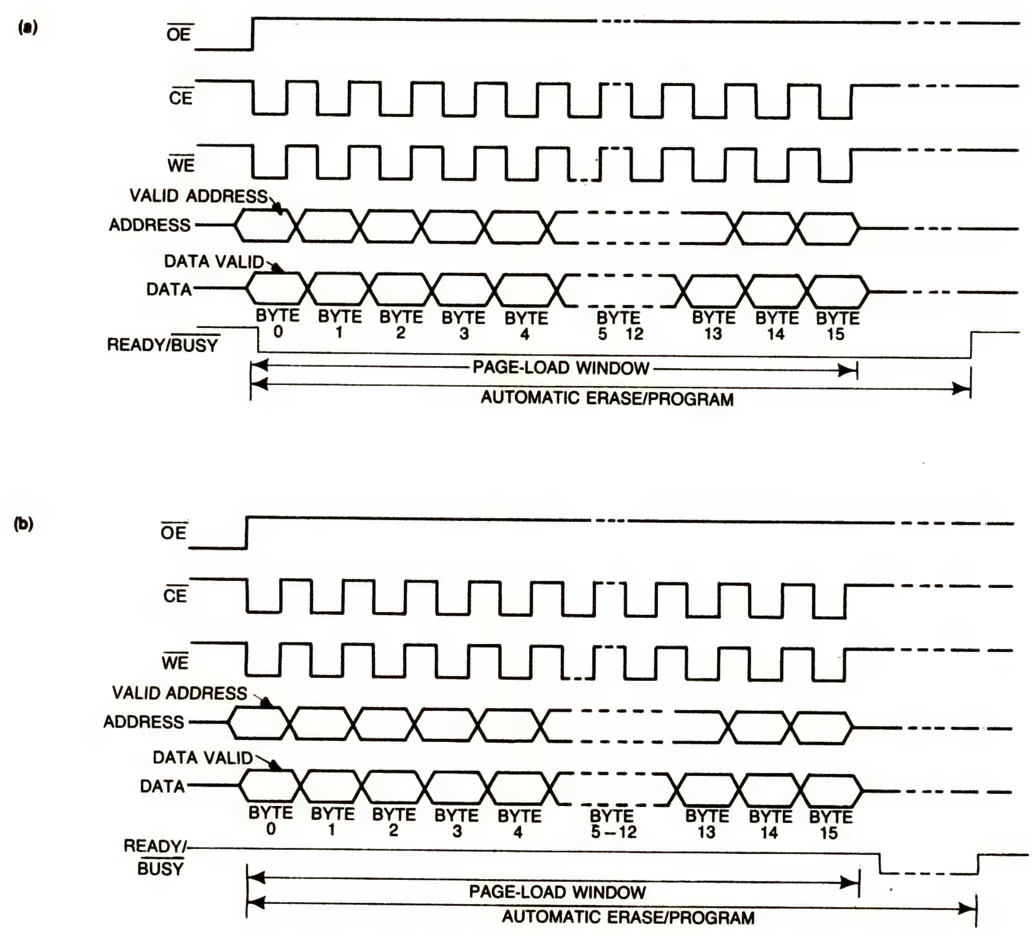


***Fig 2—The Ready/$\overline{\text{Busy}}$ pin is a hardware** signal that tells when an EEPROM is ready for more data. Part **a**'s Ready/$\overline{\text{Busy}}$ line works well with single-byte writes but goes low during a page-mode write-timing window while the device can still accept data. Part **b**'s Ready/$\overline{\text{Busy}}$ line inhibits the system during a page-mode write but stays active longer than necessary for a single-byte write.*

internal write cycle causes the device to furnish the complement of the data last written into it. So the processor can poll the device until it no longer sees the complement of the data it last wrote into the EEPROM.

The standard EEPROM-busy scheme for 64k-bit EEPROMs has not yet been determined. In fact, most manufacturers have opted for both $\overline{\text{Data}}$ polling and Ready/$\overline{\text{Busy}}$ on their devices. Xicor, however, supports only $\overline{\text{Data}}$ polling on the X2864A. Xicor is reluctant to include Ready/$\overline{\text{Busy}}$ on 64k-bit EEPROMs for several reasons. Two key reasons are that Ready/$\overline{\text{Busy}}$ is incompatible with page-mode operation, and that designing a 256k-bit, 28-pin device that supports Ready/$\overline{\text{Busy}}$ is difficult.

Ready/$\overline{\text{Busy}}$'s incompatibility with page-mode-write operation arises because all implementations of the page-mode write are *software* approaches. (There's one exception—the Inmos device—which includes several nonstandard features.) Ready/$\overline{\text{Busy}}$ is a *hardware* signal that can interrupt the processor upon the comple-

tion of the write cycle. You can optimize the Ready/$\overline{\text{Busy}}$ signal for either byte- or page-write operation but not both.

Fig 2a shows an implementation in which Ready/$\overline{\text{Busy}}$ goes low immediately after the first write cycle. This works well in byte mode but not in page mode, because in page mode the EEPROM would erroneously signal that it's busy when it's in the page-load cycle, even though it could still accept data. **Fig 2b** shows an implentation where Ready/$\overline{\text{Busy}}$ goes low after the page-load cycle is complete. This works well in page mode, but it might cause problems in byte mode were the system to check the status of the signal, see that it was not busy, and write a byte to a different page. Because Ready/$\overline{\text{Busy}}$ is a hardware implementation, it is not always compatible with software solutions like page-mode write. Because $\overline{\text{Data}}$ polling, on the other hand, is a software implementation, it's fully compatible with page-mode write.

Xicor's other key objection to the Ready/$\overline{\text{Busy}}$ approach stems from the fact that pin 1 of a 28-pin, 256k-bit EEPROM must be preserved as an address line (A_{14}), when the pin could otherwise be used as the Ready/$\overline{\text{Busy}}$ pin. Therefore, using Ready/$\overline{\text{Busy}}$ on a 256k-bit EEPROM would require more pins per package. A 40-pin package might emerge as the standard. Xicor, however, will be sampling a 256k-bit EEPROM in the first half of 1985; the firm can't afford to wait for the industry to standardize an approach that requires a package with more than 28 pins. The firm's 256k-bit unit will have 28 pins and will not include a Ready/$\overline{\text{Busy}}$ pin. Incidentally, virtually all of the manufacturers who are putting both Ready/$\overline{\text{Busy}}$ and $\overline{\text{Data}}$ polling on their 64k-bit devices acknowledge that the Ready/$\overline{\text{Busy}}$ approach will disappear at the 256k level.

Another standardization issue concerns write-protection features that minimize the amount of external circuitry required to prevent spurious write operations during power-up and power-down. One such feature is a noise filter on the Write Enable (WE) input, which prevents glitches less than 20 nsec wide from initiating a write operation. Another feature is a write-inhibit function, which requires that the Output Enable input be high in order for a write operation to take place. This

Inmos: 64k standard not here yet

O Fred Jones, *Inmos Corp*

The quest for an industry-standard 64k-bit (8k×8) EEPROM continues. Although most vendors are offering similar features on their 64k-bit EEPROMs, 100% compatibility between different vendors' parts is still rare. In other words, the de facto standard has yet to appear for 64k-bit devices.

The pinout similarity that does exist between different vendors' parts is the result of JEDEC standards. However, the JEDEC standard doesn't cover EEPROM-specific features. In fact, the JEDEC standard allows a wide variety of functions on pin 1, such as Ready/$\overline{\text{Busy}}$, V_{PP}, no connect, or, indeed, any input or output control function.

Inmos supports page-mode programming and erasing operations in its EEPROMs, but doesn't allow the devices to initiate, by themselves, nonvolatile-data-modification cycles. Instead, the user retains complete control of program/erase initiation and program/erase intervals. Inmos believes the system should control the memory device, not the reverse. Furthermore, once the device has started a programming or erasing cycle, the system can, via normal processor commands, terminate the operation at any time.

In Xicor's article, there seems to be some confusion regarding the page-mode programming used by Inmos. The article states that Inmos's page-mode implementation does not use a software-write approach. Quite the contrary. A series of software read or write instructions can control all data modifications, including page-mode writes.

As Xicor suggests, page-mode programming can reduce test times. However, by combining page-mode nonvolatile modification cycles and abbreviated program/erase intervals (this is only possible with externally controlled modification intervals, as with Inmos parts), you can reduce test times even further. With Inmos devices, you can perform voltage margining and verify the retention and endurance characteristics of each cell.

The author is the memory applications manager for Inmos Corp, Colorado Springs, CO.

Another way to reduce the overall write time is to use page-mode-write mode, which lets you write many bytes into the device for a single device-programming cycle.

Seeq: Page mode doesn't solve problem

Larry Goss,
Seeq Technology Inc

Although page-mode operation is a clever idea, and a solution in some applications to the problem of slow write times in EE-PROMs, Seeq is not, despite the intimation in Xicor's article, working on a page-mode part.

To achieve the effective data-transfer rates specified for page-mode parts, you should load data a full page at a time. Although you're not required to load full pages, throughput will suffer if you don't. Furthermore, page-mode operation solves a hardware limitation by increasing software complexity. This problem is especially acute for devices having small page sizes (16, 32, or 64 bytes), as do many parts that manufacturers have recently announced.

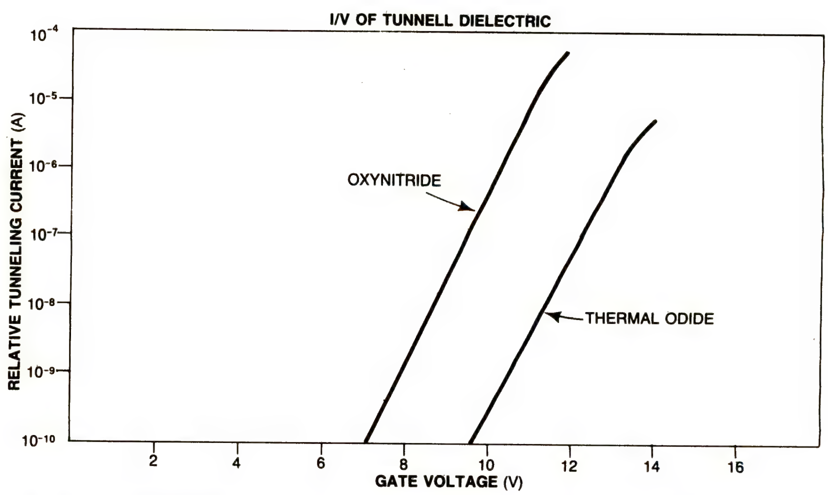
Another problem for the engineer intending to take advantage of page mode is that there's no standard for page size. There will probably never be such a standard because the physical layout of the memory array on the die, which varies from manufacturer to manufacturer, dictates optimal page size. What's more, even new generations of EEPROMs from the same manufacturer will most likely have differing page sizes.

As Xicor's article correctly states, Seeq's approach to the problem of slow write times is to decrease the actual time required to write each byte. Devices having byte-write times of 1 msec are widely available now, and parts with times of 500 μsec or less are currently being designed.

Xicor is not correct in stating that Seeq achieves these fast byte-write times by stressing the tunnel oxide to higher voltages. The internal programming voltage of Seeq's EEPROMs is in fact less than or equal to that of other manufacturers' parts. An improved tunnel-oxide layer, oxinitride, allows fast byte-write operations by improving the oxide's charge-transfer efficiency, thus allowing more charge to be forced in and out of the floating gate for any given voltage. This technique eliminates any trade-off of either data-retention time or endurance to achieve fast byte-write operations. Seeq currently supplies parts that have 1,000,000-cycle endurance and minimum data retention of 10 years.

For EEPROMs like Seeq's, which have highly stable thin oxides, a statistical approach to guarantee endurance is neither required nor desirable. Seeq has found that endurance failures are like any other semiconductor failure mechanism. They follow the bathtub curve, which consists of a period of relatively frequent infant failures, then a long period at a low failure rate, and finally, a period of increasing failure rates ("wear-out"). Because the period of low failure rate is on the order of millions of cycles for Seeq's parts, the firm guarantees the endurance of each part it ships by cycling the part thousands of times; this process eliminates infant failures without significantly reducing the useful life of the part. A statistical approach would be necessary only if the ends of the bathtub were close together.

The author is the strategic marketing manager for Seeq Technology Inc, San Jose, CA.



***Raising the programming voltage** isn't the only way to speed up EEPROM programming. Seeq's oxynitride dielectric passes more current at a given programming voltage than do conventional oxide dielectrics. Hence, the firm's parts program quickly without overstressing the dielectric.*

Exel: Future holds additional features

Steven Grossman, *Exel*

Exel agrees with Xicor that there should be a standard feature set for EEPROMs. But besides making devices that largely share Xicor's feature set, Exel makes devices that have additional features.

Xicor mentions Exel's XL48C64 8k×8 CMOS device briefly and credits that unit with futuristic features. The one feature specifically mentioned is a software-controlled mechanism for false-write protection. Other features included on this CMOS device are a 32-byte page mode that does not have a preset page-load window, a 5V chip-erase function that cannot be accidentally activated, and a fast-write mode that cuts write time in half when the bytes to be written have been erased previously. The XL48C64 is the industry's first CMOS 64k-bit EEPROM.

Exel has also developed another family of EEPROMs that is not mentioned in Xicor's article. The XL46C16 is a 5-nsec 2k×8 CMOS EEPROM, and the XL46C32 is a 7-nsec 4k×8 CMOS EEPROM. Both these devices look like bipolar PROMs. Exel's high-speed CMOS EEPROMs offer lower power dissipation and in-system reprogrammability. Exel tests all the devices leaving the factory for programmability.

The author is the memory product marketing manager for Exel, San Jose, CA.

feature allows the external power-up/power-down circuitry to provide either a high or a low signal to prevent write operations. (In a power transition where V_{CC} is not at a valid level, it's usually easier to hold a signal at ground than it is to hold a signal at a high level.)

Data needs protecting during power cycles

The 64k-bit EEPROMs also feature an on-chip V_{CC} sense function, which disables a write operation if V_{CC} is below a certain level. Standardization on this set point has not yet occurred; currently available products offer voltages such as 3.0, 3.75, and 4.25V. The desired trip point is application dependent; a system using CMOS logic, for instance, can maintain valid levels that are much lower than those of NMOS or TTL devices. Xicor's X2864A features a user-programmable V_{CC} sense capability that lets you set the trip point anywhere from 3 to 6V. But even though these features exist on the EEPROMs, you must take care when designing the system to ensure that inadvertent write operations cannot take place. After all, the primary application problem with 5V-programmable nonvolatile memories is that the systems they're used in don't include enough protection for the nonvolatile data.

Exel device hints at future trends

The Exel 48C64 includes a feature that hints at one direction EEPROMs might take. The Exel device uses pin 1 as an access-control line to an internal register called the control, or status, word.

One of the things this control word does is to enable a software write-protection scheme. With this scheme, setting an internal bit enables write operations; clearing the bit disables them. Because the device powers up in a disabled state, it's not possible to perform an inadvertent write operation on power-up. The system need only reset this bit before power-down to ensure that writes are not possible during power-down. This software write-protection scheme will no doubt find its way onto most manufacturers' new EEPROMs.

Other firms will probably implement the scheme differently, however. Like the Ready/$\overline{\text{Busy}}$ scheme, Exel's scheme requires that pin 1 be used for a function other than address line A_{14}, so devices with capacities greater than 64k bits would have to have more than 28 pins to use this scheme. A more desirable approach would be a software-access method like the one being developed by Xicor, which will introduce the scheme this year. Like the $\overline{\text{Data}}$-polling and page-mode methods, the software-access method will require no additional hardware or pins but will place many functions, such as software write protection, under software control.

But Exel hasn't ignored the problem of upward compatibility. To compensate for not having pin 1 available for address-line use, the firm uses some of the bits in the 48C64's control register as page or bank designators. Because the memory is divided into pages, a 28-pin device could provide 256k bits of capacity even though pin 1 is occupied. Although this approach is inevitable at high densities, a 256k-bit device is not dense enough to warrant it. Above the 256k-bit level

Manufacturers have incorporated the page-mode-write mode in the new generation of EEPROMs both to benefit users and to reduce EEPROM test time.

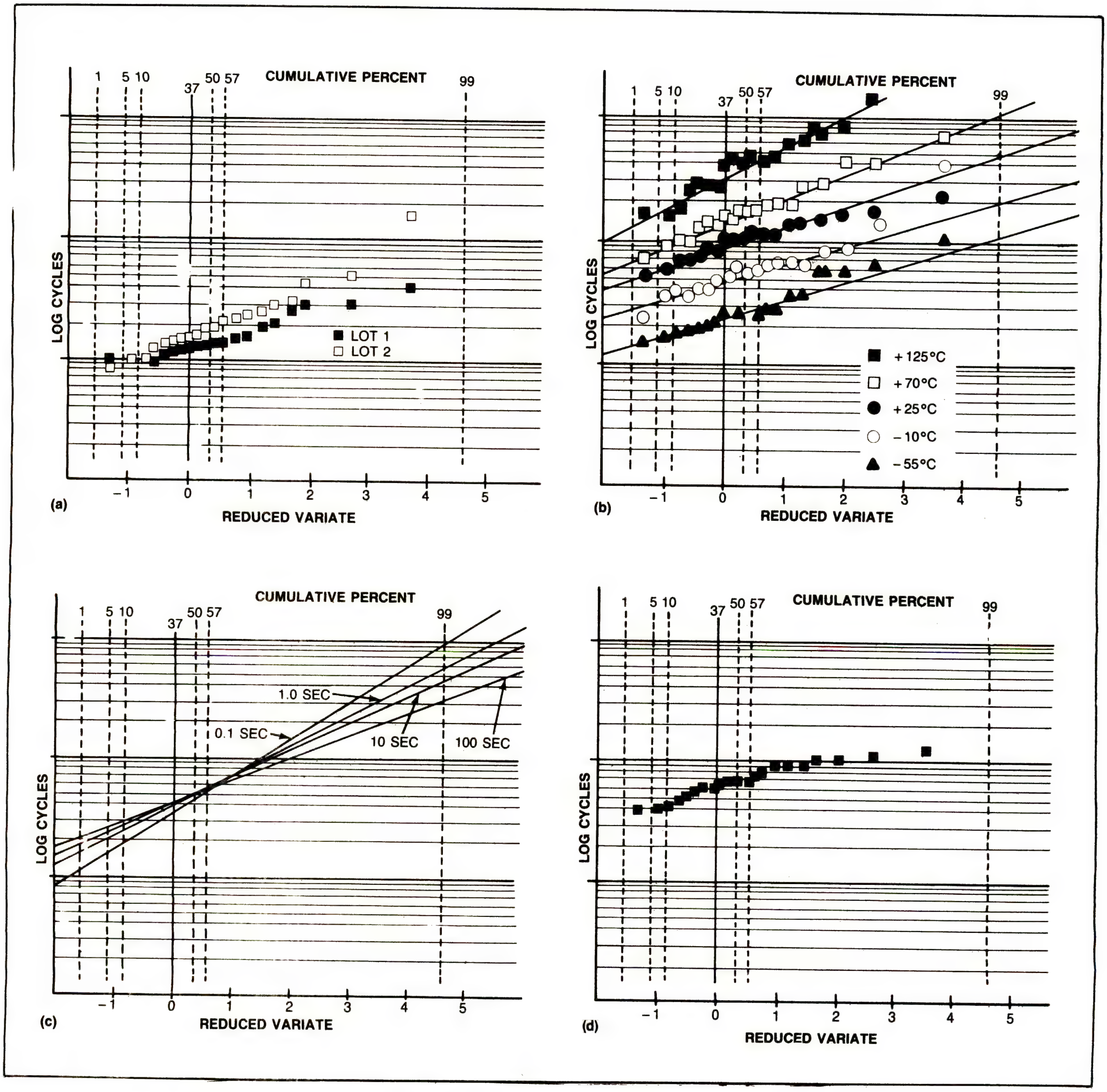


Fig 3—An extreme-value plot normalized over a sample lot of NOVRAMs (a) lets you compare the endurance of different lots. Such plots also help you to determine environmental effects on endurance. Part b shows that lengthening the write cycle increases endurance, and c shows that increasing temperature increases endurance. Part d represents EEPROM performance.

(especially at the 1M-bit level), a segmented approach makes more sense because it's undesirable in many applications to have so much directly addressed space occupied by EEPROM, even if you needed a lot of mass storage. You can expect that as EEPROM capacities increase, device organization will go from a linear-addressing scheme to a block-oriented approach.

Besides dealing with the inadvertent-write problem and the upward-compatibility issues it entails, EE-PROM makers must resolve one more data-corruption

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Manufacturers are making devices easier to test with mass-mode programming, in which a single command can set a device to all ones or all zeros.

issue, that of power loss during a write cycle, which could prevent completion of the write operation. Not only might the cycle be interrupted, but the data in the byte selected for the write operation might be lost. Xicor, for one, is investigating an uninterruptible-write-cycle function that would alleviate this problem.

Endurance specs must be standardized

Finally, the EEPROM industry needs an endurance standard, a standard for both specs and device testing. When you buy a device specified for 10,000 or 1,000,000 write cycles, you should know exactly what you're getting. Test conditions and methods must be standardized so that you can make accurate calculations of your designs' failure rates. You must be able to calculate how an EEPROM's endurance will affect your reliability analysis. Xicor has published much data on a new method for characterizing endurance, and it appears that other manufacturers may follow suit.

When determining the reliability of nonvolatile memories, you have to consider two main factors: data retention and endurance. Regarding data retention, note that virtually all of the current nonvolatile technologies have achieved significant levels of data retention —some predicted MTBFs are in excess of 1,000,000 years for data retention at 125°C.

Endurance, you will recall, describes the number of times that data can be changed before a failure occurs. For a nonvolatile array, endurance is the number of data-change cycles that take place in an entire array before the first error appears. Engineers using nonvolatile arrays are more concerned with the occurrence of the first error in the device than they are with the expected endurance of a typical bit in the array. In a wafer lot, endurance is a statistical description of a lowest or highest characteristic from a fixed set of possible values (arising from the fixed number of memory cells on the chip) and has the form of an extreme-value distribution. Xicor's "Reliability Report #RR504" contains more information about endurance.

Fig 3a shows a typical extreme-value distribution plot for endurance. The vertical axis is the base-10 logarithm of the data-changing cycles of the least reliable bit of a representative number of devices in a particular lot. The horizontal axis is a mathematical transformation of the rank of each device in terms of its endurance. This can be expressed as the fraction of the lot whose endurance is lower than a given endurance (as shown on the upper edge of the plot). The graph shows the endurance of two different lots of nonvolatile RAMs, both of which can be guaranteed to have 10,000 data changes for any bit in a device at the specified test conditions. The single part, in each lot, that has less than a 10,000-cycle endurance represents less than 5% of the lot under specific test conditions. (To include the effects of all permissible operating conditions, Xicor specs its standard NOVRAMs for 1000 cycles; **Fig 3's** plots were measured under conditions that permit 10,000 cycles.) **Fig 3d** shows typical endurance measurements for Xicor's EEPROMs, indicating an average endurance in excess of 600,000 cycles.

This analysis of the endurance of nonvolatile memories has provided a means of correlating different device lots. Not only does this help users to compare different suppliers, but it's useful in determining the effect of external conditions on the endurance of a lot of devices.

How EEPROMS fail

It's important to know how endurance failure, which can be caused by external conditions, occurs. In order for a certain value to be stored in a nonvolatile bit, electrons are either transferred to or from an isolated section, such as a floating gate, of the circuit. The electrons must be transferred through the dielectric by using a high electric field applied across the dielectric. During this transfer, a small number of electrons passing through the dielectric become trapped. These trapped electrons impart a negative charge to the dielectric, and, as the memory continues to be cycled, this negative charge counteracts the electric field that's applied to transfer electrons. When the charge of the trapped electrons becomes sufficiently high, electrons can no longer be transferred through the dielectric; the memory bit has reached its endurance limit.

After a time, the trapped electrons will tend to relax, so the dielectric's electric charge will be more evenly distributed. This characteristic of the trap-up phenomenon would give a device a higher endurance limit if the amount of time betwen each bit cycle were increased. It was difficult to check this hypothesis before extreme-value distribution was used in endurance analysis: There was no means of determining the endurance of a control lot versus that of an experimental one.

EEPROM endurance depends on environment

Fig 3b shows the effect of cycling rate on the endurance of devices from the same lot. As the amount of time between bit cycles is increased, there is a definite improvement in endurance at the low-endurance end of

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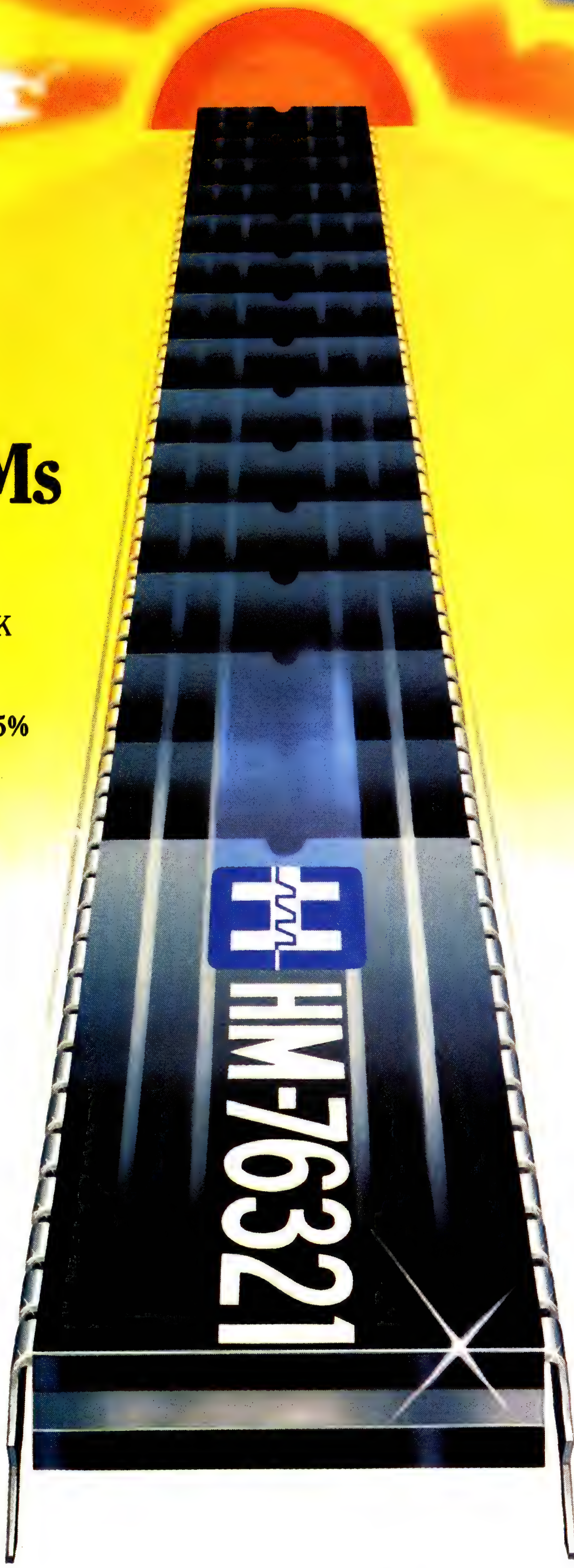

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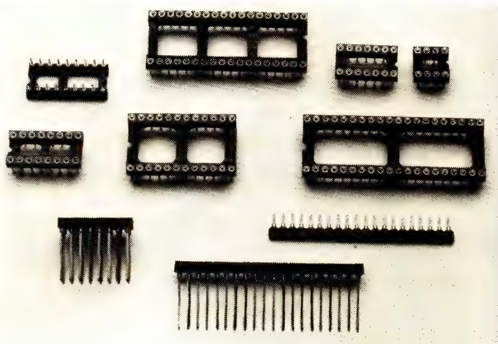

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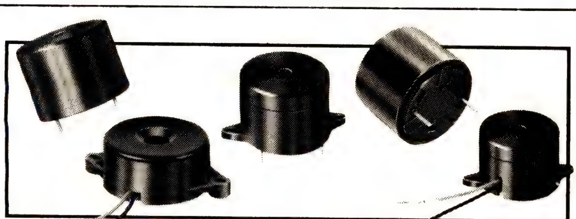

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EEPROM manufacturers must resolve the problem of power-up data corruption.

the distribution. This is important in many applications because the rate at which a typical system cycles each bit is even slower than the slowest practical rate of 100 sec per cycle (**Fig 3b**). In order to minimize test time, manufacturers usually determine guaranteed endurance values at the fastest rate at which the test system can operate. Note that an increase in the cycle period from 0.1 to 100 sec can increase the endurance of the worst bit at the 5% cumulative-failure point by a factor of 2 to 3. More important, the fraction of devices failing at a given value of endurance decreases by more than an order of magnitude.

Another external condition which should affect the rate at which the electrons can escape the trap is temperature. As the ambient temperature of the dielectric is increased, the electrons can escape more easily. **Fig 3c** is a graph of the endurance for various devices from the same lot, which were cycled at temperatures ranging from −55°C to +125°C; the endurance of the devices increases as the temperature is increased. More precisely, endurance doubles every time the temperature increases by 50°C.

The practical application of extreme-value distribution to endurance lets you predict statistically a failure rate for a given device at a given number of cycles. Typical chip temperature in a system averages 50°C, and the rate at which each bit in the nonvolatile array is changed is greater than a few minutes per bit. Xicor's definition of device endurance implies that the rest of the lot will exhibit a 5% failure rate at 25°C (room temperature); increasing operational temperature decreases the cumulative failure rate to 0.03%. Furthermore, note that the firm characterized the devices at the rate of 0.1 sec per cycle. Increasing the cycle period to greater than 1 minute further decreases the cumulative failure rate to 0.001%. **EDN**

Author's biography

Richard V Orlando is product marketing manager for Xicor Inc, where he is responsible for strategic and technical marketing for all products. He was previously employed by the AMI Microprocessor and Microcomputer Group. A member of the IEEE, he received a BSCSE from the University of Massachusetts. His hobbies include personal computers, computer architecture, and microprocessor applications.

Article Interest Quotient (Circle One)
High 476 Medium 477 Low 478

GRIMES SWITCHES: YANKEE INGENUITY AT AN IMPORT PRICE

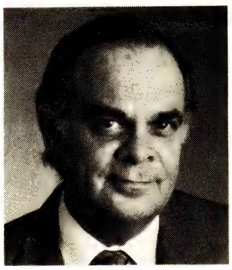
BREA, CA – Grimes Company may be the best kept secret in the electronics industry.

For years they have been the exclusive supplier of low-profile keyboard switches to one of the most successful personal computer manufacturers in the industry.

Aiming to produce the most inexpensive, high-quality American-made switch available, Grimes spent over $2 million perfecting the high-volume automated assembly equipment that can do it. These machines are capable of producing over 2.8 million switches per week.

This year the company tripled its total gross sales over last year's figures. Yet hardly anyone has heard of them.

Recently Grimes' management decided to let their secret out. And the industry may never be the same again.


John Gunnoe

Marketing and Sales Vice President John Gunnoe explained that after years of supplying one manufacturer with switches, joy sticks and monitor stands, Grimes felt it was time to expand their marketing base.

"We enjoy a very healthy relationship with that one manufacturer," Gunnoe said. "But you never want to put all your eggs in one basket."

Gunnoe declined to reveal the identity of that major manufacturer, but he did say "you can't turn around without seeing one of the ads in a magazine or on television."

As part of their aggressive new marketing strategy, Grimes Company will promote the advantages of their low-cost American-made switch over foreign competitors.

"Grimes' American-made switches cost less because of our high volume automated manufacturing process," said Operations Vice President Bruce Shepard.

"And American-made means immediate delivery, immediate credit and no overseas freight charges," he added.

Shepard was quick to point out that Grimes didn't sacrifice high quality for their low price. Their switches are proven reliable for over 10 million cycles; most switches are good for only 100,000 cycles.

After establishing their presence in the electronics market, Grimes plans to continue researching and developing new products for the personal computer field. Recently Grimes Company purchased Track House, maker of the programmable IIe Tender keypad for the Apple IIe.

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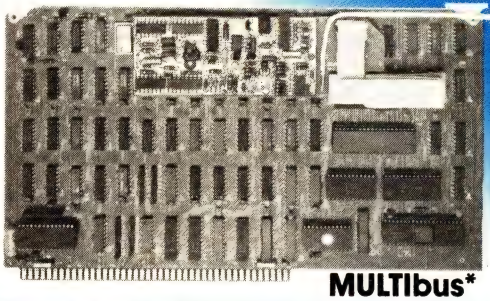
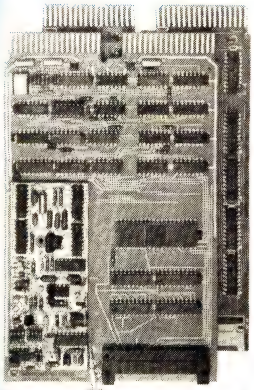
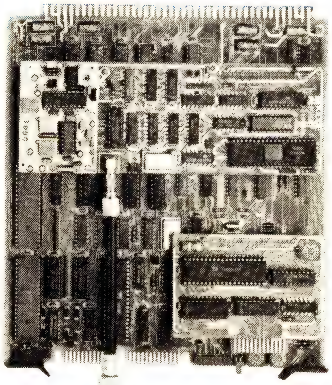


MULTIbus*

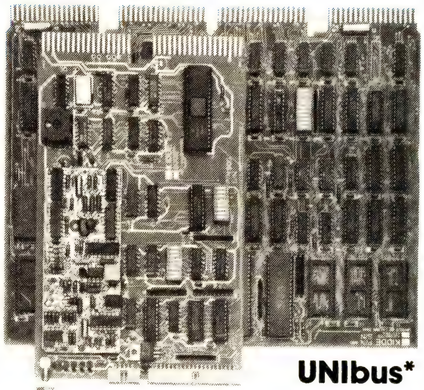
BUS ARCHITECTURE



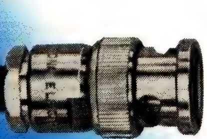
Q-bus*



IEEE-488



UNIbus*



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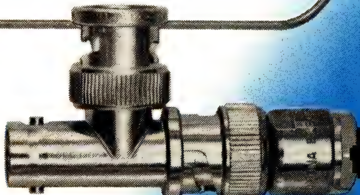

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CIRCLE NO 110

NAPLPS standard defines graphics and text communications

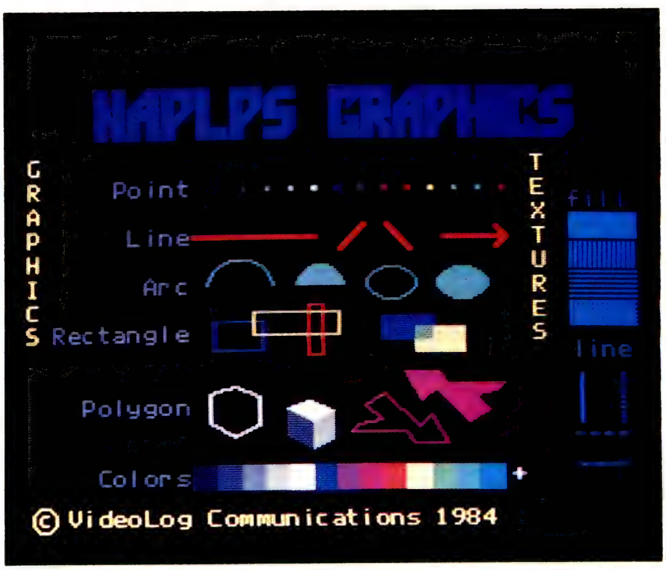
The continuing evolution of display-presentation technology is evidenced by the emergence of NAPLPS. This standard for communications provides a formal protocol that facilitates the transmission of text and graphics characters.

Gary L Holland, *Videolog Communications*

The North American Presentation Level Protocol Syntax (NAPLPS), approved by major standards organizations in 1983, provides a communication standard for the exchange of textual and graphical information among computers. It's particularly well suited for encoding the graphical data in a highly portable and resolution-independent form.

ANSI Standard X3.110-1983 "describes the formats, rules and procedures for the encoding of alphanumeric text and pictorial information," which can then be transmitted via the most appropriate medium for an application (telephone, modem, network, terminal mechanisms, FM-sideband radio, or broadcast television). This transmission-medium independence is one of NAPLPS's most important features: It will allow painless migration to new transmission technologies as they are introduced—so there's no built-in obsolescence.

The ASCII communications protocol is the closest thing there is to a universal standard for sending data via telephone lines. Though ASCII might be adequate for most text-only applications, it's unacceptable for computer graphics because its format incorporates only alphanumeric codes. NAPLPS, however, which was voted into its present form by ANSI and the Canadian Standards Association in November 1983, embraces ASCII and offers an easy, fast, and effective way of dealing with communications-based graphics.



***Using the NAPLPS standard,** you can simply outline the shapes surrounding an area, such as an arc, a polygon, or a rectangle, or you can fill them in with a textured pattern.*

NAPLPS is particularly well suited for encoding graphic data in a highly portable and resolution-independent form.

NAPLPS offers special visual effects and capabilities, *such as color mapping, text character sizing, text rotation, and the ability to form text paths.*

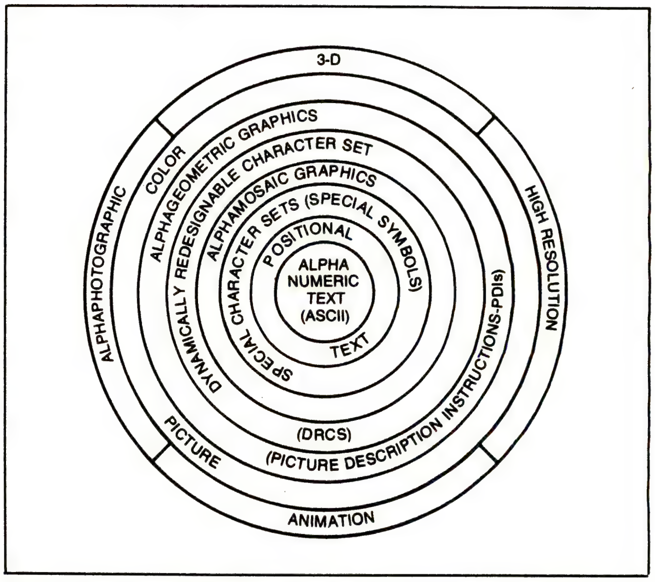


Fig 1—A layered capabilities model *for text and graphics display standards expands with each advance in display technology.*

In simplified terms, NAPLPS is a superset of ASCII (ANSI X3.4-1977); it enhances the alpanumeric text capabilities of ASCII through the use of extensions. This allows more complex display capabilities to be incorporated into the same visual image, so that words and pictures can appear on the same screen. The extensions are accomplished primarily through the use of op codes that tell the terminal which of several predefined or variable (dynamically redefinable) character sets to use, which graphic shape from a repertory of simple geometric primitives (point, line, arc, polygon, etc) to draw, what kind of environment to use to paint the graphics and text on the screen (color, blinking, stroke width, textures, etc), and where to draw them.

NAPLPS is a comparative newborn among standards; to understand the current status of the protocol, you should review the circumstances leading to its development, which involves a discussion of CRT evolution.

The evolution of display technologies

You could view the evolution of the CRT and its display capabilities as an expanding sphere, with each new development adding a layer of new features (**Fig 1**). Two factors that contributed to the increased use of the CRT were the growth of timesharing computing and the decreasing unit cost of both memory and computing power. The initially crude placement of dots

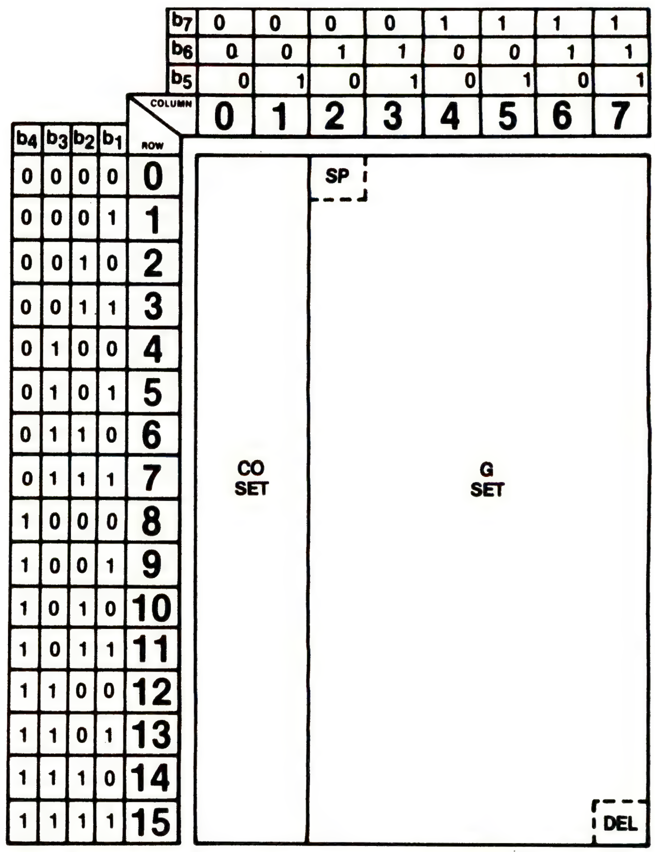


Fig 2—This 7-bit in-use table *provides 128 NAPLPS code positions arranged into one 2×16-position command set (the C set) and one 6×16-character argument set (the G set).*

and lines on a CRT evolved into the orderly arrangement of those dots and lines to form the shapes of alphanumeric text characters. Text that was restricted to top-to-bottom, left-to-right display gave way to the development of positionally variable text capabilities.

Tektronix's introduction of the direct-view storage-tube monitor (611 DVST) represented a significant divergence of display technology; the device was directed toward computer graphics applications instead of the text-based applications of early CRTs. Technological areas were never clearly separated, however: The graphics world needed text, and the text world increasingly found areas where graphics capability was beneficial.

By expanding character sets to include scientific symbols, other special symbols, and graphic shapes, designers gave nonintelligent text-only CRTs new display capabilities, expanding their usefulness into quasigraphic areas. Then terminal designers added alphamosaic graphics, which display the mosaic patterns possible in a 2×3 matrix that occupies the same space as a text character. Alphamosaic graphics gave terminals a degree of pictorial capability, but these graphics had unmistakably mosaic characteristics.

An even greater degree of graphic sophistication was provided by the development of the dynamically redefinable character set (DRCS). When you use DRCS techniques, the terminal is equipped with a buffer of blank character cells of a certain pixel density. The host computer tells the terminal which pixels in a given DRCS character to switch on, thus forming whatever shape is required—within the limits of the character-cell pixel matrix.

Each increase in display functionality called for greater levels of terminal intelligence in the form of customized hardware, software, and firmware; larger μPs; and more memory. The recent incorporation of alphageometric graphic and color capabilities into more general-purpose terminals and personal computers was, in fact, the next logical step in the development of the display screen, bringing the capabilities of graphics and text terminals together. And **Fig 1**'s model of layered capabilities is by no means complete. New capabilities will go beyond 3-dimensional, animation, and alphaphotographics technologies.

Graphics and text must coexist

Some observers, like Sam Berkman of AT&T Information Services (a key participant in the development of the PLPS standard), suggest that NAPLPS must supplant ASCII as the dominant form of computer interaction, because "the text-only capabilities of ASCII are not up to the task of coping with the volumes and complexities of today's information-handling requirements. Both graphics and text are required, and NAPLPS is superbly efficient at providing both."

In a 7-bit environment, NAPLPS uses a 128-code-position table arranged into one 2×16-position command set (the C set) and one 6×16-character argument set (the G set) (**Fig 2**). The C set contains two sets of control sequences, designated C0 and C1, while the G set incorporates six different sets of display capabilities. The control-sequence sets also contain op codes for transmission flow control (X-on/X-off, etc) and some graphics environment controls such as cursor on/off/flashing/positioning and predefined text sizes. The different values loaded into the code-position table and activated are grouped into related sets. Special escape sequences are used to swap the required set into the active or in-use table area prior to its access.

These escape sequences take the form ESC-I-F, where I is the intermediate character and F is the final

INTERMEDIATE (I) CHARACTERS FOR DESIGNATION SEQUENCES

INTERMEDIATE CHARACTER	SET TO BE DESIGNATED
2/1	C0
2/2	C1
2/8	G0
2/9	G1
2/10	G2
2/11	G3

FINAL (F) CHARACTERS FOR DESIGNATION SEQUENCES OF G-SETS

FINAL CHARACTER	G SET
4/2	PRIMARY CHARACTER SET
7/12	SUPPLEMENTARY CHARACTER SET
5/7	PICTURE DESCRIPTION INSTRUCTION SET
7/13	MOSAIC SET
7/10	MACRO SET
7/11	DYNAMICALLY REDEFINABLE CHARACTER SET

*Fig 3—**These designation sequences are key factors** in controlling the NAPLPS graphics environment. The intermediate characters determine which C or G set will be changed (redesignated). The final characters determine which set from the G set's repertory will be selected.*

NAPLPS allows more complex display capabilities to be incorporated into a visual image, so that words and pictures can appear on the same screen.

character. The intermediate character determines which C or G set will be changed (redesignated). The final character determines which set from the G set's repertory will be selected. **Fig 3** shows the intermediate and final designation sequences.

For more economy in storage and transmission, NAPLPS supports the 8-bit environment displayed in **Fig 4.** In an 8-bit NAPLPS system, there are two in-use C and two in-use G sets. The graphics builder shifts these sets in and out of the active table much less frequently, saving the overhead of the sequences needed to designate the shifting.

Characters, graphics, and PDIs

To the traditional 94-character ASCII alphanumeric text set **(Fig 5)**, NAPLPS adds two other fixed character sets: a supplemental set of 94 special symbols, international accents, and text characters **(Fig 6)**, and the 65 mosaic patterns possible in a 2×3 matrix assigned to a character cell **(Fig 7).** The host computer, through a NAPLPS terminal, can define as many as 96 macro sequences. You can also define as many as 96 characters to form the dynamically redefinable character set.

The graphics part of the standard is based on a set of five geometric primitives—points, lines, arcs, rectangles, and polygons. These primitives combine to create the graphics part of a NAPLPS image. **Fig 8** displays the sixth G set, which includes picture description instructions (PDIs). The PDIs are a collection of 32 op codes that you invoke to specify the shape and placement of a graphics primitive on the screen. This G set

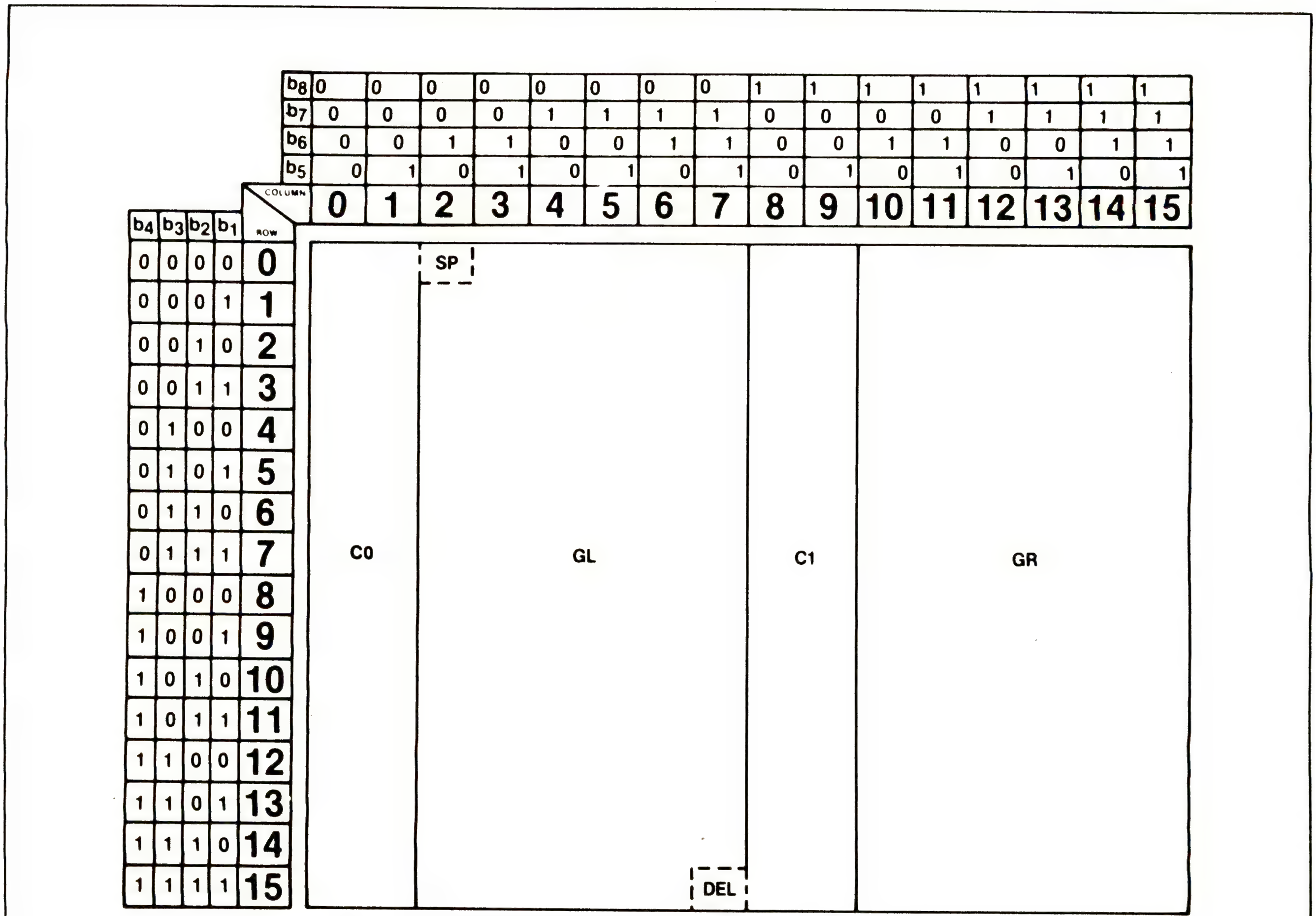


Fig 4—Two in-use C and two in-use G sets *are used in an 8-bit NAPLPS system. Because there are two C and two G sets, the graphics builder doesn't need to shift frequently, eliminating keystrokes or other sequences needed to designate the shifting.*

b7					0	0	1	1	1	1
b6					1	1	0	0	1	1
b5					0	1	0	1	0	1
b4	b3	b2	b1	ROW \ COLUMN	2 (10)	3 (11)	4 (12)	5 (13)	6 (14)	7 (15)
0	0	0	0	0		0	@	P	`	p
0	0	0	1	1	!	1	A	Q	a	q
0	0	1	0	2	"	2	B	R	b	r
0	0	1	1	3	#	3	C	S	c	s
0	1	0	0	4	$	4	D	T	d	t
0	1	0	1	5	%	5	E	U	e	u
0	1	1	0	6	&	6	F	V	f	v
0	1	1	1	7	'	7	G	W	g	w
1	0	0	0	8	(	8	H	X	h	x
1	0	0	1	9	)	9	I	Y	i	y
1	0	1	0	10	*	:	J	Z	j	z
1	0	1	1	11	+	;	K	[	k	{
1	1	0	0	12	,	<	L	\	l	|
1	1	0	1	13	–	=	M	]	m	}
1	1	1	0	14	.	>	N	^	n	~
1	1	1	1	15	/	?	O	_	o	

Fig 5—The traditional 94-character ASCII alphanumeric set is defined by NAPLPS according to this 7-bit primary character G set.

b7					0	0	1	1	1	1
b6					1	1	0	0	1	1
b5					0	1	0	1	0	1
b4	b3	b2	b1	ROW \ COLUMN	2 (10)	3 (11)	4 (12)	5 (13)	6 (14)	7 (15)
0	0	0	0	0		°	⁻	—	Ω	ĸ
0	0	0	1	1	¡	±	`	¹	Æ	æ
0	0	1	0	2	¢	²	´	®	Đ	đ
0	0	1	1	3	£	³	^	©	ª	ð
0	1	0	0	4	$	×	~	™	Ħ	ħ
0	1	0	1	5	¥	µ	¯	♪	⊞	ı
0	1	1	0	6	#	¶	˘	⊟	Ĳ	ĳ
0	1	1	1	7	§	·	˙	◫	Ŀ	ŀ
1	0	0	0	8	¤	÷	¨	⧄	Ł	ł
1	0	0	1	9	‘	’	/	⧅	Ø	ø
1	0	1	0	10	“	”	°	◪	Œ	œ
1	0	1	1	11	«	»	¸	◩	º	ß
1	1	0	0	12	←	¼	▯	⅛	Þ	þ
1	1	0	1	13	↑	½	˝	⅜	Ŧ	
1	1	1	0	14	→	¾	˛	⅝	Ŋ	ŋ
1	1	1	1	15	↓	¿	ˇ	⅞	ŉ	

Fig 6—This supplementary character set of 94 special symbols, international accents, and text characters is another standard NAPLPS G set.

also contains a few environmental characteristics such as Color and Blink commands.

A PDI takes the form of a 1-byte op code followed by a variable number of operands whose size and interpretation vary according to the op code, the current drawing environment, and the display capabilities of the device that receives them. For a graphic shape, the operands are the X-Y coordinate locations on the screen where the shape should be deposited, or they're displacements from where the previous drawing instruction left the drawing point or cursor. For an environmental PDI like Set Color, the operand bytes specify the amounts of red, blue, and green to mix into the required shade.

Use of this coding scheme makes NAPLPS very byte-efficient. For example, a line specification takes only seven bytes, regardless of its length and orientation—one byte for the line PDI and two 3-byte X-Y coordinates for the line's end points. Similarly, a rectangle is seven bytes, but the X-Y coordinates are for the ends of either of the rectangle's diagonals. Circles are a special form of the Arc PDI, which requires only 10 bytes, regardless of its size. In this case, the arc's beginning and end points are the same, and the midpoint becomes the other end of the circle's diameter. Polygons are like connect-the-dot images; their shapes

New display capabilities of the CRT will go beyond 3-dimensional, animation, and alphaphotographics technologies.

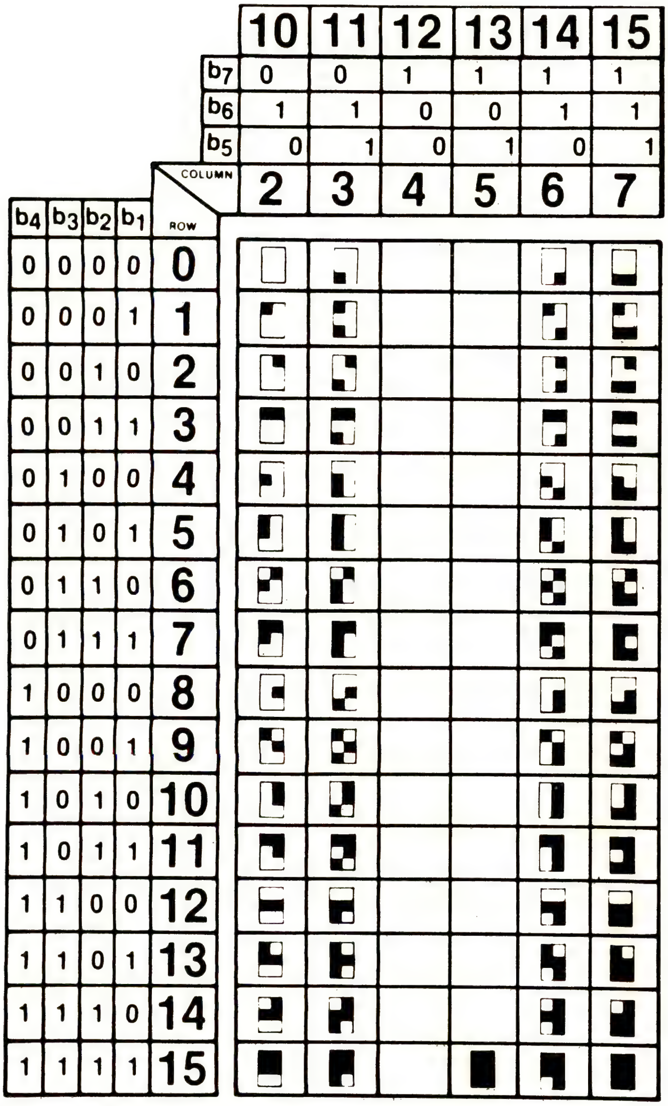


Fig 7—The 65 mosaic patterns possible in a 2×3 matrix are assigned under NAPLPS to character cells in the third G set.

					10	11	12	13	14	15
				b7	0	0	1	1	1	1
				b6	1	1	0	0	1	1
				b5	0	1	0	1	0	1
b4	b3	b2	b1	COLUMN / ROW	2	3	4	5	6	7
0	0	0	0	0	RESET	RECT (OUTLINED)	NUMERIC DATA			
0	0	0	1	1	DOMAIN	RECT (FILLED)				
0	0	1	0	2	TEXT	SET & RECT (OUTLINED)				
0	0	1	1	3	TEXTURE	SET & RECT (FILLED)				
0	1	0	0	4	POINT SET (ABS)	POLY (OUTLINED)				
0	1	0	1	5	POINT SET (REL)	POLY (FILLED)				
0	1	1	0	6	POINT (ABS)	SET & POLY (OUTLINED)				
0	1	1	1	7	POINT (REL)	SET & POLY (FILLED)				
1	0	0	0	8	LINE (ABS)	FIELD				
1	0	0	1	9	LINE (REL)	INCR POINT				
1	0	1	0	10	SET & LINE (ABS)	INCR LINE				
1	0	1	1	11	SET & LINE (REL)	INCR POLY (FILLED)				
1	1	0	0	12	ARC (OUTLINED)	SET COLOR				
1	1	0	1	13	ARC (FILLED)	WAIT				
1	1	1	0	14	SET & ARC (OUTLINED)	SELECT COLOR				
1	1	1	1	15	SET & ARC (FILLED)	BLINK				

Fig 8—The picture-description instructions (PDIs) in the G set form a collection of 32 op codes that you invoke to specify the shape and placement of a graphics primitive on the screen. The G set also contains a few environmental characteristics such as Color and Blink commands.

are defined by their vertices to a maximum of 256 coordinate triplets per polygon. Shapes that surround an area (arcs, polygons, and rectangles) can be rendered as outlines or they can be filled with textured patterns. Furthermore, lines and unfilled outline shapes can be drawn with four different line textures: solid, dotted, dot-dashed, and dashed.

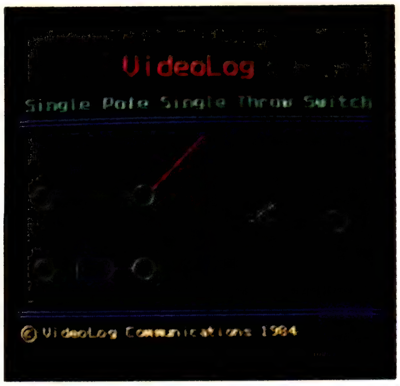
Compatibility through the unit screen

The concept of the unit screen is an important aspect of the NAPLPS standard and is fundamental to the standard's longevity. The X-Y coordinates specified in the PDI structure are expressed in terms of a square display area ranging from (0,0) in the lower left region to (1,1) in the upper right region. (Because most display devices have a visual area that's more rectangular, coordinates above 0.75 are typically not used, but they could be if some display technology or graphics application needed them.)

Because the interpretation of a NAPLPS data stream is left up to the device receiving it, the unit-screen concept lets devices of varying resolution display the same incoming image to their own limits of detail. For example, coordinates of (0.5,0.39) following a Point op

From code to graphics . . .

One of the best ways to confront NAPLPS is to see actually what bits and bytes are required to convey a given graphic image in the standard's own syntax. Videolog, a NAPLPS-based database for design engineers, provided the annotated listing of NAPLPS code, which was used in part to create this graphic image of a single-pole, single-throw switch.



ANNOTATED LISTING OF NAPLPS GRAPHICS

```
0e                               Shift to PDI set
3e 6c                            Set current drawing to red

2a 49 54 43 41 5c 5b             Line (x,y)=(80,99)-(27,99)
2a 52 41 53 49 5d 78             Line (x,y)=(130,139)-(95,104)
2a 40 5e 61 40 6e 51             Line (x,y)=(28,49)-(42,49)
2a 48 56 41 48 46 69             Line (x,y)=(80,49)-(69,49)
2a 48 66 49 50 46 59             Line (x,y)=(97,49)-(131,49)
2a 51 62 71 59 5a 41             Line (x,y)=(166,81)-(215,49)
24 4a 4e 59                      Move drawing point to (x,y)=(75,177)
22 40 40 40 4a 64                Set text size to 12 x 20 pixels

0f                               Shift to Primary Text Character Set

56 69 64 65 6f 4c 6f 67          "VideoLog"

0e                               Shift to PDI set

24 42 43 6d                      Move drawing point to (x,y)=(5,157)
22 40 40 40 49 44                Set text size to 8 x 12 pixels

3e 74                            Set current drawing color to green

2e 41 4c 5b 40 48 70 78 70 50    Circle with diameter (x,y)=(11,99)-(25,99)
2e 49 54 4b 40 48 70 78 70 50    Circle with diameter (x,y)=(81,99)-(95,99)
2e 40 4e 61 40 48 70 78 70 50    Circle with diameter (x,y)=(12,49)-(26,49)
2e 48 56 49 40 48 70 78 70 50    Circle with diameter (x,y)=(81,49)-(95,49)
2e 59 5a 51 40 48 70 78 70 50    Circle with diameter (x,y)=(218,81)-(232,81)
36 51 62 69 40 51 43 47 46 45    Polygon (x,y)=(165,81)-(181,92)-(181,81)

0f                               Shift to primary text character set

53 69 6e 67 6c 65 20             "Single "
50 6f 6c 65 20                   "Pole "
53 69 6e 67 6c 65 20             "Single "
54 68 72 6f 77 20                "Throw "
53 77 69 74 63 68                "Switch"

0e                               Shift to PDI set

3e 50                            Set current drawing color to medium gray

2a 42 43 40 5a 7b 78             Line (x,y) = (0,152)-(255,152)
2a 42 42 45 5a 7a 7d             Line (x,y) = (0,149)-(255,152)
2a 40 42 44 58 7a 7c             Line (x,y) = (0,20)-(255,152)
2a 40 42 41 58 7a 79             Line (x,y) = (0,17)-(255,152)
32 40 6f 58 47 56 62             Rectangle (x,y)=(43,56)-(63,42)
2e 40 7f 70 47 47 69 7f 7f 61    Arc (xy,)=(62,56)-(67,49),63,42)
23 42                            Dashed line texture
2a 50 46 61 52 41 63             Line (x,y)=(132,49)-(132,139)
3e 70                            Set current drawing color to yellow

1b 4c                            Set text size to Normal 40 characters/line
24 40 40 41                      Move current drawing point to (0,1)
23 40                            Solid line texture

0f                               Shift to primary character set

20 63 20                         " c "
56 69 64 65 6f 4c 6f 67 20       "VideoLog "
43 6f 6d 6d 75 6e 69 63 61       }"Communica"
74 69 6f 6e 73 20 31 39 38 34    "tions 1984"

0e                               Shift to PDI set

2e 40 40 5d 40 48 50 78 70 70    Circle Radius (x,y)=(3,5)-(13,5)
```

To the traditional 94-character ASCII set, NAPLPS adds 94 special symbols, international accents, and text characters as well as 65 mosaic patterns.

Three categories of graphics standards

Graphic standards fall into three general categories determined by the issues they focus upon: device (hardware) directed, program/application (software) directed, and inter/intra-system transfer directed.

Device-oriented standards are generally called virtual device interfaces (VDIs). VDIs provide standard input and output control sequences while maintaining a device-independent "front" for application software. New graphics-device markets would open up if software based on a VDI could be ported to wide varieties of hardware.

Software standards focus on allowing a graphics-application program to access standard functions for diverse input and output peripherals in a device-independent fashion. These standards include

- Graphics Kernel System (GKS)—a largely 2-dimensional standard, which originated in West Germany
- CORE—an older 2- and 3-dimensional standard introduced by ACM/Siggraph in 1977
- Programmers Minimal Interface to Graphics (PMIG)—a new subset of GKS
- Programmer's Hierarchical Interactive Graphics System (PHIGS)—a form of GKS that adds advanced capabilities, including 3-dimensional features.

Transfer/encoding standards consider the problems of communicating graphics between systems and components within a system. These standards include

- North American Presentation Level Protocol Syntax (NAPLPS)—a published standard
- Initial Graphics Exchange System (IGES), which represents and exchanges CAD/CAM-type graphic information
- Electronic Design Interchange Format (EDIF)—a common data-interchange format for electronic design proposed by a committee of university and commercial organizations active in CAD/CAM
- Virtual Device Metafile (VTM), which is still in drafting stages.

code would turn on the pixel at (128,100) on a monitor with 256×200 resolution, while a more sophisticated device with 1024×768 resolution would turn on the pixel at (512,300). NAPLPS's device-display independence is important for software writers, publishers, and database producers, who can build an image once and be assured that it can be used with a wide range of hardware with different visual-display characteristics and capabilities.

The NAPLPS visual environment

There are many NAPLPS commands that you can use to set up an environment within which you can draw an image on a screen, printer, or other output device. For example, you can use the Select Color PDI to establish that the next item drawn will be in a specific color. Then you can use Logical Pel to set the brush width (eg, 2×2 pixels), and you can issue the Texture PDI to specify whether the lines and shapes will be solid, dotted, or textured in some other fashion.

This process continues until the graphics state is sufficiently defined, either explicitly or through dependence on the default state of various NAPLPS options. Then any shape you draw or text you write will appear according to whatever set of NAPLPS characteristics is currently active. The NAPLPS default environment specifications are as follows:

- Full-screen text size is 20 lines×40 characters per line.
- Text runs left to right from top left to bottom right.
- Text orientation is normal.
- Brush size is 1×1 pixels on a 200×256-pixel displayable grid.
- Lines are solid.
- Shapes that enclose areas such as rectangles and polygons are solidly filled with the current drawing color.
- The 16 entries of the color map are set up with black, white, six shades of gray, and eight other colors evenly spaced about the color wheel.
- The initial drawing color is white, and there is no

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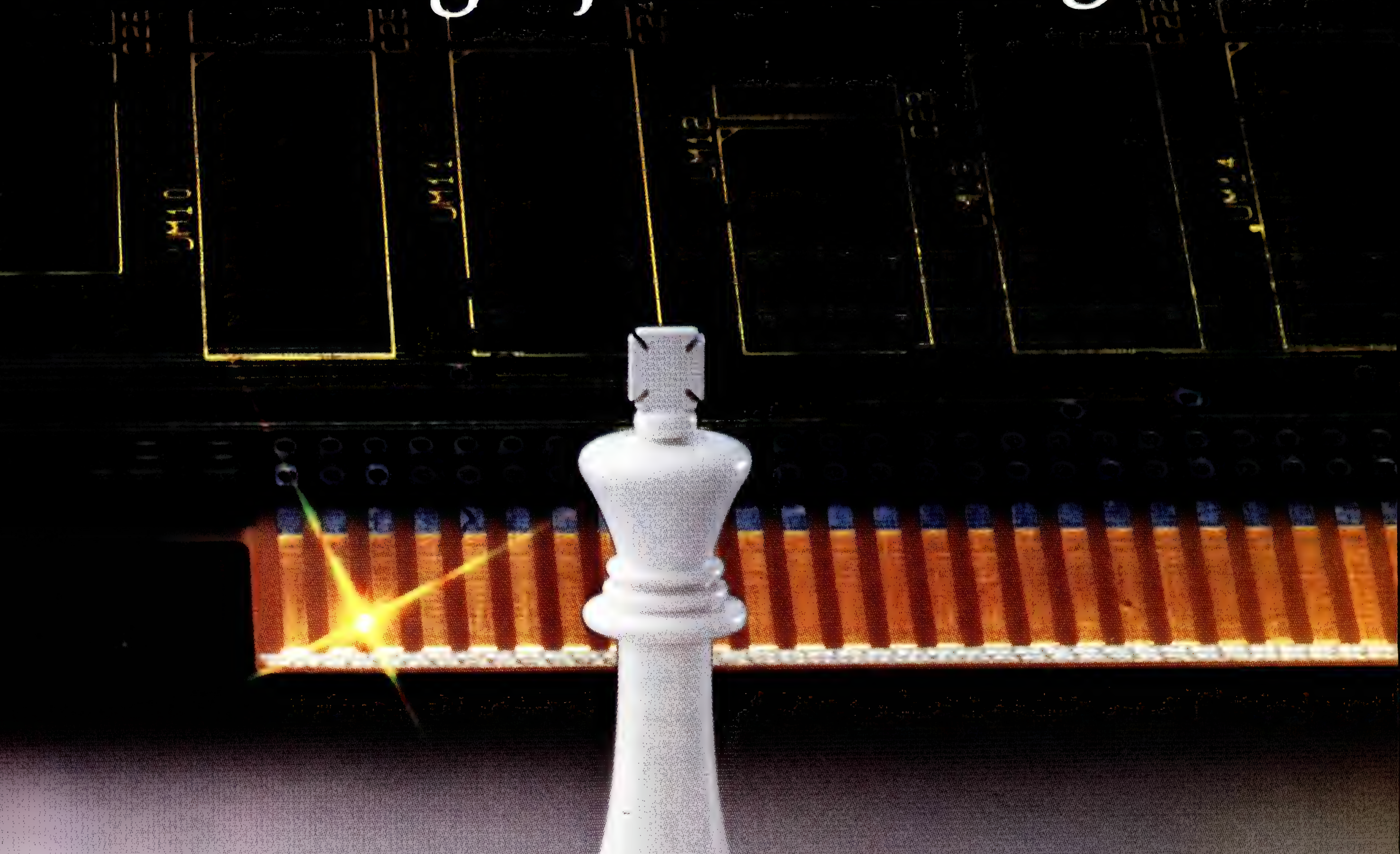

The rules keep changing. Today's rapidly advancing technology is bringing the need for increasingly dense and sophisticated interconnect systems. Forward thinking electronic industry leaders realize that staying ahead is no easy game. The stakes are too high in personnel and equipment.

These key players know that becoming partners with HADCO is the best move. HADCO will invest $30 million this year to be at the forefront of interconnect technology.

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CIRCLE NO 112

NAPLPS is very byte-efficient; a line specification takes only seven bytes, regardless of its length and orientation.

active background color.

A variety of special visual effects can be displayed on a device implementing NAPLPS and rendered by the following instructions:

- Logical Pel—This instruction allows specification of a variable-width brush for the geometric PDIs.
- Color Mapping—This command provides for 16 simultaneous colors on the screen, although extension to more than 16 color-map entries is possible. The size of the color palette from which the color-map entries may be set is an implementation-dependent function of the number of bits of resolution in each color-map entry. Although the upper limit is 16 bits of precision—so there are 65,536 available colors—current implementations are in the 9- to 11-bit range, yielding 512 to 4096 colors.
- Text Character Size—This instruction is entirely variable because the unit-screen coordinate schema is used to express the width (dx) and height (dy) of characters. Proportional spacing of letters is supported, as are spaces of 1, 1.25, and 1.5 times the available character width.
- Text Path—Characters can run left, right, up, or down.
- Text Rotation—The system rotates a defined character field 90°, 180°, or 270° counterclockwise from the horizontal, using the lower left corner of the character-field area as a display reference point.
- Blink—You can set up color-map entries to change their values according to variable timing parameters. As many as 16 blinking processes can be linked to yield effects ranging from simple timed flashing to sophisticated animation.
- Field—This PDI provides a simple windowing capability to specify text margins and areas for block-mode transmission interactions between the terminal user and the host system.

Videotex and teletext—the first arena

Most of the attention NAPLPS has received thus far has been in connection with its use in information service activities, which are generally divided into two areas—videotex and teletext.

Videotex is an interactive communications medium through which users receive information and services electronically. It's really not much more than a conventional timesharing and database service with added graphics elements and a higher degree of user-interface simplification. This simplification is achieved through the extensive use of menus and elementary inquiry procedures. Because the user's terminal is typically connected to the central computer by telephone via a modem, the size of the database and diversity of the service is limited only by the central system operator's investment in disk space and CPU power.

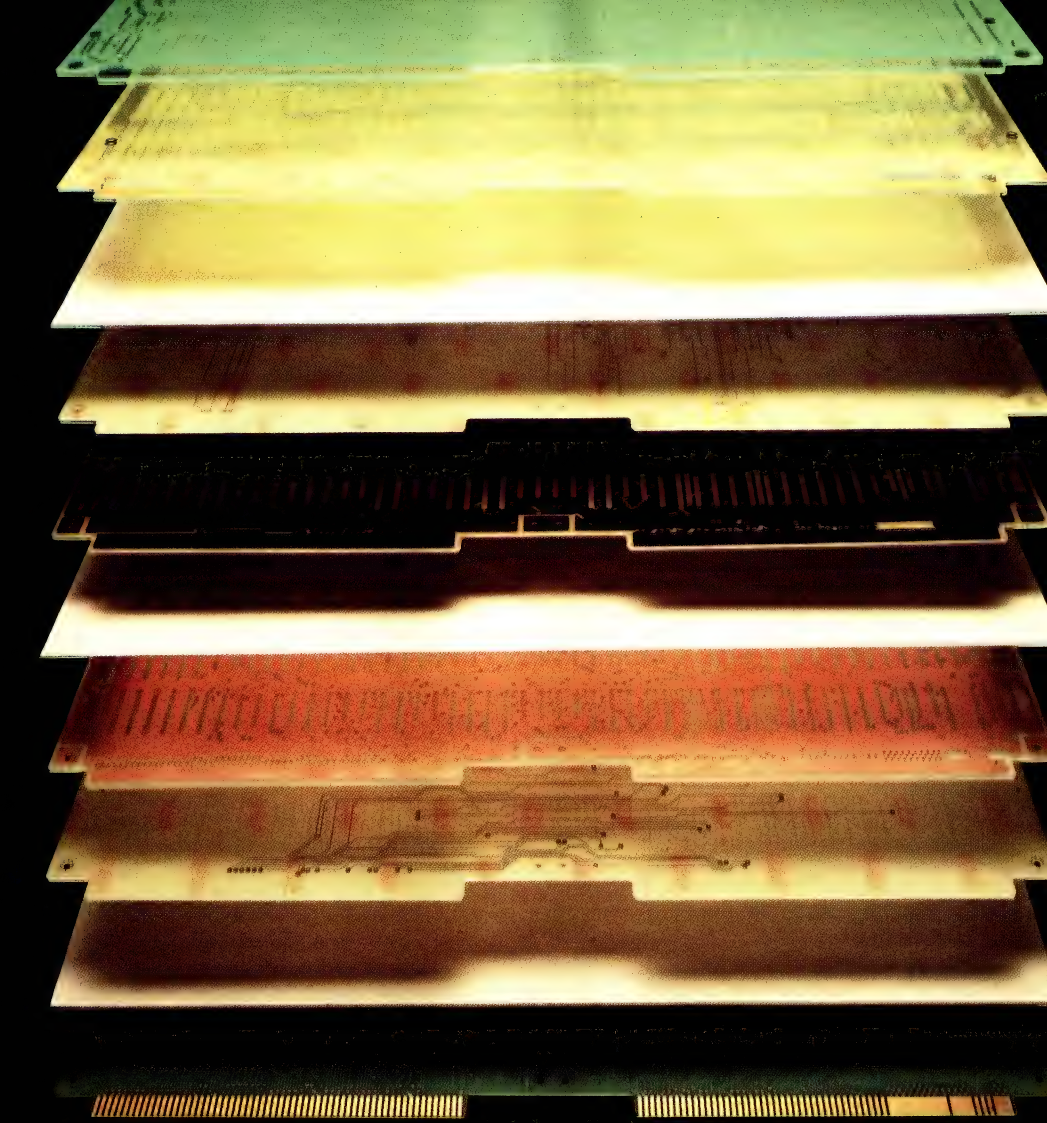
Teletext is the 1-way transmission of graphics and text information using broadcast (or cable) TV technology. In teletext, the digitally formatted NAPLPS images are multiplexed into the TV signal. On the receiving end, special circuitry built into a TV or in a separate decoder box processes the incoming TV signal and isolates the NAPLPS code, making it available as a separate channel for information services on a TV set. The system operates only as a broadcast medium; interactive services are not possible.

The level of videotex activity in the US is increasing, and a key factor in NAPLPS's success will be the decision by videotex operators to incorporate NAPLPS's advanced display features into their service. So far, at least six US companies have active programs in which NAPLPS is central to their service's look: Three are consumer-oriented companies, and the other three direct their activities toward the business community. A score of other companies is engaging in various stages of planning or developing NAPLPS-based videotex services or investigating ways to add NAPLPS capability to their existing ASCII text-only services.

Adopting the standard

Although the step from standards approval to actual market adoption and use is sometimes less than guaranteed, some major companies seem to be lining up behind NAPLPS. Personal computer manufacturers such as IBM, DEC, and Wang have made clear their intention to support NAPLPS in their products with terminal-emulation software, and they have demonstrated the software's operation. A host of software houses, including Microstar, Ashdune, Avcor, Manitoba Telephone, Faxtel, Wolfdata, and Microtaure, are developing or delivering NAPLPS software. And companies like AT&T, Electrohome, Panasonic, Sony, and Norpak are offering dedicated NAPLPS decoder terminals that can be used in home or office settings.

Texas Instruments has identified NAPLPS products as an application area for its new AVDP display chip. AT&T is working on a VLSI NAPLPS decoding device for use in its next-generation NAPLPS terminal. It's



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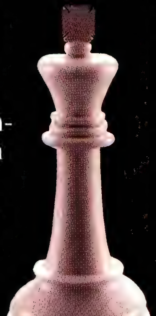

As integrated circuitry increases intricacy, and packaging densities require more layers, a qualified, r able source is needed to meet the advancing technology. HADCO h made the commitment to be that source. From initial design to pos delivery support, HADCO can fu all your multilayer needs. That involves more than meets the eye

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CIRCLE NO 113

Because the interpretation of a NAPLPS data stream is left up to the device receiving it, devices of varying resolution can display the same incoming image.

Reference model for communications standardization

Graphics standards are in the top levels of the Open Systems Interconnection (OSI) reference model, which is schematically outlined in the **table.** Introduced in 1978 by the International Standards Organization (ISO), the OSI plan calls for the eventual standardization of communications structures in a 7-layer format. Each layer provides a consistent set of services to the end user, which may be a terminal operator or an applications program. A set of protocols specifies each layer, and modularity stems from a standard interface between layers. Although it's by no means complete, the OSI model's lower levels (1 to 3) are essentially agreed upon, and the upper four are developing rapidly.

OPEN SYSTEMS INTERCONNECTION REFERENCE MODEL

7
APPLICATION
(USER SERVICES)

FILE TRANSFER/ACCESS
MESSAGE HANDLING
DOCUMENT TRANSFER
JOB MANIPULATION PROTOCOL
NETWORK MANAGEMENT
TRANSACTION PROTOCOLS
VIDEOTEX

6
PRESENTATION
(DEVICE DEPENDENT SYNTACTICAL CODE)

SPECIFIES TRANSFER SYNTAX FOR CHARACTER SETS, ENCRYPTION, ETC
NAPLPS

5
SESSION
(DIALOG, CONNECTION ESTABLISHMENT)

CONNECTION/TERMINATION
DATA TRANSFER
TASK SYNCHRONIZATION FOR END USERS
DIALOG CONTROL
DATA BUFFERING
CODE CONVERSION

4
TRANSPORT
(PROCEDURES FOR END-TO-END CONNECTION)

MULTIPLEX END USERS ONTO NETWORK
MESSAGE ADDRESSING/ROUTE INDEPENDENCE
QUALITY OF SERVICE MONITORING

3
NETWORK
(ROUTING & PACKET MANAGEMENT)

PACKET SWITCHING (X.25)
FLOW CONTROL
INTERNETWORKING
VIRTUAL CIRCUIT ESTABLISHMENT

2
DATA LINK
(PACKET, CIRCUIT & LINE PROTOCOLS)

LOCAL NETWORK PROTOCOLS
HDLC
SDLC

1
PHYSICAL
(MECHANICAL & ELECTRICAL INTERFACES)

COLLISION DETECTION FOR CSMA/CD
CABLE, CONNECTOR, AND COMPONENT RULES
ELECTRICAL PULSE/VOLTAGE HANDLERS
RS-232C

possible to couple the NAPLPS presentation-level standard with the other emerging graphics standards on the application-software level (Graphics Kernel System, or GKS) and the hardware interface end (Virtual Device Interface, or VDI). As a consequence, NAPLPS would seem to be a likely candidate to facilitate the spread of NAPLPS use in transportable applications and to penetrate other markets with NAPLPS-compatible equipment.

In CAD/CAM, for instance, it's very difficult to maintain a current library of component data in light of the rapidly changing selection of components. Because component data contains both graphic and textual technical detail, an obvious way for a manufacturer to ensure that data on its components is included in the libraries of all CAD/CAM suppliers is to describe it in NAPLPS, which handles both graphic and textual information.

If these suppliers adopt NAPLPS in this fashion, companies using CAD/CAM need only develop interpreters to translate common NAPLPS formats into whatever internal representation they need. Updating could take place on line. By dialing into a service company such as Videolog, the designer could not only locate the device needed to satisfy a particular requirement and learn about its characteristics but could also

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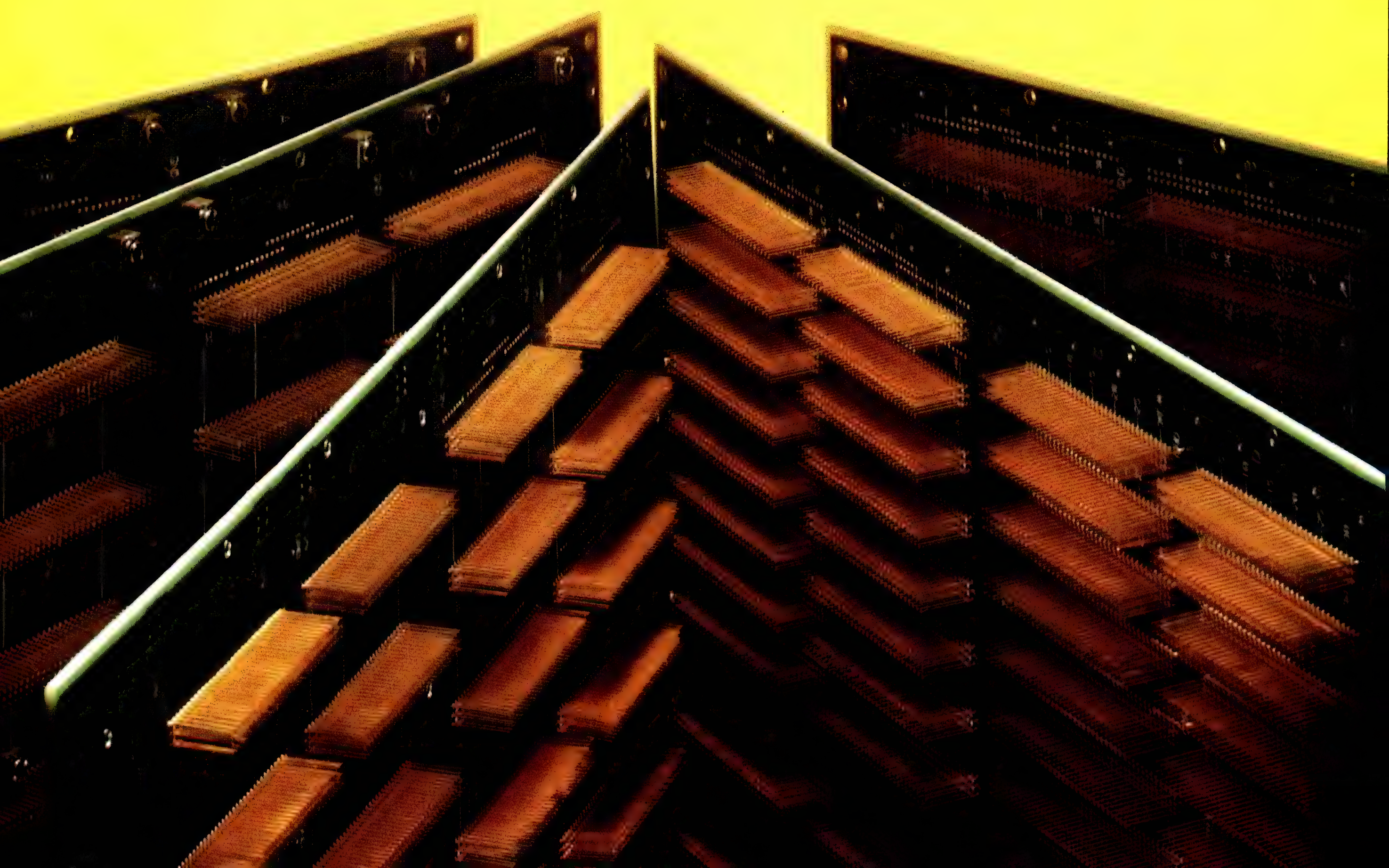

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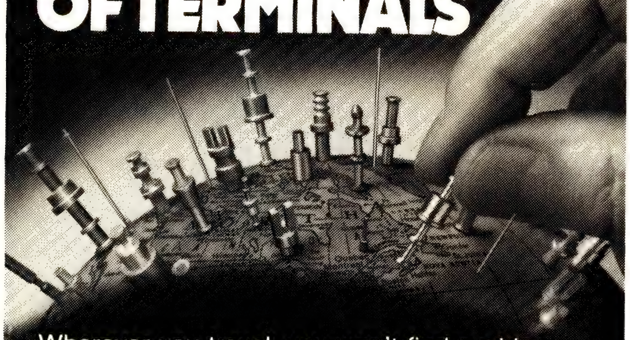

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An obvious way for a manufacturer to ensure that data on its components is included in the libraries of all CAD/CAM suppliers is to describe it in NAPLPS.

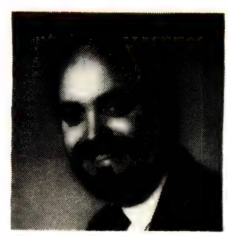
download its model into a local workstation for use in a CAD/CAM network.

A slightly different twist in the CAD/CAM area is the problem of transporting designs from one supplier's CAD/CAM system to another. Development of a translator to convert the internal formats into a NAPLPS format would not only permit transfer to another system, it would also allow telecommunication of the designs to any remote geographic location without delay. Engineers using different CAD/CAM systems could exchange designs, even designs for very different or specialized applications and even on CAD/CAM systems in different geographical locations. NAPLPS is an important aspect of the IGES/EDIF standards' efforts to transform this concept into reality.

To see the advantage of using NAPLPS in this way, consider how much a company spends to create charts and graphs in hard-copy form and ship them all over the world either via physical means or by telecopying. With NAPLPS, you could develop a graphic on the office microcomputer, dial another office on the phone, and ship the design via modem for remote disk storage and replay, all at a much lower cost. In addition, if you nestled NAPLPS between appropriate GKS and VDI interfaces, the images could then be locally manipulated or rendered into a variety of hard-copy formats as application needs dictated.

The emerging NAPLPS standard offers a range of new tools that companies can use to build innovative products and explore new applications. And there's no shortage of companies willing to enter the market with new products and services, which will have a significant impact on future graphics technologies. **EDN**

Author's biography



Gary Holland is vice president of product development at Videolog, which he helped to found in 1982. He received a BS in computer science from Massachusetts Institute of Technology in 1973. His hobbies include personal computing and photography.

Article Interest Quotient (Circle One)
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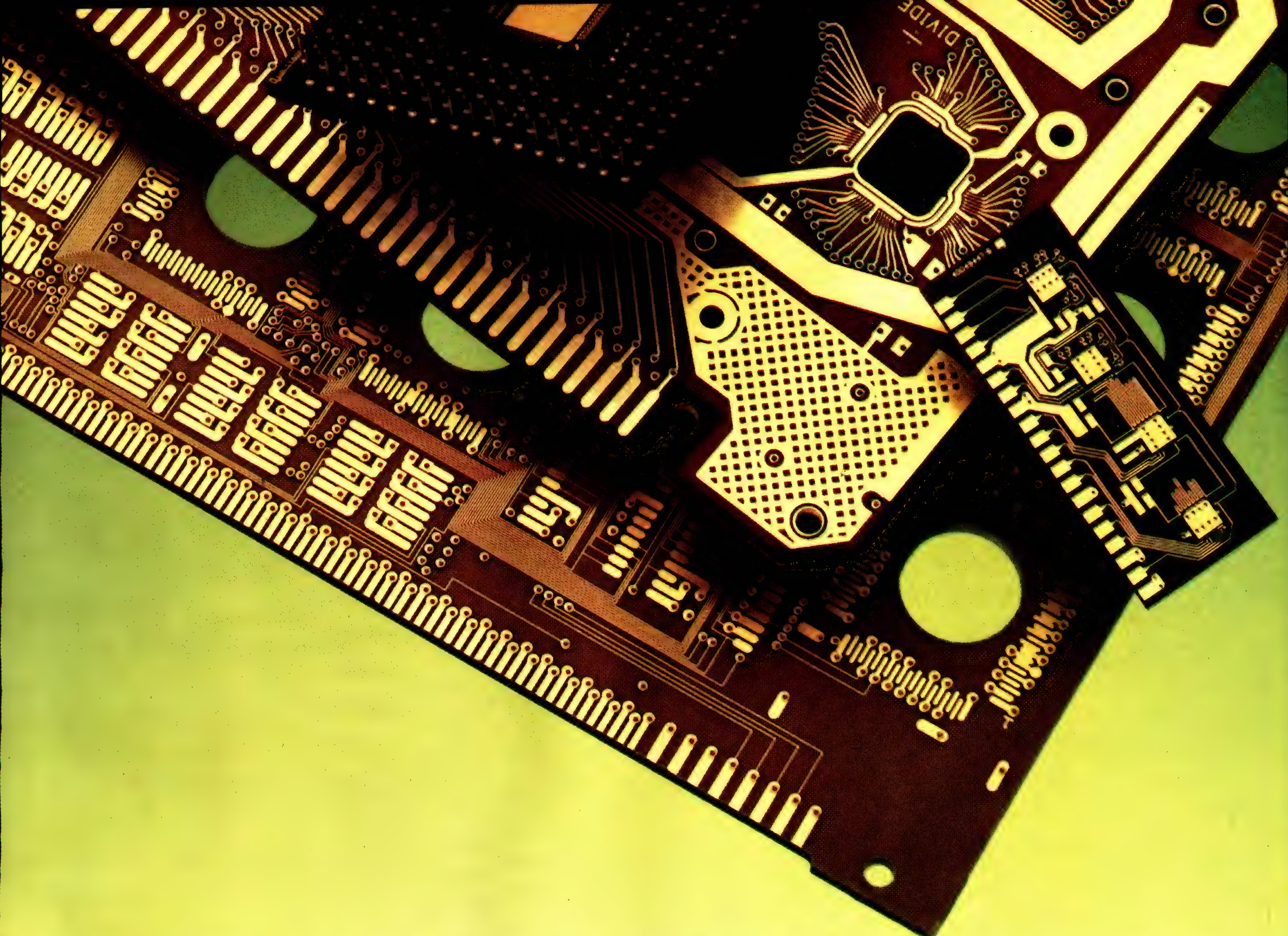

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CIRCLE NO 115

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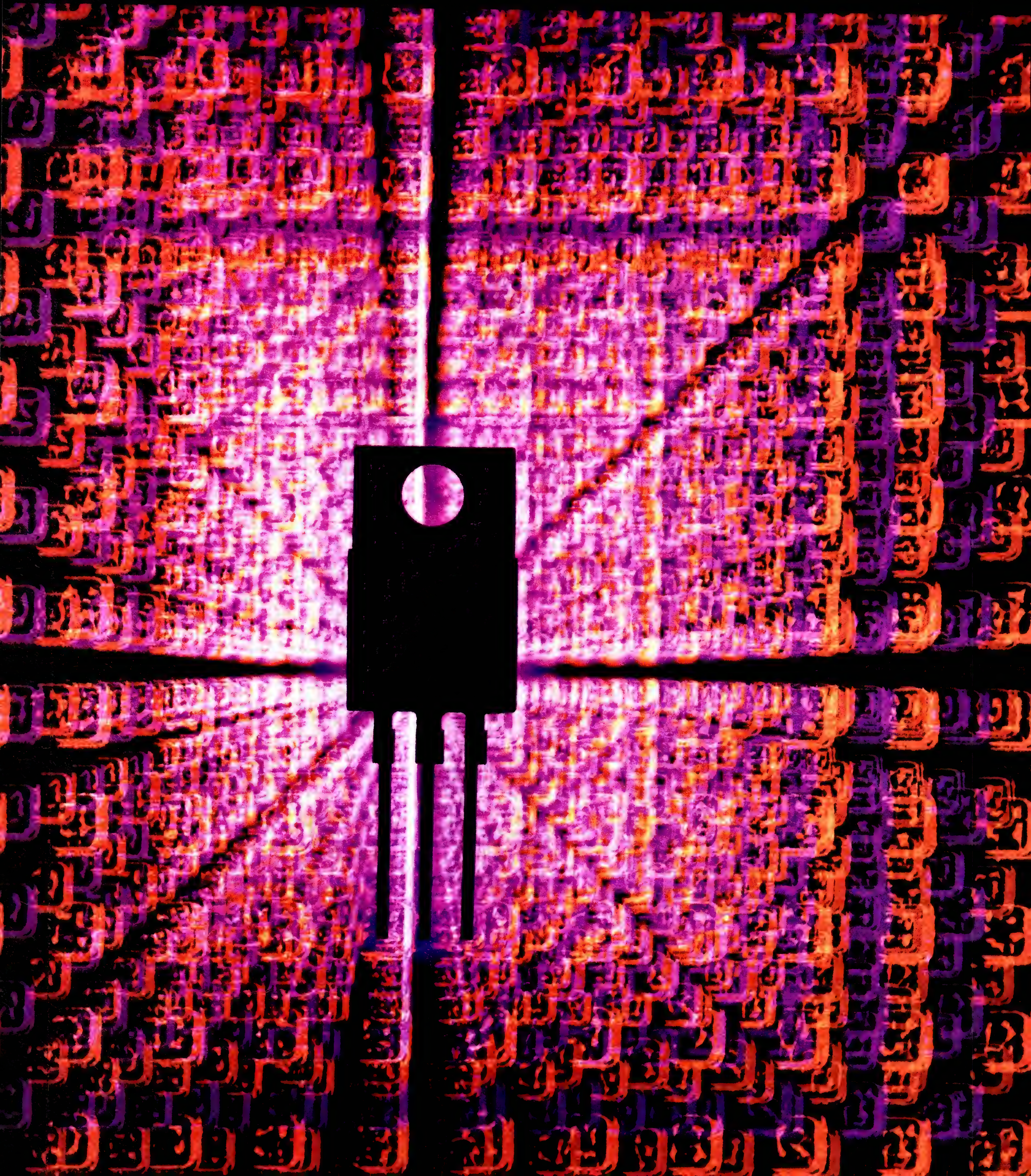

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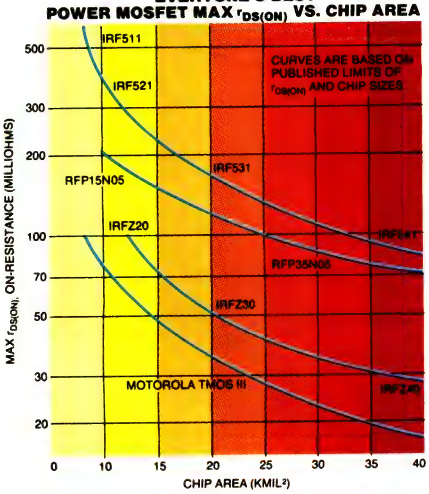

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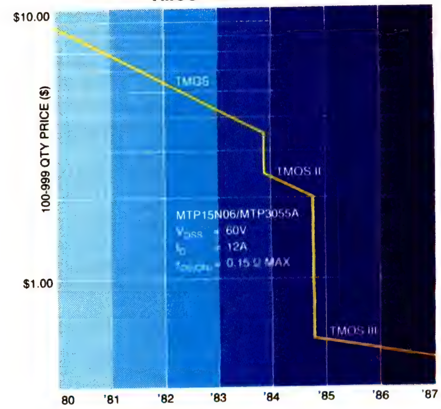

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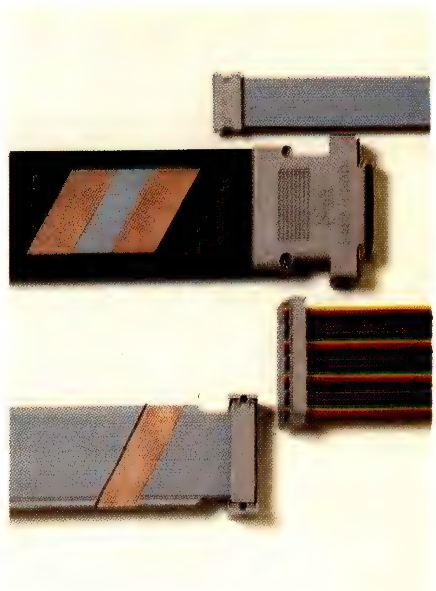

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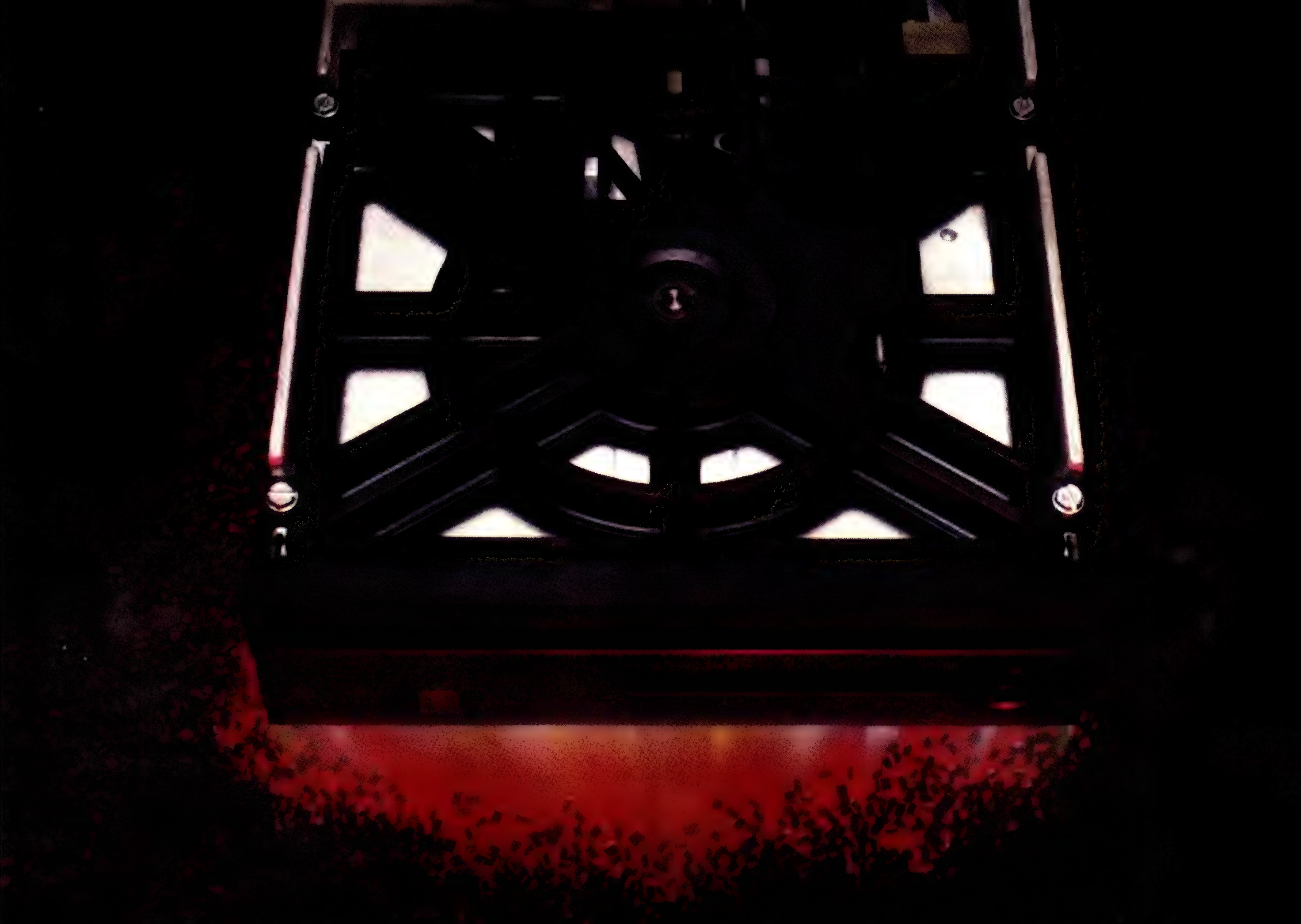

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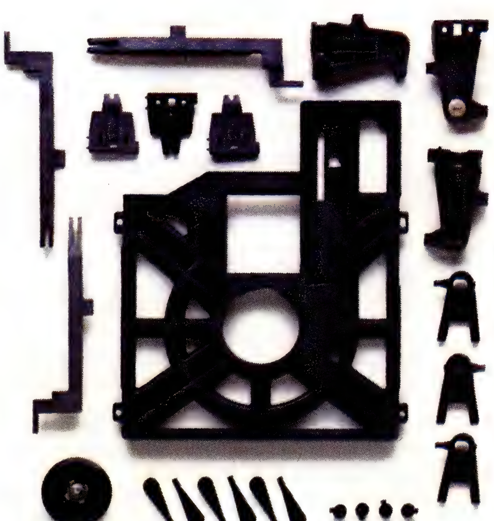

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Digitize transducer outputs directly at the source

Designers are searching for ways to digitize transducer outputs at the transducer itself. In Part 1 of this series, we described some circuit-design techniques that did the job for pressure and force transducers. Other physical properties—humidity, light, level, and acceleration—are subject to such design innovations as well.

Jim Williams, *Linear Technology Corp*

Digitizing transducer outputs far up in the signal chain is highly desirable—but tricky. Part 1 of this 2-part series demonstrated that it's possible to digitize directly at the transducer, without resorting to dc preamplification. It then described circuits that digitize the outputs of such common transducers as those that measure temperature and force. This second installment examines methods of digitizing outputs of transducers that detect light, humidity, surface levels, and acceleration.

Because of their extremely wide dynamic range, photodiodes generate outputs that are particularly difficult to digitize. High-quality devices furnish linear current outputs over a 100-dB range, and directly digitizing these outputs while maintaining that dynamic range would require 17-bit A/D converters as well as current/voltage input amplifiers. To mitigate the effects of this restriction, one common alternative approach calls for the compression of the diode's output with a logarithmic current/voltage input amplifier. This approach allows you to use a lower-resolution A/D converter, saving you the cost of a 17-bit A/D converter. However, nonlinear outputs aren't convenient to work with, and log amps respond slowly and can degrade performance in some photometric measurements.

The circuit shown in **Fig 1a** provides another alternative. It directly converts a photodiode's current output to a frequency output that has a 100-dB dynamic range. An optical input of 20 nW to 2 mW produces a linear, calibrated output of 20 Hz to 2 MHz. The circuit responds quickly to input steps, yet it costs little to implement.

Modified I/F converter does the trick

In operation, the photodiode's output current feeds a modified high-frequency version of a Pease charge-pump I/F converter. The output current biases amplifier IC_1's negative input, causing the amp's output (**Fig 1b,** trace A) to ramp down. When IC_1's output crosses zero, comparator IC_2's output (trace B) goes low. (The comparator's high-frequency response is aided by the 200-pF/1.8-kΩ network at the positive input.) The LT1009 diode and its associated diode bridge limit IC_2's output to −3.7V. When IC_2's output goes low, it also provides ac positive feedback to its positive input (trace D). Additional ac positive feedback comes from transistor Q_3's collector (trace C).

During this interval, the 47- and 5-pF capacitors pull charge from IC_1's summing point (trace E). This action causes IC_1's output to switch rapidly in a positive

Aimed at light-sensing applications, an I/F circuit converts a photodiode's output current to a frequency signal with a 100-dB dynamic range.

direction, and this event in turn switches IC_2 after the positive feedback around it has decayed. Now the LT1009 and its associated diode bridge limit IC_2's output to +3.7V. As the capacitor pair receives charge, IC_1's summing junction recovers, and the entire cycle repeats at a frequency linearly related to photodiode output current.

While D_1 and D_2 compensate the bridge diodes, transistor Q_1 compensates transistor Q_2. These two transistors, connected as diodes (Q_2 operates as a steering diode), provide lower leakage current than standard components. Comparator IC_3 provides protection against circuit latchup—a precaution made necessary by the circuit's ac-coupled feedback loop. If latchup occurs, IC_1's output saturates low, causing IC_3's emitter-follower-connected output to go high. This change forces IC_1's output positive and initiates normal circuit operation.

The LT1021-10 reference biases the photodiode to obtain optimum optical response. To trim this circuit, place the photodiode in a *completely* dark environment. Trim the dark-current adjust control so that the circuit oscillates at the lowest possible frequency—typically 1 to 2 Hz. Next, apply or electrically simulate a 2-mW optical input and trim the 5-pF adjust control for a 2-MHz output. If the adjustment falls outside the trimmer's range, alter the 47-pF capacitor's value. Once calibrated, this circuit maintains 1% accuracy over the photodiode's 100-dB range, and photodiode characteristics—and not the circuit—limit accuracy. **Fig 1c** shows the circuit's dynamic response to a fast light pulse (trace A); note that the frequency output settles within 1 μsec on both edges.

Humidity transducers pose problems

One the most difficult physical properties to detect electronically is relative humidity. The circuit shown in **Fig 2a** incorporates a recently introduced humidity transducer that transmits readings of relative humidity (RH) as a linear function of capacitance shift. The transducer features a nominal ±1.7-pF/%RH shift; a 500-pF value corresponds to RH=76%, and the transducer doesn't require temperature compensation. When conditioning its signals, however, note that the average voltage across it must be 0V; no net voltage may be applied to it.

The circuit converts the RH transducer's capacitive shifts directly into a calibrated frequency output. The LTC1043 switched-capacitor IC has an internal clock, and because it runs free at 150 kHz, it switches, via pin 2 (**Fig 2b**, trace A), between the LT1004 negative reference and IC_1's summing junction. (The 1-μF/22-MΩ combination ensures that no dc signal component is applied to the transducer.) Two states are therefore possible: When pin 2 connects to pin 6, the transducer receives a negative charge; when pin 2 connects to pin 5, the transducer's charge goes into IC_1's summing point.

IC_1's input (trace B, just faintly visible) shows transducer current, while trace C is IC_1's output. Functioning as an integrator, IC_1 ramps up in steps as successive packets of charge appear at its summing point. Concurrently with this action, a second set of switches (pins 7, 11, 8, 13, 12, and 14) synchronously transfers a fixed charge of opposite polarity into IC_1's summing junction. The amount of this fixed charge cancels the sensor offset (for instance, 0% RH doesn't extrapolate to 0-pF sensor capacitance). Consequently, the slope of the stepped ramp at IC_1's output varies with the sensor's value minus its offset term.

IC_1's output continues to ramp up until it equals the voltage at comparator IC_2's negative input and triggers IC_2's output high (trace D). AC-positive feedback holds IC_2's output high long enough for the 2N4393 FET to discharge IC_1's feedback capacitor. Then IC_1's output drops to zero, and the entire cycle repeats. The frequency of repetition is a function of the RH transducer's capacitance.

Low dependency on temperature

The LTC1004 reference provides an input voltage for IC_2, while the LTC1043's pins 3, 18, and 15 and the 330-pF capacitor form a simple charge pump that biases IC_3's summing point. IC_3's output assumes the value required to keep its summing point at zero. The 0.22-pF capacitor across IC_3 integrates that amp's response to dc, and the feedback resistors establish its operating point. Because IC_3's output voltage determines ramp height, these feedback resistors set the circuit's gain slope. The time and magnitude expansions in traces A_{EXP}, B_{EXP}, and C_{EXP} detail the effects of the transducer's charge dumping on IC_1's output ramp.

Temperature dependency in this circuit is low because the −120-ppm drifts of the 330-pF and 0.01-μF polystyrene capacitors (both gain terms) cancel ratiometrically. Further ratiometric error cancellation occurs because the transducer's charge source and IC_3's output voltage both come from the LT1004 reference. The only uncompensated term in the circuit, the 470-pF capacitor that supplies the offsetting charge, has a

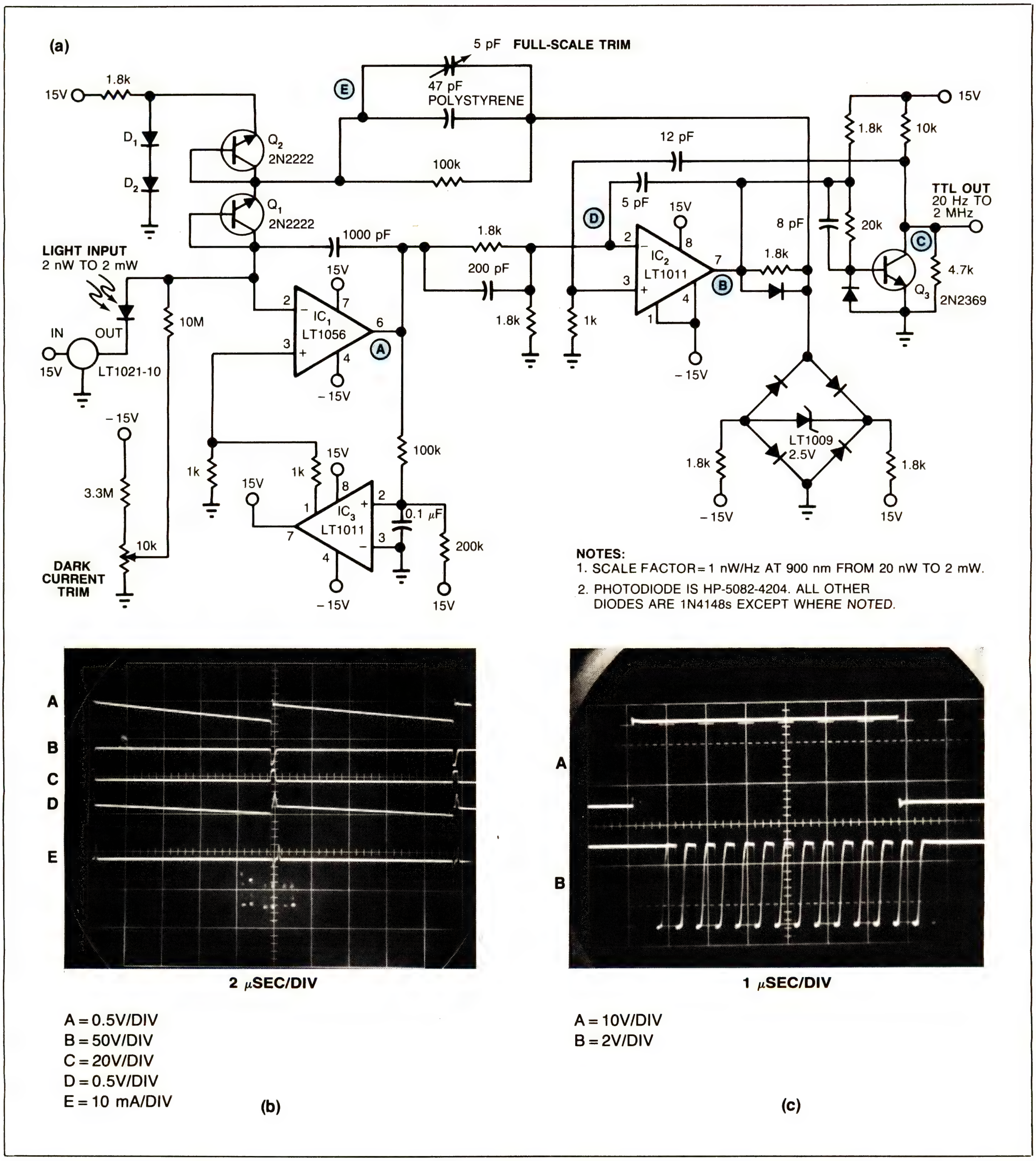


***Fig 1—This circuit (a) directly converts the current output** of a photodiode into an output frequency with 100 dB of dynamic range. Once calibrated, the circuit—a modified Pease charge-pump I/F converter—maintains 1% accuracy over the full range. Its frequency output settles within 1 μsec on both edges **(c)**.*

A variable-capacitance transducer forms the basis of a circuit that generates an output frequency proportional to relative humidity.

−120-ppm/°C drift that's well below the transducer's 2% accuracy specification. Circuit temperature independence is thus assured.

To calibrate this circuit, place the transducer in a 5% RH environment and adjust the 5% trim for a 50-Hz output. Next, place the transducer in a 90% RH environment and adjust the 90% trim for a 900-Hz output. By repeating this procedure until both points are fixed, you'll achieve relative-humidity accuracy of 2% over the 5 to 90% RH range. If RH standards aren't available, you can approximately calibrate the circuit by using fixed capacitors in place of the sensor. Ideal values are 5% RH=379.3 pF and 90% RH=523.8 pF. You should note that these values assume an ideal sensor, and that an actual device's values can deviate by 10%.

Another common physical property that lends itself to direct digitization is surface level. You'll find transducers that measure the angle of deviation from an ideal level in road-construction applications, machine tools, inertial-navigation systems, and other systems requiring a gravity reference.

A small tube, containing a partially conductive fluid and leaving a bubble that changes location with respect to level, forms an elegant, simple level transducer (**Fig 3a**). Electrodes are inserted in each end of the tube, and a common electrode penetrates the center. If the tube is level with respect to gravity, the bubble sits in the center, and respective resistance values between

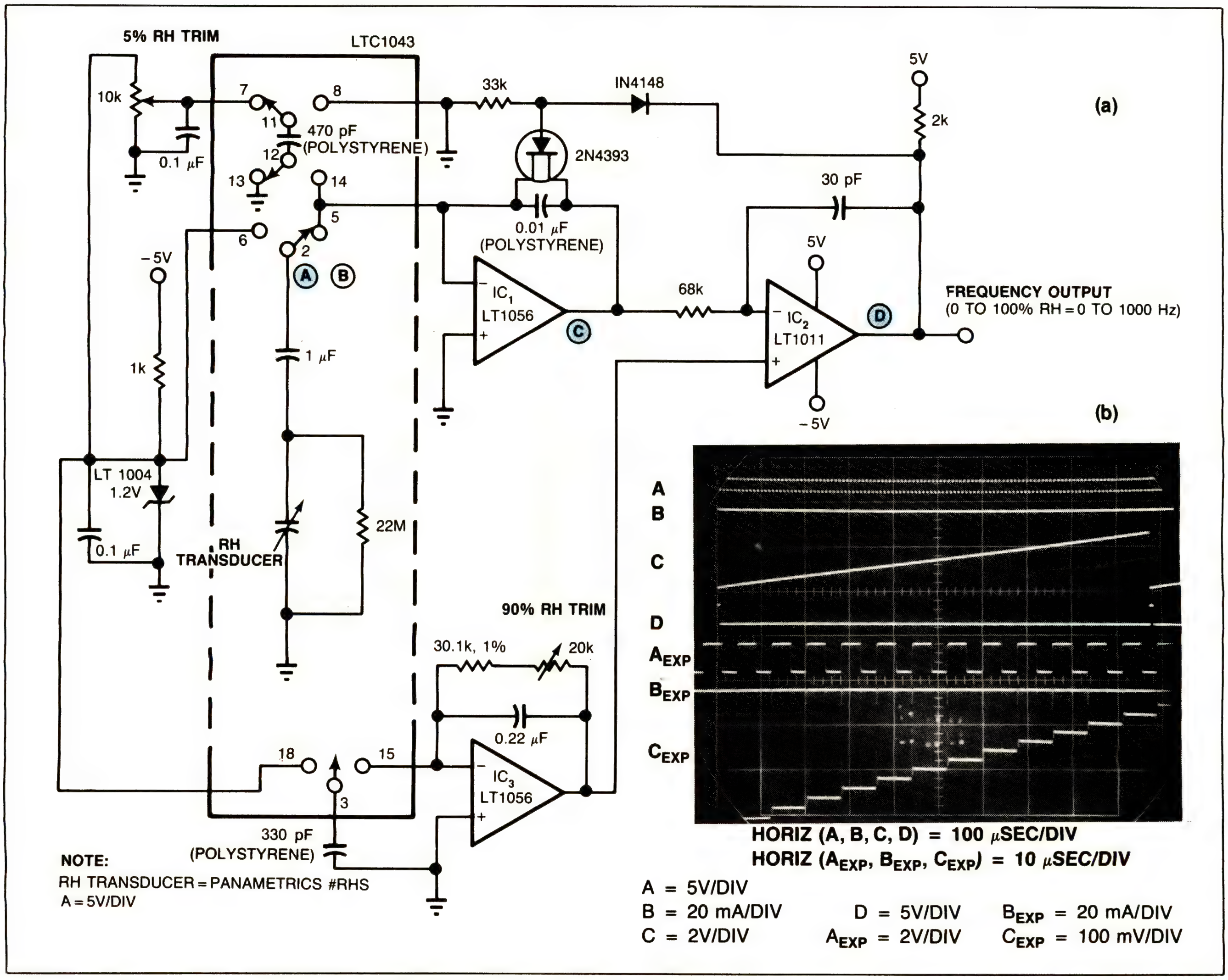


Fig 2—Tracking relative humidity as a function of linear capacitance shift, *the transducer in this circuit* ***(a)*** *requires no temperature compensation. Be sure to keep the average voltage across the device at 0V.*

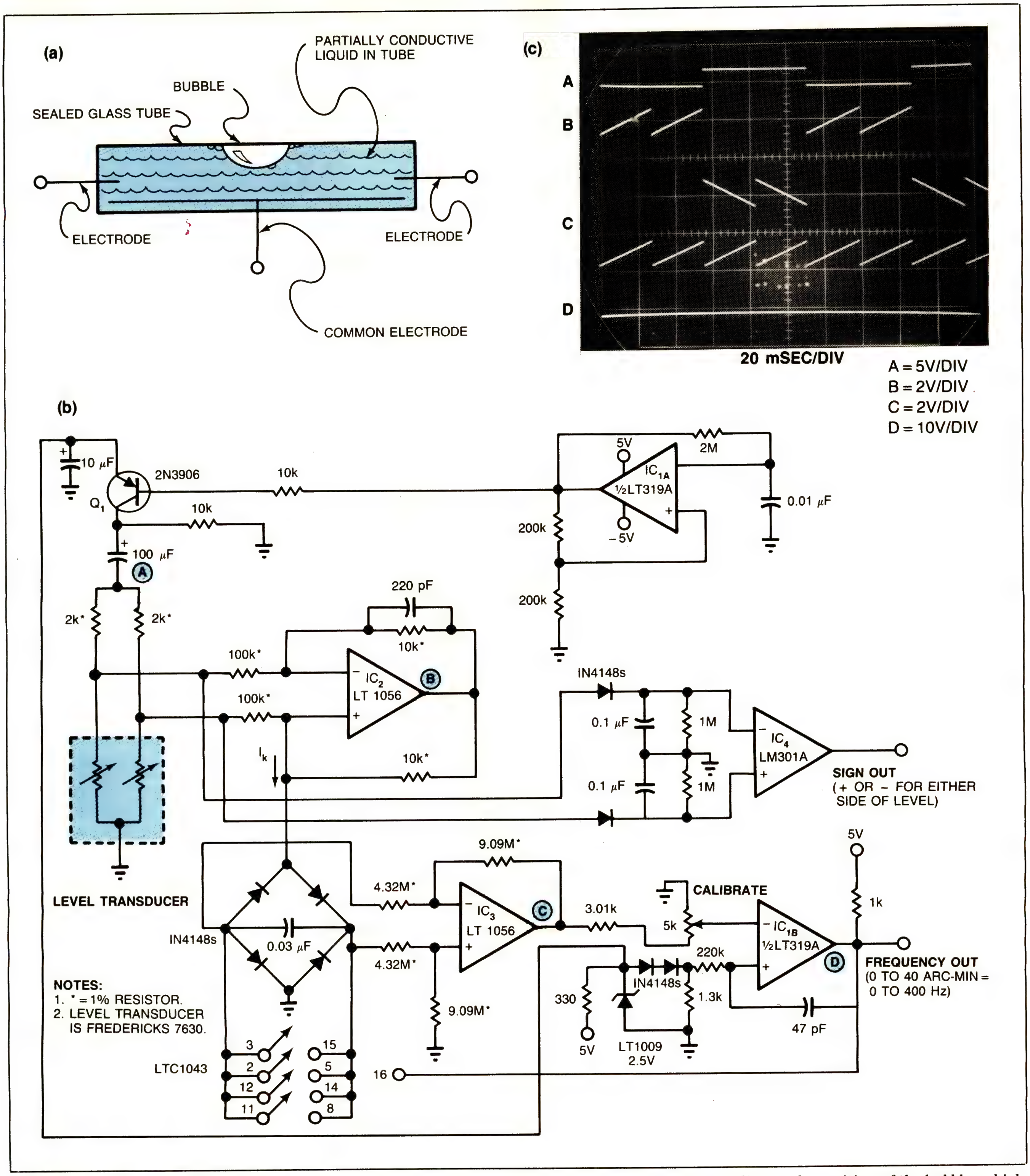


***Fig 3—A simple level transducer (a)** contains partially conductive fluid and determines level according to the position of the bubble, which alters resistance values between the respective end electrodes and the common electrode. The transducer's attached circuitry **(b)** produces a calibrated frequency output corresponding to surface level.*

the common electrode and the two end electrodes are identical. As the tube shifts away from level, however, these resistance values change proportionally. By controlling tube shape, suppliers can produce units with linear output that you can incorporate into a bridge circuit.

To avoid damaging the tube's conductive liquid, you must excite it with an ac waveform. The transducer circuit then must generate this excitation as well as extract angle information and determine polarity (ie, determine in which direction the level has shifted). **Fig 3b** shows a circuit that directly produces a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

The level transducer consists of two 2-kΩ resistors in a bridge that takes ac excitation from IC_{1A} (which is

An elegant level transducer employing a curved tube and conductive liquid measures a surface's angle of deviation from the horizontal.

configured as a multivibrator) in the following manner: IC_{1A} biases Q_1, which switches the LT1009's 2.5V potential through the 100-μF capacitor to provide the ac drive. Then IC_2, operating as a Howland current pump, converts the bridge's differential-output ac signal into a current. This current, whose polarity reverses as the bridge's drive polarity switches, is rectified by the diode bridge. As a consequence, the 0.03-μF capacitor receives unipolar charge. IC_3, running at a differential gain of 2, senses the voltage across the capacitor and presents its single-ended output to IC_{1B}.

When the voltage across the 0.03-μF capacitor becomes high enough, IC_{1B}'s output goes high and turns on the paralleled sections of the LTC1043 switch to discharge the capacitor. A 47-pF capacitor provides enough ac feedback to IC_{1B}'s positive input to allow a complete zero reset for the 0.03-μF capacitor.

Offset translates level to frequency

When the ac feedback ceases, IC_{1B}'s output goes low and the switch goes off. The 0.03-μF unit again receives constant current charging, and the entire cycle repeats. The magnitude of the constant current delivered to the bridge/capacitor configuration determines this oscillation's frequency; that magnitude depends on the transducer bridge's offset, which is related to level.

Fig 3c shows circuit waveforms. Trace A represents the bridge's ac drive, and trace B is IC_2's output. Note that when bridge drive changes polarity, IC_2's output rapidly switches polarity to maintain a constant current into the bridge/capacitor configuration. IC_3's output (trace C) is a unipolar, ground-referred ramp, and trace D shows IC_{1B}'s output pulse, which is the circuit's output.

The diodes at IC_{1B}'s positive input provide temperature compensation for the sensor's positive temperature coefficient, allowing IC_{1B}'s trip voltage to track bridge output over temperature ratiometrically. The sign output comes from IC_4, which operates without feedback and compares the rectified and filtered bridge-output signals with respect to ground.

To calibrate this circuit, place the level transducer at a 40-arc-min angle and adjust the 5-kΩ trimmer at IC_{1B} for a 400-Hz output. The transducer limits circuit accuracy to roughly 2.5%.

Accelerometers exploit ceramics

The final example concerns direct digitization of the outputs of piezoelectric accelerometers, which rely on the properties of ceramic materials to produce charge when mechanically excited. In such transducers, a mass is coupled with a ceramic element, which dispenses a charge when the mass experiences acceleration. The transducer's sensitivity and frequency response vary according to the device's mechanical design and the ceramic used.

The best way to condition a piezoelectric output is to unload it through a coaxial cable directly into the virtual ground of an op amp's summing point. This method ensures that there will be no voltage difference in the coaxial cable between its center conductor and its shield, and it thereby eliminates cable capacitance as a parasitic term—an important consideration in any charge-output transducer. Because the accelerometer produces ac outputs, a direct digitization of its output must include a sign bit as well as amplitude data.

Square-wave source is instructive

The circuit shown in **Fig 4a** accomplishes a complete direct A/D conversion of the piezoelectric accelerometer's output, and it will work with other devices in the same class. To understand the circuit, it's instructive to replace the accelerometer with a square-wave source coming through a resistor. When the square wave is positive, IC_1's integrator responds with a negative ramp output (**Fig 4b,** trace A). IC_2, also detecting the square wave's polarity, goes high, but the LT1009 and its associated diode bridge (trace B) limit the signal to +3.7V.

These two signals converge at IC_3's negative input, where IC_1's ramp output combines with the bridge's output. For stability, the series diodes provide temperature compensation for the bridge diodes. When IC_1's output goes negative to a specified point, IC_3's output (trace C) goes high. The two comparators control output gating: When IC_2's output is low and IC_3's is high, Q_1's gate (trace D) receives turn-on bias.

When Q_1 comes on, it discharges IC_1's feedback capacitor and resets IC_1's output to zero. Local ac-positive feedback at IC_3 ensures adequate time for a complete zero reset of IC_1's feedback capacitor. The 100-pF capacitor at IC_3's input aids high-frequency response. When the ac feedback decays, Q_1 goes off, IC_1 again ramps down, and the cycle repeats as long as the input square wave is positive. The frequency of oscillation is directly proportional to the current flowing into IC_1's summing point.

When the input square wave goes negative, IC_1 abruptly ramps up. Simultaneously, the output of IC_2's input-polarity detector goes negative and forces the

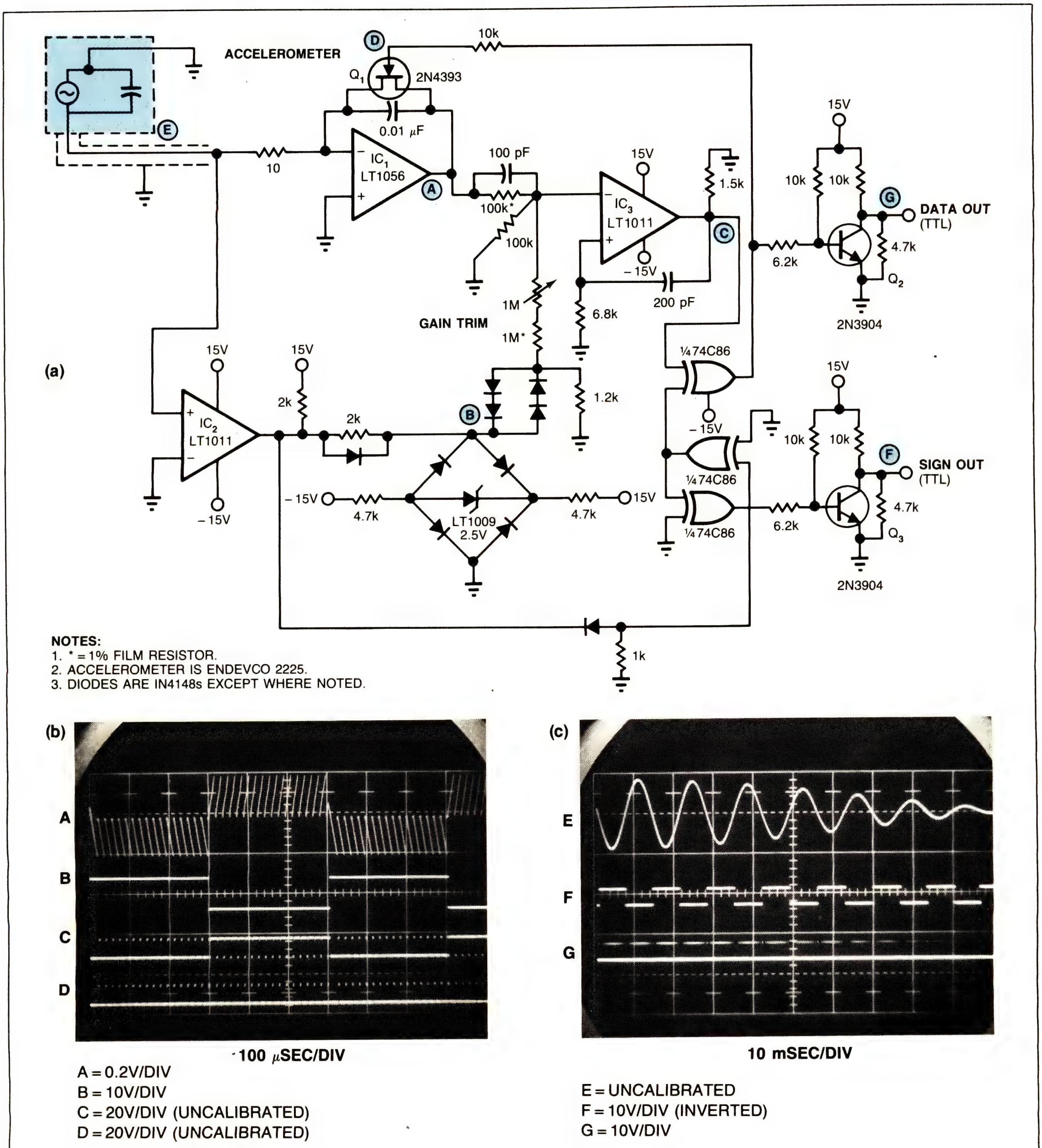


Fig 4—By replacing the accelerometer in this circuit (a) *with a square-wave source, you can more easily understand its operation. Direct digitization of a signal proportional to acceleration results when you return the piezoelectric accelerometer to the circuit. The waveforms in* ***c*** *show circuit response when you apply acceleration to the transducer.*

A piezoelectric accelerometer's ceramic elements release charge when excited.

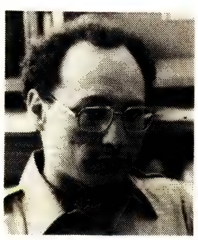
LT1009 and its diode bridge's output negative. IC_3's output now switches when IC_1's output exceeds a positive limit. The output gating, directed by IC_2's polarity signal, inverts IC_3's output to supply proper drive to Q_1's gate. Q_1 turns on and resets the circuit. Consequently, the loop maintains oscillation, but with all signs reversed. The Q_2 and Q_3 level shifters supply TTL data outputs for sign and magnitude.

Insert accelerometer for digitization

The circuit described constitutes an I/F converter that responds to ac signals. If you now replace the square-wave source with a piezoelectric accelerometer, direct digitization results. **Fig 4c** shows circuit response when you apply an acceleration (trace E) to the transducer; in this case the response is a damped sinusoid. The sign bit (trace F) tracks acceleration polarity, while the frequency output supplies amplitude data.

Note the drop in output frequency as the input waveform damps. A monitoring process, sampling the sign and frequency waveforms faster than twice the highest frequency of acceleration, can extract the desired acceleration waveform data. To trim the circuit, apply a known amplitude acceleration and adjust the 1-MΩ gain trim at IC_3. As an alternative, you can electrically simulate the accelerometer using scale factors provided in accelerometer data sheets. **EDN**

Author's biography



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA) specializes in the design of analog circuits and instruments. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

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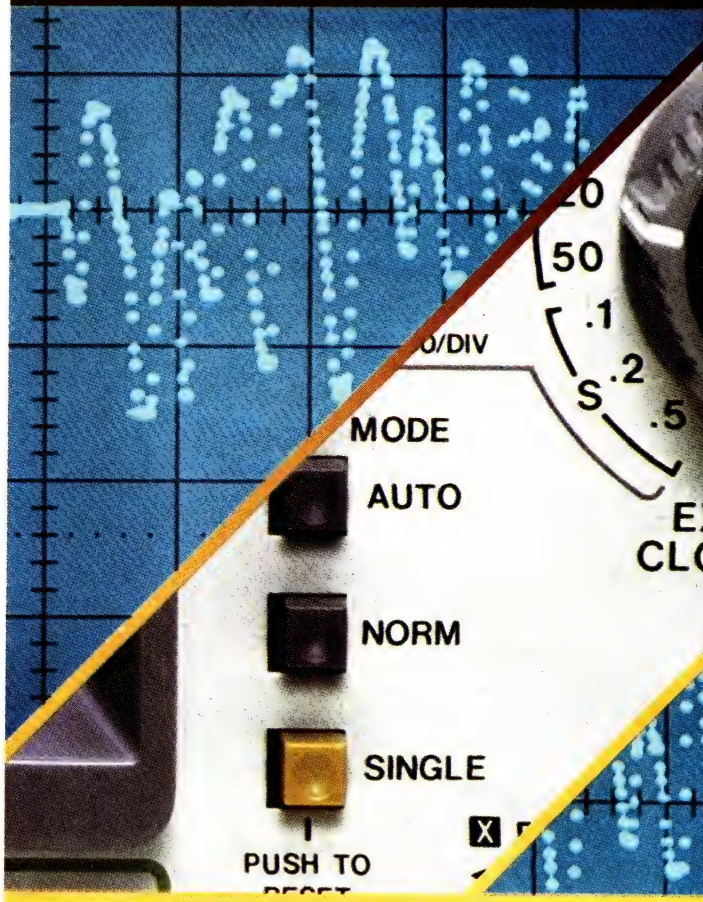

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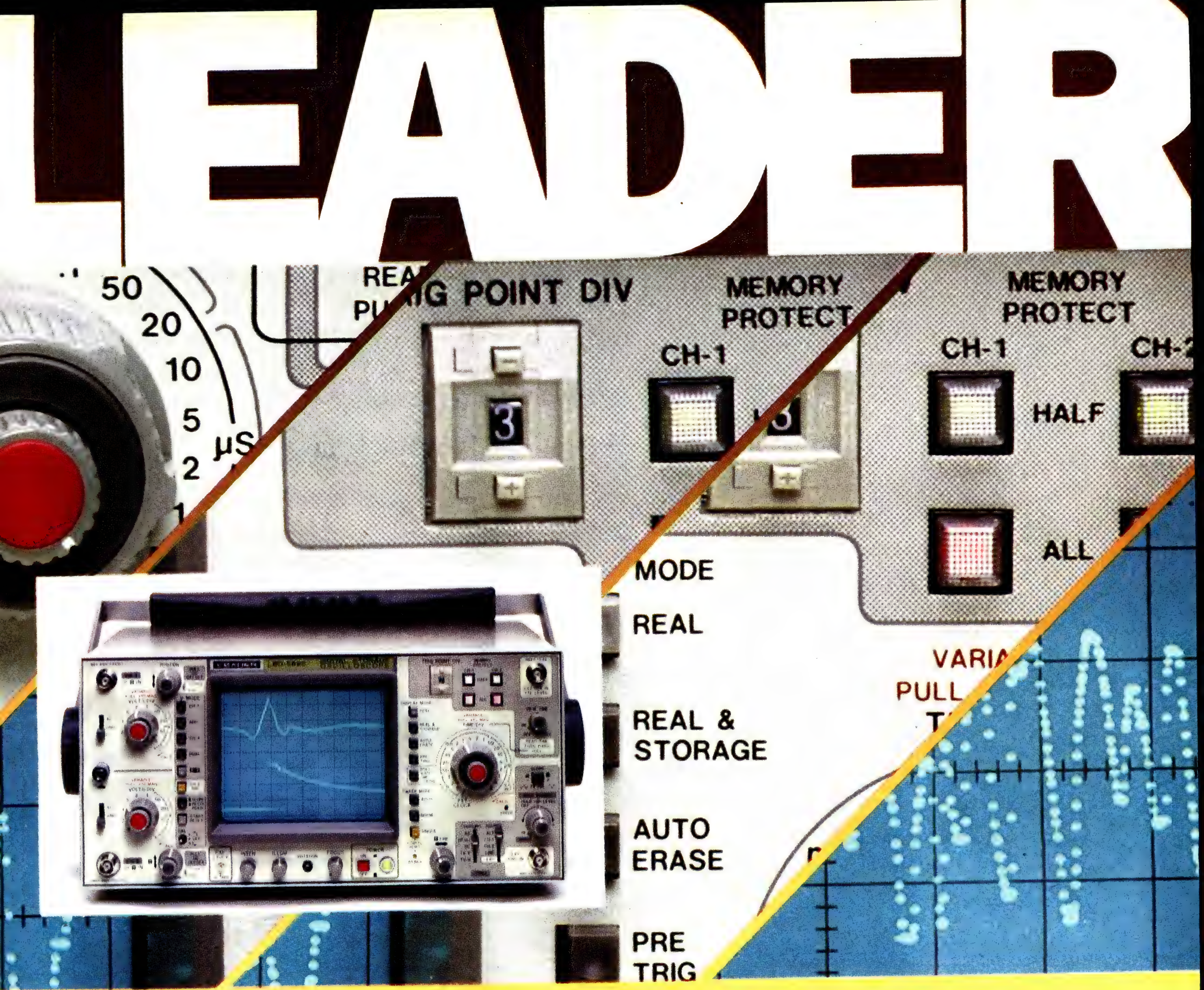

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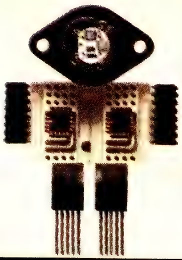

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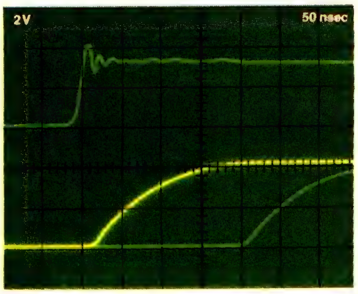

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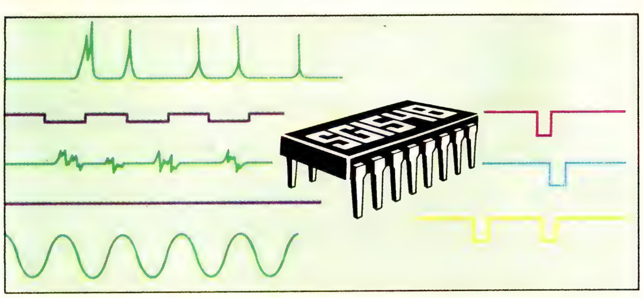

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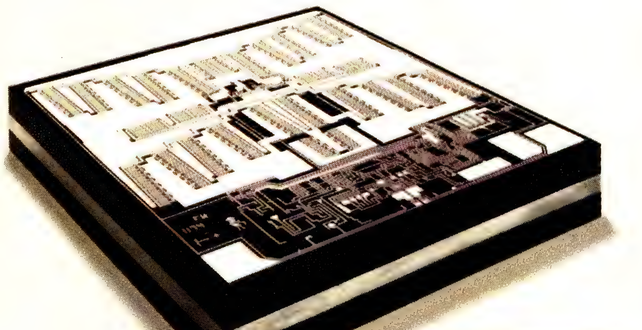

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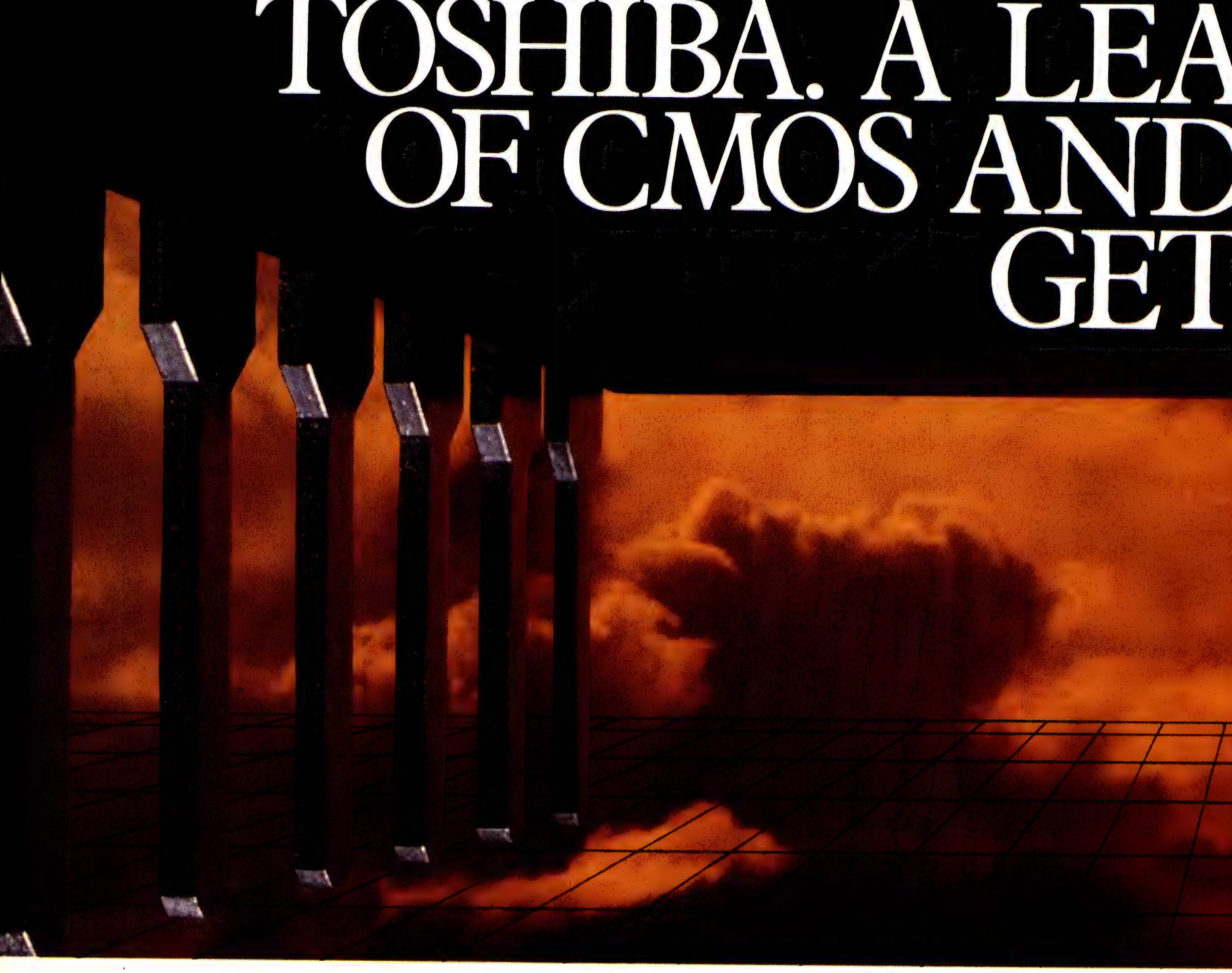

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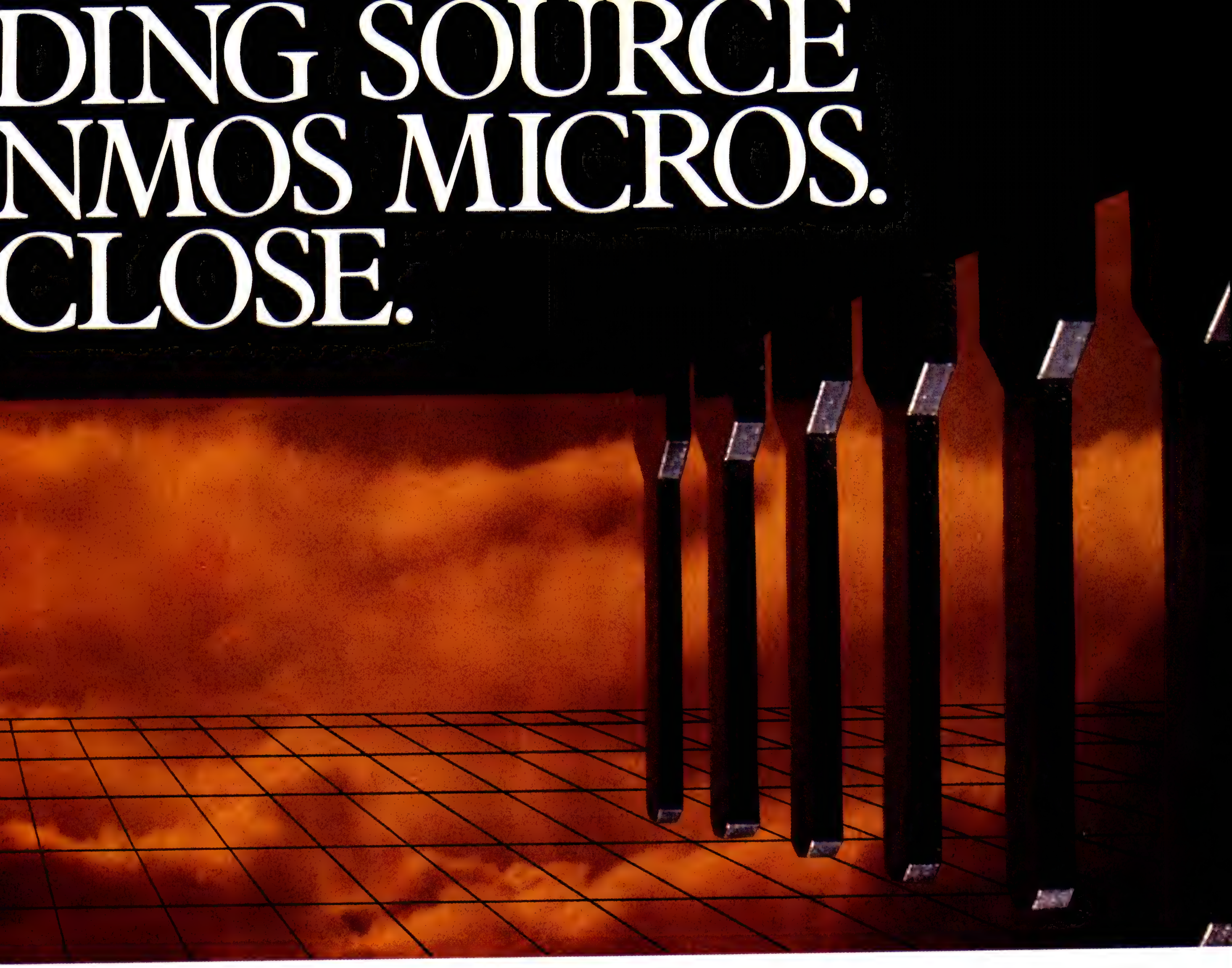

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8-BIT SINGLE CHIP MICROCOMPUTERS—8048/8049 FAMILY						
Device	Technology	ROM (Bytes)	RAM (Bytes)	Speed	Operating Current (Max)	Standby Current
TMP8048	NMOS	1K	64	6MHz	135mA	15mA
TMP80C48	CMOS	1K	64	6MHz	10mA	10μA
TMP8049	NMOS	2K	128	6MHz/11MHz	170mA	50mA
TMP80C49	CMOS	2K	128	6MHz	10mA	10μA
TMP80C50	CMOS	4K	256	6MHz	15mA	10μA

8-BIT MICROPROCESSOR—CMOS Z80A FAMILY				
Device	Description	Technology	Operating Current	Power-Down Current
TMPZ84C00	4MHz Z80A CPU	CMOS	15mA (@ 4MHz)	10μA

Also available are the popular Z80 peripherals in CMOS including P I/O, CTC, CLOCK, DMA & S I/O.

8-BIT MICROPROCESSOR—8085A FAMILY			
TMP8085A	NMOS	8085A	3MHz CPU plus many of the popular 8-bit peripherals.

4-BIT SINGLE CHIP MICROCOMPUTERS—TLCS-47 FAMILY

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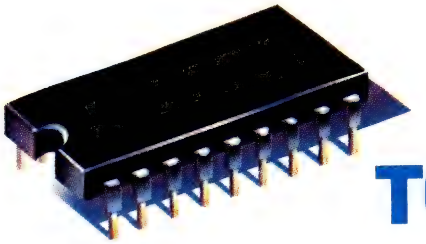

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CIRCLE NO 123

TURNING YOUR PC INTO A FASTER TOOL FOR MODERN TIMES.

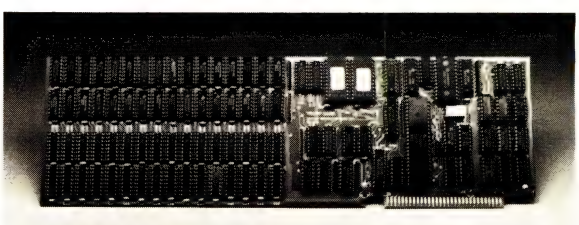
This is the 3rd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

IBM® and other compatible PC computers are fast enough for general home and office use. But, for hardware and software development applications, the gears turn slowly.

What you need is a faster "gear" to co-process with the Intel 8088 inside IBM's PC. Like Zilog's Z8001® CPU. Now, there's a way to increase throughput for the IBM PC—as well as test the performance of the Z8001 CPU for your high-performance applications with a Z8001 CPU-based board called the "Trump Card" from Sweet Microsystems. And it proves dramatically how powerful Zilog's 16-bit CPU really is.

The new device is a peripheral board that plugs into any expansion slot on an IBM PC or compatible PC computer. Trump Card is addressed as an I/O device that communicates through the expansion bus. It is powered by Zilog's Z8001 CPU.

The Trump Card increases the computational power of the IBM PC, and provides maximum performance with a minimum of board space.



The Trump Card, shown from the front.The left side of the board contains 512 K-bytes of type-4164 dynamic RAM; the right side contains the Zilog Z8001 and *an interface* to the IBM PC I/O-expansion bus.

Z8001 COMPILER BASIC IS 80 TIMES FASTER THAN IBM INTERPRETIVE BASIC.

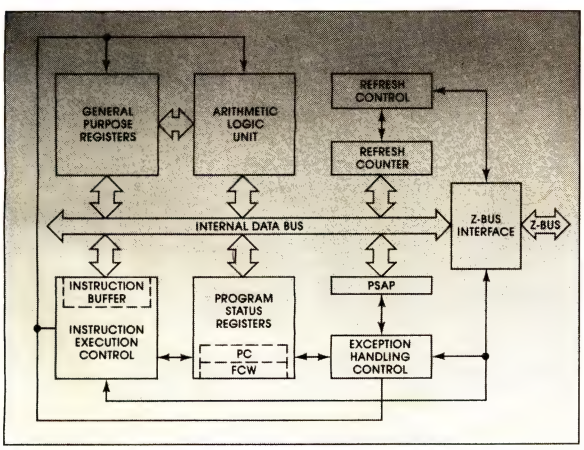
Essentially a monolithic minicomputer central processing unit, the Z8001 CPU is characterized by an instruction set more powerful than many minicomputers. As the programmer sees it, the Z8001 contains sixteen 16-bit general-purpose registers (for addresses or data) that may also be used in groups to form as many as eight 32-bit registers or four 64-bit registers. The low-order halves of the registers may be used for byte operations, thus the Z8001 CPU is able to manipulate data in 8-, 16-, 32-, and 64-bit pieces.

The Z8001 CPU, running at 10 MHz, can execute the same programs 4 to 10 times faster than the Intel 8088. What's more, the Z8001 CPU, with its large 8-megabyte memory range, makes the Trump Card's 512K bytes of memory easy to design with. (To use this memory in the card, you simply load a BASIC, CP/M-80, or C program from PC-DOS and type "RUN.")

Apple II	Apple III	TRS-80 Model II	IBM PC	IBM PC (with Trump Card)
224	222	189	190	2.4

A comparison of execution times (in seconds). Running on IBM's interpretive BASIC, a Sieve program takes 190 seconds to execute. Running the same program under TBASIC on the Trump Card Compiler takes only 2.4 seconds.

The eight addressing modes are register, indirect-register, direct-address, indexed, immediate, base-address, base-indexed, and relative-address. The instruction set utilizes data types ranging from single bits to a 32-bit long word. What's more, the processor executes 110 distinct instruction types that, when permuted by all the addressing modes and data types, create a set of more than 400 instructions.



A Z8000 CPU functional block diagram of the internal structure of the Zilog Z8000 family of high-performance microprocessors.

ALL THE PROPER SUPPORT FOR 512K BYTES OF MEMORY.

The wide range of software written for the Z8001 CPU is proven by all the programs you can run on the Trump Card. With the Z8001-based Trump Card, you can run the following software on your IBM or other compatible PC:

BASIC Compiler—TBASIC is PC BASICA-compatible. Most instructions are implemented without modification.

CP/M-80 Emulator—Allows you to run CP/M-80 Z80 assembly language programs directly. Just download your Z80 programs and run them.

C-Compiler—The industry standard version of C is available.

Debugger—Intended to aid in program development, you can examine and change memory and register contents and more.

Screen-editor—Has many word processing features, including ASCII text file development.

Multilevel Language Compiler—Allows Pascal-like control and data types, arithmetic expressions with automatic or specified allocations of registers, and more.

RAM Disk—Can allocate 128K to 387K bytes of on board memory to function as an intelligent RAM disk.

COPROCESSING IS JUST PART OF THE STORY.

The Z8001-based Trump Card is just one example of a successful application design for the Z8001 CPU. But there's far more to the Z8000 family than this.

Today, Z8000 CPU's are used in a wide range of applications, from industrial and medical products to computers and graphics imaging machines. And Zilog stands behind every application with service and software support that makes your Z8000-based products get to market on time.

Find out for yourself how much power Zilog packs into every Z8000 CPU by turning your IBM PC into a faster tool for modern times.

To get your own Trump Card and complete instructions, call Sweet Microsystems at (401) 461-0530.

For information about the Z8000 CPU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call 408-370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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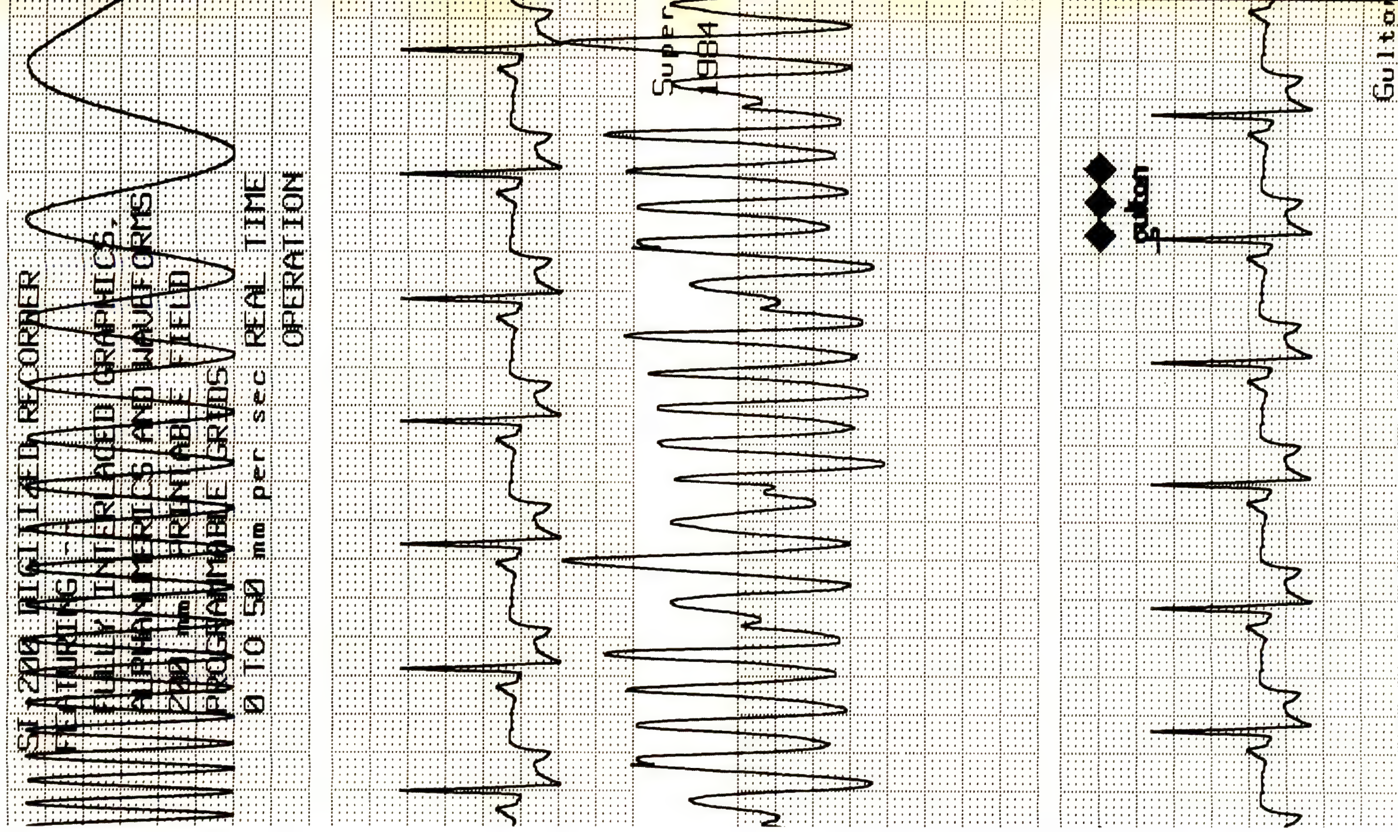

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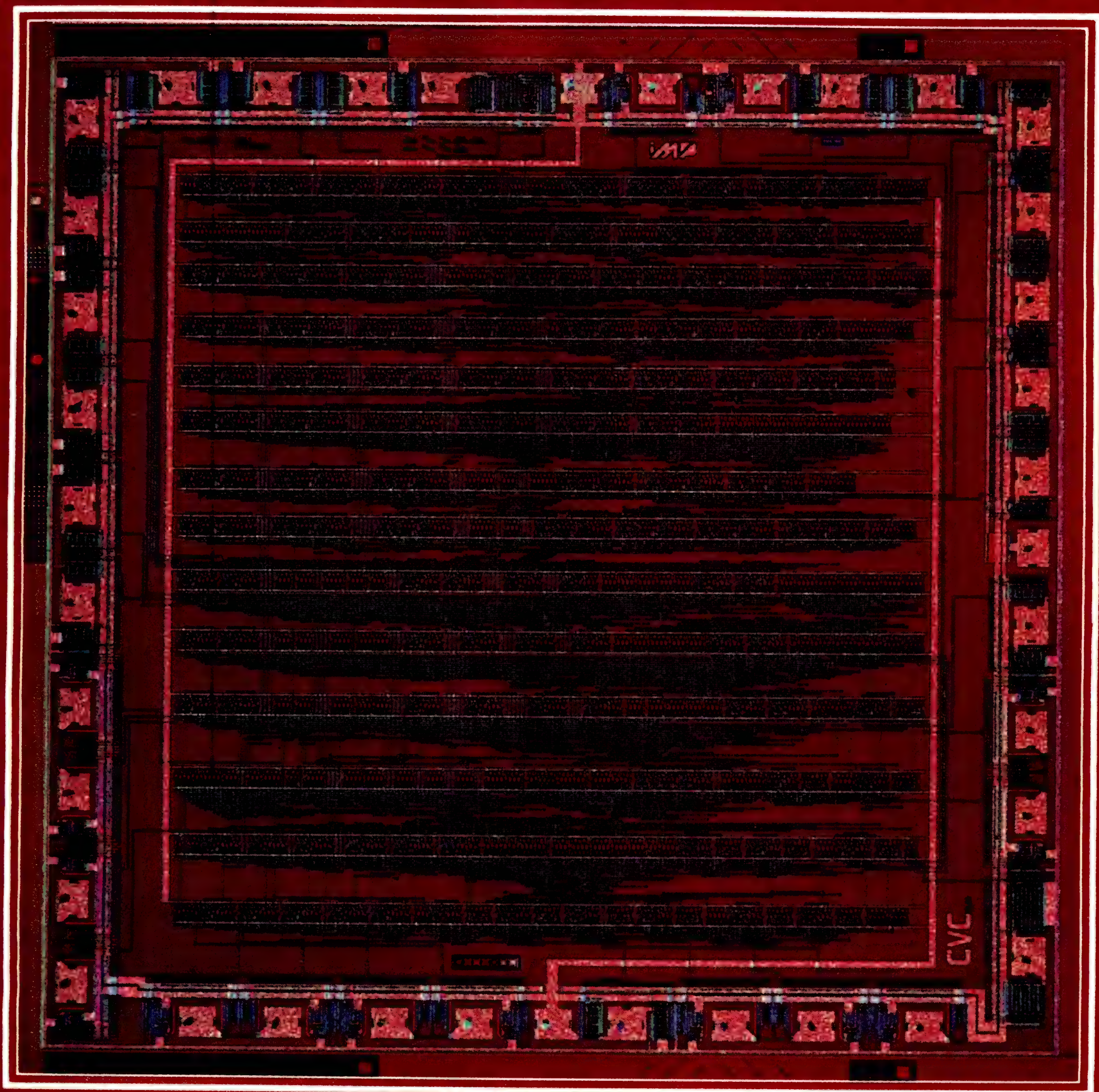

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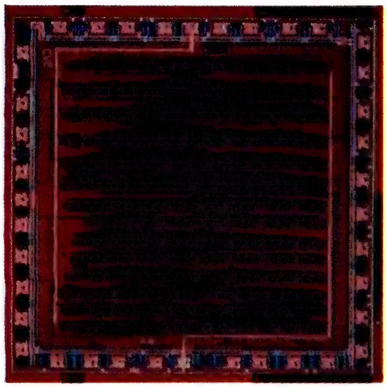

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Keyword Index

EDN TECHNICAL-ARTICLE DATABASE

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A/D converters

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A-d converter-filter chip serves as front end for digital signal processing. *Mok, Tsung D, EG&G Reticon; Ambrose, John R, EG&G Reticon; Electronic Design, 09/06/84, pg 205, 7 pgs.*

Analog converters, sample-and-hold amps lead the way to a world of ideal design parameters. *Goodenough, Frank, Technology Editor; Electronic Design, 09/06/84, pg 106, 29 pgs.*

Converters gain speed, resolution. *Bindra, Ashok, Components; Electronics Week, 08/20/84, pg 63, 6 pgs.*

Data Converters. *Travis, Bill, Associate Editor; EDN, 06/14/84, pg 118, 21.5 pgs.*

FIFO eases ADC-to-UART interface. *Freeman, Wes, Teledyne Semiconductor; EDN, 08/09/84, pg 274, 1.5 pgs.*

Floating-point converter uses hardware to get a 20-bit dynamic range. *Burrier, Richard, Raytheon; et al,, Electronic Design, 09/06/84, pg 175, 10 pgs.*

Increased A/D resolution improves image processing. *Chocheles, Ellen H, TRW/LSI Products; Electronic Products, 10/15/84, pg 69, 5.5 pgs.*

Monitor detects status changes. *Murugesan, S, ISRO Satellite Centre; EDN, 07/12/84, pg 335, 1 pg.*

Monolithic a-d converter interfaces directly with most microprocessors. *Moore, Stephen, Precision Monolithics; Pietkiewicz, Steve, Precision Monolithics; Electronic Design, 09/06/84, pg 191, 8 pgs.*

Numerical-integration techniques speed dual-slope A/D conversion. *Grandbois, Gary, Teledyne Semiconductor; Freeman, Wes, Teledyne Semiconductor; EDN, 10/31/84, pg 147, 7.5 pgs.*

Track-and-holds take flash converters to their limits. *Neal, Jerry, Analog Devices/Computer Labs; Surber, Jim, Analog Devices; Electronic Design, 05/03/84, pg 381, 7 pgs.*

Watch for superposition errors in data-converter applications. *Michaels, Stuart R, ILC Data Device; EDN, 09/20/84, pg 255, 4 pgs.*

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Calculator program designs filters built around MF10 switched-capacitor IC. *Slife, Jim, GTE Lenkurt/Special Service Products; et al,, Electronic Design, 09/20/84, pg 302, 3.33 pgs.*

Compute lowpass filter responses for special driving functions. *Cobb, Raymond F, Harris; EDN, 05/03/84, pg 265, 7 pgs.*

Extend BASIC FFT capabilities to handle many filter types. *Cobb, Raymond F, Harris; EDN, 06/14/84, pg 183, 9.5 pgs.*

New tools tackle switched-cap net designs. *Zuppardo, Joe, Associate Editor; Electronic Products, 09/03/84, pg 41, 8.33 pgs.*

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Switched-capacitor ICs simplify filter design. *Davis, A M, San Jose State University; Small, W Timothy, EG&G Reticon; EDN, 06/14/84, pg 197, 10.5 pgs.*

Techniques simplify active filters. *Cereijo, Manuel, Florida Int'l University; EDN, 06/28/84, pg 280, 1.67 pgs.*

Varying input clock rate fine-tunes filters' cutoff frequencies. *Lubs, Steve, Electronic Design, 06/28/84, pg 293, 1 pg.*

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Eight ICs form bipolar log amp. *Barnett, Thomas, London Hospital; EDN, 05/31/84, pg 207, 1 pg.*

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Monolithic power-buffer IC drives difficult loads. *Williams, Jim, Linear Technology; EDN, 08/09/84, pg 153, 7 pgs.*

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Analog board cuts data acquisition costs using STD bus. *Davis, Andrew, Data Translation; Connors, Steve, Data Translation; Computer Design, 10/15/84, pg 121, 4 pgs.*

Analog signal processing

Analog chip set smoothes out digital signal processing. *Hester, Richard, Texas Instruments/Central Research Labs; Electronic Design, 05/17/84, pg 243, 5.5 pgs.*

Image signal processor computes fast enough for gray-scale video. *Fukushima, Tadashi, Hitachi; Electronic Design, 10/04/84, pg 209, 7 pgs.*

Take advantage of thermal effects to solve circuit-design problems. *Williams, Jim, Linear Technology; EDN, 06/28/84, pg 239, 9 pgs.*

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Monolithic CMOS-switch IC suits diverse applications. *Williams, Jim, Linear Technology; EDN, 10/04/84, pg 183, 11 pgs.*

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Array processor tamed by structural innovations. *Krishna, Shailendra, Design Engineer; Frisch, Robert, Mercury Computer Systems; Electronic Products, 08/15/84, pg 77, 4.33 pgs.*

Systolic array chip matches the pace of high-speed processing. *Davis, Ronald, NCR; Electronic Design, 10/31/84, pg 207, 8 pgs.*

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Information technologies race to merge. *Feldt, Terry, Communications & Microwave; Rosenberg, Robert, Systems Integration; Electronics Week, 09/24/84, pg 57, 11 pgs.*

LISP software-development environments increase programmer productivity. *Marrin, Ken, Associate Editor; EDN, 08/23/84, pg 89, 5.33 pgs.*

Practical tools earn AI new level of respectability. *Spitznogle, Frank, LISP Machine; Computer Design, 09/84, pg 197, 3.75 pgs.*

Software tool packages the expertise needed to build expert systems. *Williams, Chuck, Inference; Electronic Design, 08/09/84, pg 153, 10.5 pgs.*

Software tools, tailored architectures extend LISP and Smalltalk capabilities. *Marrin, Ken, Associate Editor; EDN, 10/04/84, pg 53, 6 pgs.*

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VLSI testers help guarantee chip quality. *Kline, Scott, Megatest; Electronics Week, 10/29/84, pg 63, 4 pgs.*

Versatile tester takes guesswork out of finding µP-based system faults. *Swan, William, Applied Microsystems; Electronic Design, 05/03/84, pg 341, 6 pgs.*

B

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CRTs and monitors

Color monitors. *Wright, Maury, Western Editor; EDN, 05/31/84, pg 106, 14 pgs.*

High-resolution CRTs hold their lead, despite the rise of compact plasma panels. *Costlow, Terry, Midwestern Editor; Electronic Design, 07/12/84, pg 112, 8 pgs.*

Cabinets and enclosures

19-in. cabinets sport shielding for FCC compliance. *Marrin, Ken, Associate Editor; EDN, 07/12/84, pg 156, 9 pgs.*

Industrial Interconnect Devices. *McDermott, Jim, Special Features Editor; EDN, 08/09/84, pg 128, 14 pgs.*

Capacitors

Ceramic chip capacitors decrease noise in DIP-mounted digital ICs. *Biswas, Ranjit, Electronic Design, 07/12/84, pg 193, 3 pgs.*

Demand for compact high-frequency units inspires new capacitor types and sizes. *McDermott, Jim, Special Features Editor; EDN, 10/04/84, pg 91, 8 pgs.*

Metalized-film capacitors take new shot at IC decoupling. *Richardson, Dave, TRW/Electronic Components; von Kampen, Ted, TRW/Capacitor; Electronic Products, 05/15/84, pg 115, 3.33 pgs.*

Charge-coupled devices

Standard-cell core µPs evolve slowly but promise bright future. *Travis, Bill, Senior Editor; EDN, 10/18/84, pg 53, 6.67 pgs.*

Circuit packages

Semiconductor Technology. *Biancomano, Vincent, Technology Editor; Electronic Design, 06/14/84, pg 0, 11 pgs.*

Clipper circuits

Circuit uses only resistors, diodes. *Morgan, Dennis, General Electric; EDN, 05/17/84, pg 213, 0.67 pgs.*

Comparators

Build word comparators with three ICs. *Pease, Robert A, National Semiconductor; EDN, 09/06/84, pg 228, 1 pg.*

Window comparator provides hysteresis. *Ferriss, Licoln, Singer; EDN, 08/23/84, pg 240, 1.5 pgs.*

Computer interfaces, other

Efficient I/O unleashes benefits of open bus concept. *Cory, Chappell, Xylogics; Jackson, George, Xylogics; Computer Design, 10/01/84, pg 157, 6 pgs.*

Special boards solve tough application problems. *Persun, Terry, Associate Editor; Electronic Products, 06/18/84, pg 65, 5 pgs.*

Two-chip set cleans up controller design for streaming-tape drives. *Vakil, Vik, Western Digital; Doshi, Raj, Western Digital; Electronic Design, 09/20/84, pg 225, 7 pgs.*

Computer peripherals, other

Pointing-device innovations enhance user/machine interfaces. *Comerford, Richard, Senior Editor; EDN, 07/26/84, pg 54, 10.5 pgs.*

Computer software, communications

Hardware-specific software packages adapt BASIC to data-acquisition tasks. *Powers, Don, Associate Editor; EDN, 09/06/84, pg 55, 7.33 pgs.*

Software reduces costs of local-area networking. *Powers, Don, Associate Editor; EDN, 05/31/84, pg 51, 5 pgs.*

Computer software, graphics

Anatomy of a graphics editor–the inside story. *Hamm, Terry, Communication Dynamics; Bergstedt, Gar, Communication Dynamics; Computer Design, 05/84, pg 187, 5 pgs.*

GKS-based graphics software adapts to changing technologies. *Waggoner, Clinton N, Nova Graphics International; EDN, 05/31/84, pg 127, 5.5 pgs.*

Is GKS powerful enough for the applications? *Wright, Thomas, Integrated Software Systems; Computer Design, 05/84, pg 211, 3 pgs.*

Proprietary/standard graphics software mix to give more. *Davis, Andrew, Tektronix; Computer Design, 05/84, pg 229, 5 pgs.*

VDI promises graphics software portability. *Langhorst, Fred, Digital Research; Computer Design, 05/84, pg 197, 5.5 pgs.*

Computer software, other

A few statement types adapt C language to parallel processing. *Naeini, Ray, Flexible Computer; Electronics Week, 06/28/84, pg 125, 5 pgs.*

A module approach to microcomputer operating systems. *Little, John, Multi Solutions; Computer Design, 07/84, pg 217, 5.75 pgs.*

A three-part compiler heralds the arrival of microprocessor standards. *Wolf, Lowell, Digital Research; Electronic Design, 08/23/84, pg 229, 7 pgs.*

Actors set the stage for software advances. *Pugh, John R, Carleton University/School of Computer Science; Computer Design, 09/84, pg 185, 4 pgs.*

Advanced Computer Languages. *Bryce, Heather, Field Editor; Electronic Design, 05/03/84, pg 229, 14 pgs.*

Advanced language leads to smoother designing with programmable logic. *Burrier, Daniel, Data I/O; Electronic Design, 08/09/84, pg 247, 9 pgs.*

Analog software comes of age. *Grossman, Morris, Special Features Editor; Electronic Products, 08/01/84, pg 44, 5 pgs.*

Choosing the best operating system. *Hatch, Theodore F, Honeywell; et al,, Computer Design, 10/01/84, pg 171, 5 pgs.*

Component-based operating system works in real time. *Funck, Gary, Hunter & Ready; Computer Design, 07/84, pg 203, 6.5 pgs.*

Disk translation software solves format mismatches. *Mitchell, George, Contributing Editor; Computer Design, 05/84, pg 123, 3.5 pgs.*

Dual port solves compatibility problem. *Bott, Ross A, Pyramid Technology; Computer Design, 08/84, pg 205, 8 pgs.*

EE software for design tasks spreads use of personal computers. *Small, Charles H, Associate Editor; EDN, 09/20/84, pg 63, 5.5 pgs.*

Evolution of future microcomputer operating systems. *Alia, Vincent, Digital Research; Gysin, Gary, Digital Research; Computer Design, 07/84, pg 187, 9 pgs.*

Fault-tolerant mini needs enhanced operating system. *Glazer, Samuel D, Auragen Systems; Computer Design, 08/84, pg 189, 7 pgs.*

Fifth-generation computing: dedicated software is the key. *Hindin, Harvey J, Special Features Editor; Computer Design, 09/84, pg 150, 11.5 pgs.*

Forth word simplifies numeric data entry. *Anthony, Jeffrey, Corby Industries; Electronic Design, 09/06/84, pg 268, 1.25 pgs.*

Generating CRCs with software. *Grappel, Robert, MIT Lincoln Laboratory; EDN, 10/31/84, pg 205, 1 pg.*

LISP software-development environments increase programmer productivity. *Marrin, Ken, Associate Editor; EDN, 08/23/84, pg 89, 5.33 pgs.*

Lack of federal software-protection law produces inefficient, incomplete coverage. *Clifford, Ralph D, Attorney at Law; EDN, 06/28/84, pg 347, 2 pgs.*

Logic design software casts workstation in role of manufacturer's aide. *Perry, Richard, LSI Logic; Hayes, Dennis, LSI Logic/CAD; Electronic Design, 05/31/84, pg 267, 5.5 pgs.*

Micro operating systems yield mixed blessings. *Hindin, Harvey J, Special Features Editor; Computer Design, 07/84, pg 155, 9 pgs.*

Minicomputer system offers time-sharing and realtime tasks. *Sherrod, Phil, S&H Computer Systems; Brenner, Stephen, S&H Computer Systems; Computer Design, 08/84, pg 223, 5 pgs.*

Multistage compilers move from mainframes to micros. *Bassett, Sam, Field Editor; Computer Design, 06/01/84, pg 45, 1.33 pgs.*

Object models simplify and speed system design. *Passon, Gary L, Telenova; Computer Design, 07/84, pg 231, 6.5 pgs.*

Operating system extensions link disparate systems. *Row, John, Applied Intelligence; Daugherty, David, Applied Intelligence; Computer Design, 07/84, pg 171, 7.5 pgs.*

Operating system features real time and fault tolerance. *Snead, Bob, AT&T; et al,, Computer Design, 08/84, pg 177, 6 pgs.*

Operating systems abound for the IBM PC/XT and clones. *Powers, Don, Associate Editor; EDN, 10/31/84, pg 115, 19 pgs.*

Operating systems for minis emphasize UNIX compatibility. *Hindin, Harvey J, Speical Features Editor; Computer Design, 08/84, pg 165, 6.5 pgs.*

Packaged-software market to see tenfold increase. *Stubbs, George, Assistant Editor; EDN, 06/28/84, pg 362, 0.25 pgs.*

Personal-computer-based software helps you to limit CAE costs. *Prasad, Roy, Personal CAD Systems; EDN, 09/20/84, pg 207, 5.5 pgs.*

Portable native-code package suits 8- to 32-bit micros. *Smith, Thorn, Zilog; Computer Design, 06/15/84, pg 145, 7 pgs.*

Practical tools earn AI new level of respectability. *Spitznogle, Frank, LISP Machine; Computer Design, 09/84, pg 197, 3.75 pgs.*

Short software routine quickly generates pseudorandom numbers. *Breemer, Jan D, Technician; Electronic Design, 06/28/84, pg 296, 0.66 pgs.*

Silicon compiler lets system makers design their own VLSI chips. *Johnson, Stephen C, Silicon Compilers; Electronic Design, 10/04/84, pg 167, 15 pgs.*

Software aids in PAL circuit design, simulation, and verification. *Schmitz, Nick, Monolithic Memories; Greiner, Jerry, Monolithic Memories; Electronic Design, 05/31/84, pg 243, 8 pgs.*

Software development evolves into software engineering. *Batni, Ramachendra P, ITT Telecom; Computer Design, 09/84, pg 165, 5 pgs.*

Software engineering with personal computers. *Villapiano, Gavin, Electronic Design, 05/31/84, pg 109, 14 pgs.*

Software fault tolerance staves off the errors that besiege µP systems. *Jarrett, Dick, Software Consultant; Electronic Design, 08/09/84, pg 187, 10.5 pgs.*

Software mixes graphics with text on screen. *Boucher, David A, Interleaf; Electronic Products, 10/01/84, pg 51, 4 pgs.*

Software package lets PC control instruments with a touch. *Haroldsen, Douglas R, Optimatic Solutions; Electronic Design, 10/31/84, pg 180, 9 pgs.*

Software quality: design it in from the start. *Ghiassi, M, National Semiconductor; Computer Design, 08/84, pg 91, 5 pgs.*

Software standards will usher in the age of graphics. *Panasuk, Curtis, West Coast Editor; Electronic Design, 07/12/84, pg 94, 10 pgs.*

Software tools automate structured analysis. *Kerth, Norman L, Tektronix; Electronics Week, 08/20/84, pg 69, 4 pgs.*

Software tools, tailored architectures extend LISP and Smalltalk capabilities. *Marrin, Ken, Associate Editor; EDN, 10/04/84, pg 53, 6 pgs.*

Supervisory software ties semicustom tools into a fully automated bundle. *Lydick, Richard, RCA; Morris, Stephen, RCA; Electronic Design, 06/14/84, pg 289, 6.5 pgs.*

Toolkit extends the benefits of Lisp-based computer to Fortran programming. *Hirsch, Abe, Symbolics; Electronic Design, 05/31/84, pg 193, 8 pgs.*

Workstation software manages project schedules, costs, and resources. *Massey, Anita, Tektronix; Electronic Design, 10/18/84, pg 185, 7.5 pgs.*

Computer software, performance measurement

Z80 routine tests RAM at power-on. *Dean, Paul, Sperry; EDN, 10/18/84, pg 325, 1 pg.*

Computer-aided design/manufacturing (CAD/CAM)

Integrating the engineer's environment. *Evanczuk, Stephen, Contributing Editor; Electronics Week, 05/17/84, pg 121, 9 pgs.*

PC-based CAD can't do it all. *Monego, Philip J, Paragon Technology; Electronic Products, 10/01/84, pg 57, 2.5 pgs.*

VLSI circuit design reaches the level of architectural description. *Johnson, Stephen C, Silicon Compilers; Electronics Week, 05/03/84, pg 121, 8 pgs.*

Weigh pc-board CAD choices to match price and performance. *Peddie, Cynthia, Paragon Technology; EDN, 09/20/84, pg 221, 7.5 pgs.*

Computers, other

Comdex sessions and exhibited products will help designers gauge computer market. *Teja, Ed, Western Editor; EDN, 10/31/84, pg 69, 2 pgs.*

Information technologies race to merge. *Feldt, Terry, Communications & Microwave; Rosenberg, Robert, Systems Integration; Electronics Week, 09/24/84, pg 57, 11 pgs.*

Intelligent computing era takes off. *Highberger, Deb, Sr Associate Editor; Edson, Dan, Contributing Editor; Computer Design, 09/84, pg 78, 13.5 pgs.*

NCC exhibits prove commercial viability of networking schemes and products. *Comerford, Richard, Senior Editor; EDN, 09/20/84, pg 79, 10.33 pgs.*

NCC program close-up. *Panasuk, Curtis, West Coast Editor; Electronic Design, 06/28/84, pg 97, 3.5 pgs.*

Parallel architectures put fifth-generation machines on the right track. *Patton, Carole, East Coast Editor; Electronic Design, 05/03/84, pg 174, 14 pgs.*

Tagged architecture supports symbolic processing. *Hirsch, Abraham, Symbolics; Computer Design, 06/01/84, pg 75, 5 pgs.*

Ten computer experts contemplate the future. *Staff; Electronic Design, 05/03/84, pg 201, 21 pgs.*

Conferences/conventions/shows

Autofact 6, *Computer Design, 09/84, pg 247, 2.5 pgs.*

Comdex sessions and exhibited products will help designers gauge computer market. *Teja, Ed, Western Editor; EDN, 10/31/84, pg 69, 2 pgs.*

Electro program close-up. *Gold, Martin, Editor-at-large; Electronic Design, 05/03/84, pg 121, 5.5 pgs.*

Electro/84. *Asbrand, Deborah, Assistant Editor; Stubbs, George, Assistant Editor; EDN, 05/03/84, pg 127, 10 pgs.*

Electronica 84 conference program maintains high technical content. *Harold, Peter, European Editor; EDN, 10/31/84, pg 75, 1.33 pgs.*

Midcon '84. *Weghorn, Frank, Sr News Editor; Electronic Products, 09/03/84, pg 84, 8 pgs.*

Mini/Micro program close-up. *Gold, Martin, Editor-at-large; Electronic Design, 05/03/84, pg 133, 4 pgs.*

Mini/Micro southwest computer conference and exhibition. *Computer Design, 08/84, pg 65, 2 pgs.*

NCC exhibits prove commercial viability of networking schemes and products. *Comerford, Richard, Senior Editor; EDN, 09/20/84, pg 79, 10.33 pgs.*

NCC program close-up. *Panasuk, Curtis, West Coast Editor; Electronic Design, 06/28/84, pg 97, 3.5 pgs.*

NCC sessions to highlight software developments. *Comerford, Richard, Senior Editor; EDN, 06/28/84, pg 167, 4 pgs.*

SID 84 to highlight global advances in TV, flat panels, large-area displays. *Ormond, T, Senior Editor; EDN, 05/31/84, pg 65, 3.67 pgs.*

Standards bring the future one step closer. *Weiss, Ray, Electronic Design, 10/18/84, pg 97, 9 pgs.*

WESCON/84. *Clarke, Robert M, Assistant Editor; EDN, 10/18/84, pg 135, 8.33 pgs.*

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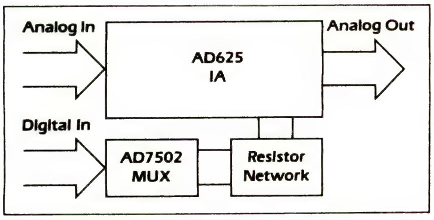

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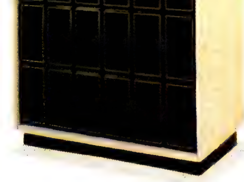

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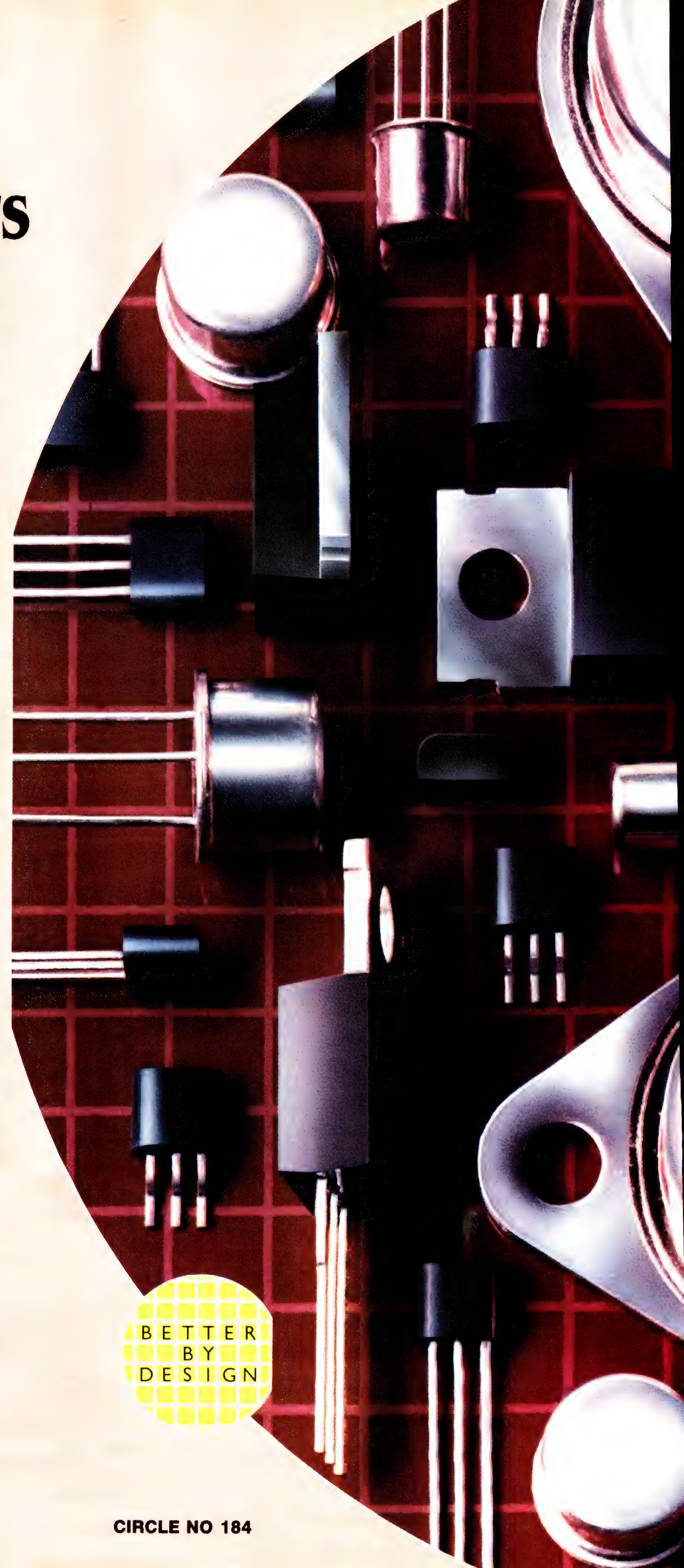

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Connectors-the mising link in EMI suppression. *Drzymkowski, Frank, ITT Cannon; Goodman, Dave, ITT Cannon; Computer Design, 08/84, pg 77, 6 pgs.*

Filtered connectors fight the EMI gremlins. *Boutros, Kamal, Amphenol Products; Electronic Products, 07/02/84, pg 79, 3.33 pgs.*

Industrial Interconnect Devices. *McDermott, Jim, Special Features Editor; EDN, 08/09/84, pg 128, 14 pgs.*

Ribbon cable and IDCs make the connection. *Wiater, Mike, Thomas & Betts/Ansley Electronics; Electronic Products, 08/15/84, pg 71, 4.66 pgs.*

Counters

Build a frequency counter from a µC. *Valiant, H D, Dept of Energy, Mines and Resources; EDN, 08/23/84, pg 244, 0.75 pgs.*

Circuit disables up/down counters. *Perry, John, PCA International; EDN, 05/17/84, pg 214, 0.67 pgs.*

Hybrid design improves counters. *Inkol, Robert, National Defense; EDN, 05/31/84, pg 214, 1 pg.*

PROM and octal latch make a simple, versatile 7-bit counter. *Rao, Vital, ISRO Satellite Centre; Electronic Design, 10/4/84, pg 275, 1.67 pgs.*

Current sources

Floating driver and MOSFET create universal current source and sink. *Salvati, M J, Flushing Communications; Electronic Design, 08/09/84, pg 265, 1.33 pgs.*

Precision voltage to single-ended current source sidesteps CMRR problems. *Baert, D, State University of Ghent/Electronics Lab; et al, Electronic Design, 06/14/84, pg 320, 1 pg.*

D

D/A converters

Analog converters, sample-and-hold amps lead the way to a world of ideal design parameters. *Goodenough, Frank, Technology Editor; Electronic Design, 09/06/84, pg 106, 29 pgs.*

Complete DAC chip weds true monotonicity to 16-bit resolution. *Guy, Tom, Analog Devices; Grant, Doug, Analog Devices; Electronic Design, 06/14/84, pg 273, 9 pgs.*

Converters gain speed, resolution. *Bindra, Ashok, Components; Electronics Week, 08/20/84, pg 63, 6 pgs.*

Data Converters. *Travis, Bill, Associate Editor; EDN, 06/14/84, pg 118, 21.5 pgs.*

High-speed video D/A converters simplify graphics-display designs. *Castleberry, Randel, TRW LSI; EDN, 05/31/84, pg 185, 5.5 pgs.*

Quad voltage-output DAC trims the offsets of up to four op amps. *Byrne, Mike, Analog Devices; Wynne, John, Analog Devices; Electronic Design, 08/23/84, pg 248, 1.75 pgs.*

Watch for superposition errors in data-converter applications. *Michaels, Stuart R, ILC Data Device; EDN, 09/20/84, pg 255, 4 pgs.*

DPSK modulators

Comparator produces narrow pulses. *Kuklewicz, John, Advanced Micro Devices; EDN, 05/03/84, pg 329, 1.33 pgs.*

DTMF ICs

DTMF encoder draws no standby current, thus eliminating on/off switch. *Kosco, Edward G, Sperry Defense Electronics; Electronic Design, 05/03/84, pg 395, 1.25 pgs.*

Data acquisition and communications, other

Analog board cuts data acquisition costs using STD bus. *Davis, Andrew, Data Translation; Connors, Steve, Data Translation; Computer Design, 10/15/84, pg 121, 4 pgs.*

Designing analog data-collection circuits. *Chase, Don, Analogic; Electronic Products, 05/15/84, pg 76, 6.66 pgs.*

From analog to digital in data acquisition. *Schenkel, Jeffrey, Hybrid Systems; Electronic Products, 05/15/84, pg 85, 4 pgs.*

PCs invade data acquisition with I/O interface. *Supernault, Shari L, Data Translation; Electronic Products, 06/04/84, pg 85, 4.33 pgs.*

Data communications

Bit-oriented coprocessor resolves incompatibilities of small and large networks. *Madan, Pradip, Exel Microelectronics; et al, Electronic Design, 07/26/84, pg 155, 9 pgs.*

Chip family combines voice and data communications. *Dunn, Susan, Motorola; Mouton, Al, Motorola; EDN, 05/03/84, pg 229, 6.5 pgs.*

Chips support two local area networks. *Dahlberg, Bob, Intel; Computer Design, 05/84, pg 107, 5 pgs.*

Data-acquisition system for PCs packs powerful tools. *Sostek, Ron, Cyborg; Ciociolo, Jim, Product Specialist; Electronic Products, 08/01/84, pg 65, 4.66 pgs.*

Eight UARTs on one chip slash parts count and simplify multiplexing. *Blake, William C, Digital Equipment; et al, Electronic Design, 09/20/84, pg 187, 6.5 pgs.*

Emulate SDLC/HDLC controllers. *Richardson, Robert M, Richcraft Engineering; EDN, 10/18/84, pg 326, 5.67 pgs.*

Formal protocol specification ready to make its mark. *Hindin, Harvey J, Special Features Editor; Computer Design, 06/15/84, pg 57, 6.75 pgs.*

From analog to digital in data acquisition. *Schenkel, Jeffery, Hybrid Systems; Electronic Products, 07/16/84, pg 74, 5 pgs.*

Intelligent host adapter directs I/O traffic, freeing up host processor. *Snively, Robert, Adaptec; Electronic Design, 09/20/84, pg 243, 6.5 pgs.*

Leased-line and videotex applications are targets of one-chip modem. *Eidson, Stevan, Advanced Micro Devices; Electronics Week, 07/12/84, pg 119, 5 pgs.*

Monitor communications between computers. *Massery, Dean, Microcontrol Systems; EDN, 10/04/84, pg 254, 0.5 pgs.*

Optimize the hybrid interface to increase modem dynamic range. *Single, Peter, National Semiconductor; EDN, 10/18/84, pg 279, 7 pgs.*

Serial backplane suits multiprocessor architectures. *Webb, Mike, Intel; Computer Design, 07/84, pg 85, 6.75 pgs.*

Single chip unlocks phase-shift keying for 1200-bit/s modem. *Hanson, Kerry, Texas Instruments; Electronic Design, 06/14/84, pg 261, 7 pgs.*

Twisted-pair bus carries speech, data, text, and images. *Bourgonje, Wouter, Philips International BV; Electronic Design, 07/26/84, pg 171, 7 pgs.*

Database managers

Development tool helps write integrated software for personal computers. *McMahon, William J, Jetsoft; Electronic Design, 08/09/84, pg 171, 7 pgs.*

The coming surge in data-base systems. *Manuel, Tom, Senior Editor/Info Systems; Electronics Week, 05/17/84, pg 131, 13 pgs.*

Debounce circuits

Pushbutton circuit sends a bounce-free pulse or a string of timed pulses. *Bohlman, Eric, OMS Development; Electronic Design, 06/14/84, pg 322, 1 pg.*

Delay lines

Pc-board LC delay line controls strobe pulses for dynamic RAM arrays. *Wingate, David, Electronic Design, 05/03/84, pg 396, 1.75 pgs.*

Development systems

Add-on development package stretches microprocessor choices. *Hagerty, Michael, Language Resources; Electronic Design, 05/03/84, pg 333, 4.5 pgs.*

Analyzers stamp out µC software bugs. *Baldridge, Ron, Associate Editor; Electronic Products, 09/03/84, pg 59, 6 pgs.*

Development tool debugs entire microcoded systems down to VLSI chips. *Wilburn, Darrel, Step Engineering; Mick, John, Step Engineering; Electronic Design, 06/28/84, pg 169, 8 pgs.*

Microprogramming tools promise VLSI-design solutions. *Small, Charles H, Associate Editor; EDN, 07/26/84, pg 210, 9 pgs.*

Digital multimeters (DMMs)

Powerful 5½-digit DMMs abound, but intended use dictates choice. *Wright, Maury, Western Editor; EDN, 08/09/84, pg 57, 7 pgs.*

Digital signal processing

16-bit-slice family creates ultrafast digital signal processors. *Garde, Doug, Analog Devices; Oxaal, John, Analog Devices; Electronic Design, 05/17/84, pg 136, 8 pgs.*

500-kHz single-board FFT system incorporates DSP-optimized chips. *Cohen, Robert, Advanced Micro Devices; Perlman, Robert, Advanced Micro Devices; EDN, 10/31/84, pg 193, 8 pgs.*

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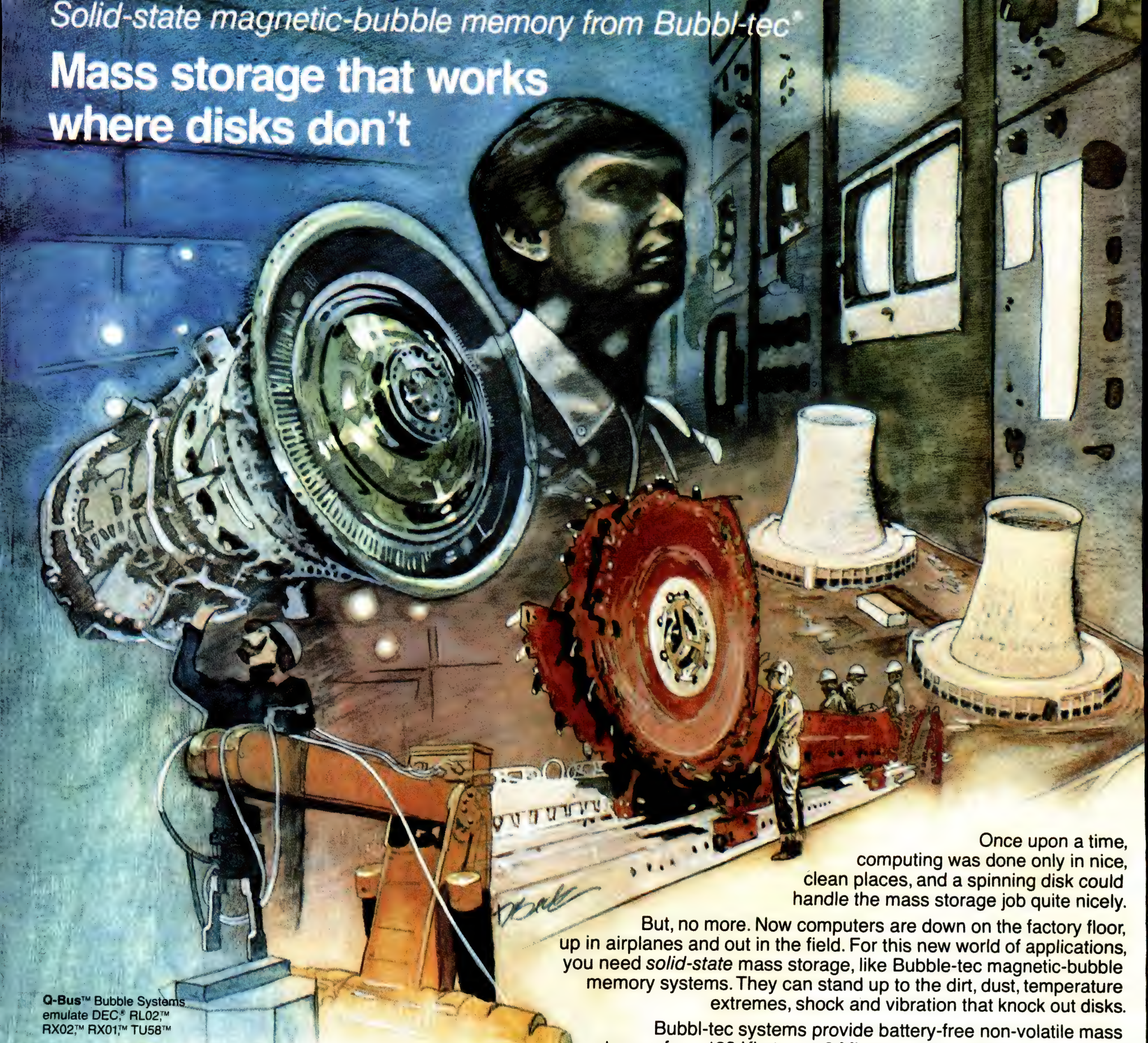

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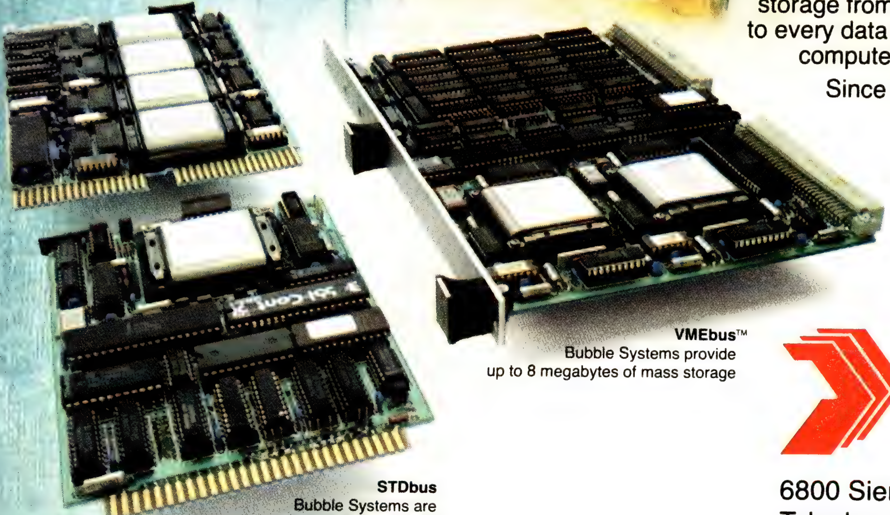

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RMS converters
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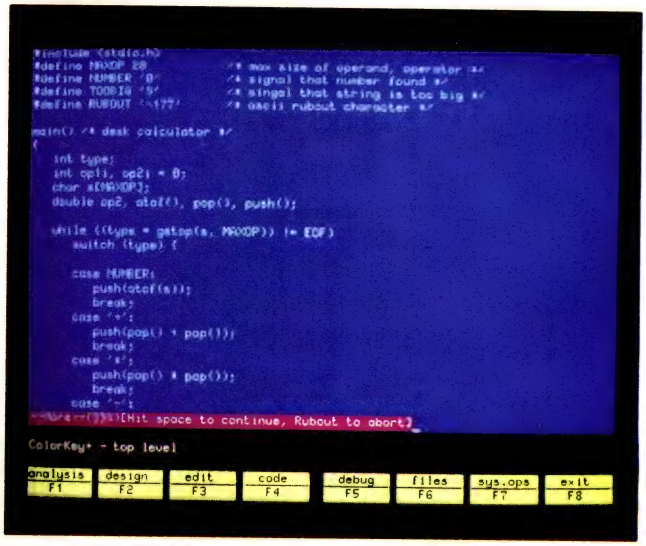

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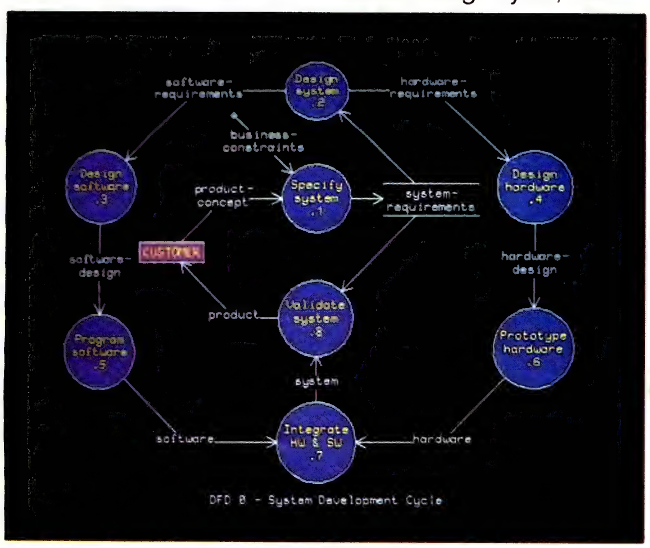

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Using personal computers as spectrum analyzers. *Darlow, Mark S, Electronics Week, 10/15/84, pg 61, 4 pgs.*

Waveform analyzers

Dynamic-signal analyzers can tune electronic components on the run. *Apker, Michael, Hewlett-Packard/Lake Stevens Instrument; Electronics Week, 05/17/84, pg 148, 4 pgs.*
Using personal computers as spectrum analyzers. *Darlow, Mark S, Electronics Week, 10/15/84, pg 61, 4 pgs.*

Winchester disk drives

3½-in. mass-storage units make their debut, cutting 5¼-in. form factor in half. *Ohr, Stephan, Technology Editor; Electronic Design, 09/20/84, pg 124, 9 pgs.*
5¼-inch Winchesters race to higher performance. *Lieberman, David, Associate Editor; Electronic Products, 07/02/84, pg 39, 10 pgs.*
Cartridge disk meets needs of portable systems. *Troutte, Dick, DMA Systems; Computer Design, 10/01/84, pg 113, 3.5 pgs.*
Half-height disk drive for 5¼-in. Winchesters stores over 100 Mbytes. *Klang, Dan, Advanced Storage Technology; Electronic Design, 06/28/84, pg 207, 6 pgs.*
Magnetic mass storage densities rise. *Rosenberg, Robert, Systems Integration; Electronics Week, 10/29/84, pg 55, 7 pgs.*
Mass storage devices keep pace with system needs. *Killmon, Peg, Senior Editor; Computer Design, 10/01/84, pg 71, 9 pgs.*
Removable disk drive provides high end muscle. *Blatchley, Carl J, Digital Equipment; et al, Computer Design, 06/15/84, pg 81, 4.75 pgs.*
Winchester disk drives. *Teja, Ed R, Western Editor; EDN, 06/28/84, pg 132, 14 pgs.*

Wire and cable

Digital signals demand high cable performance. *Shmatovich, Chris, Chabin; Electronic Products, 10/01/84, pg 77, 4 pgs.*

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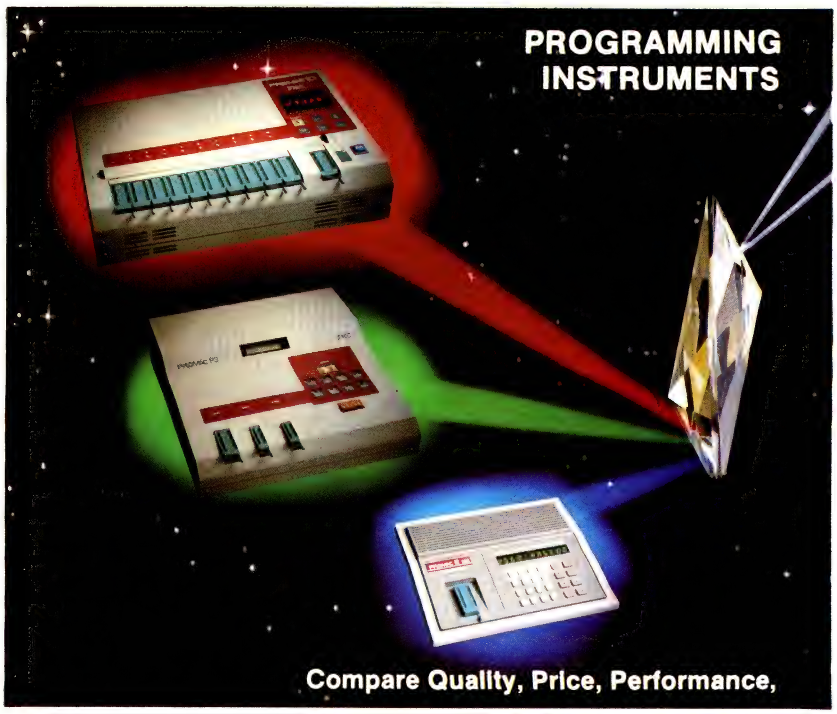

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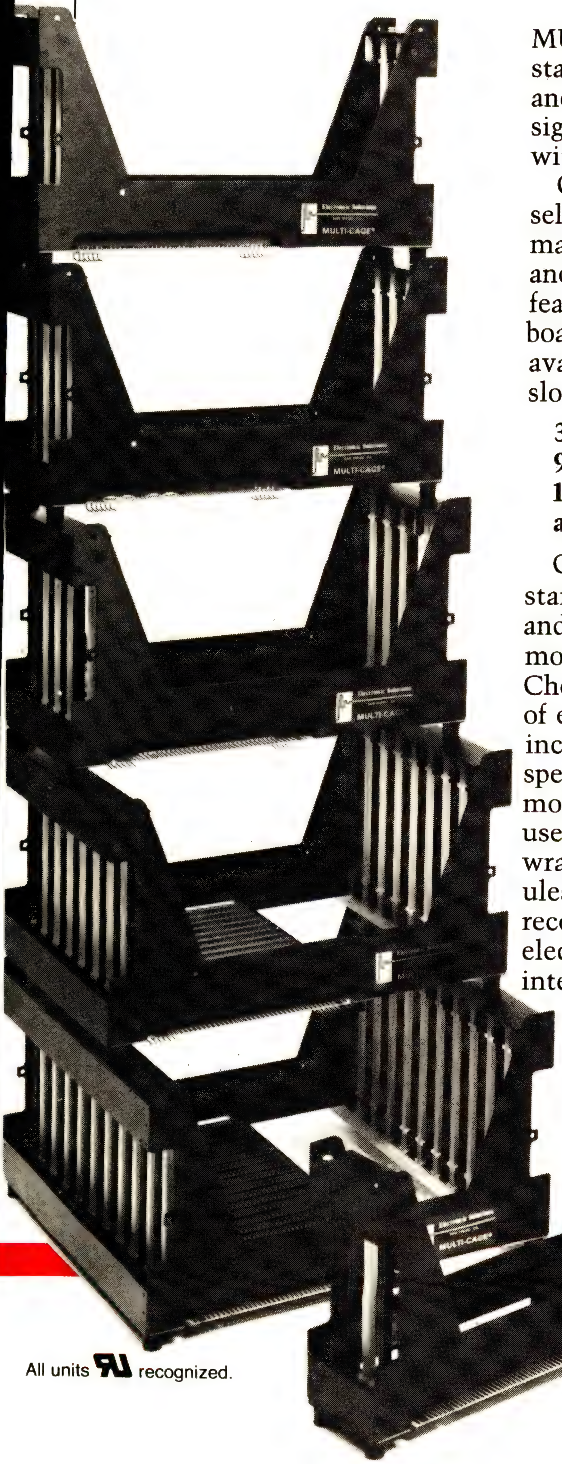

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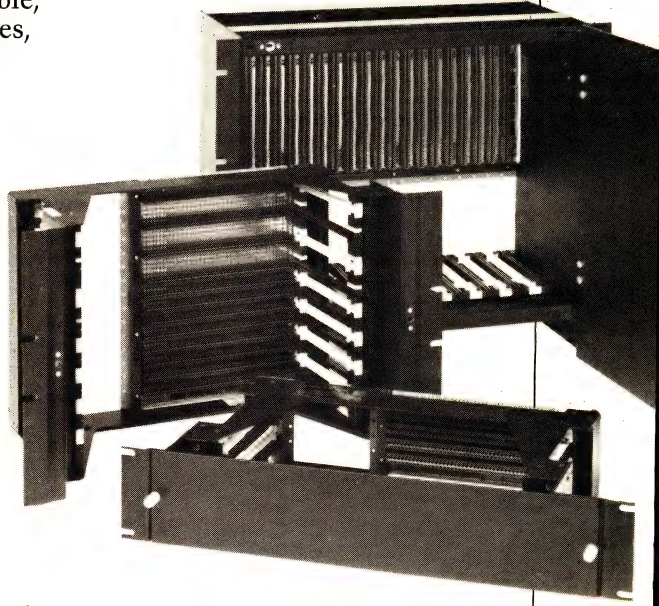

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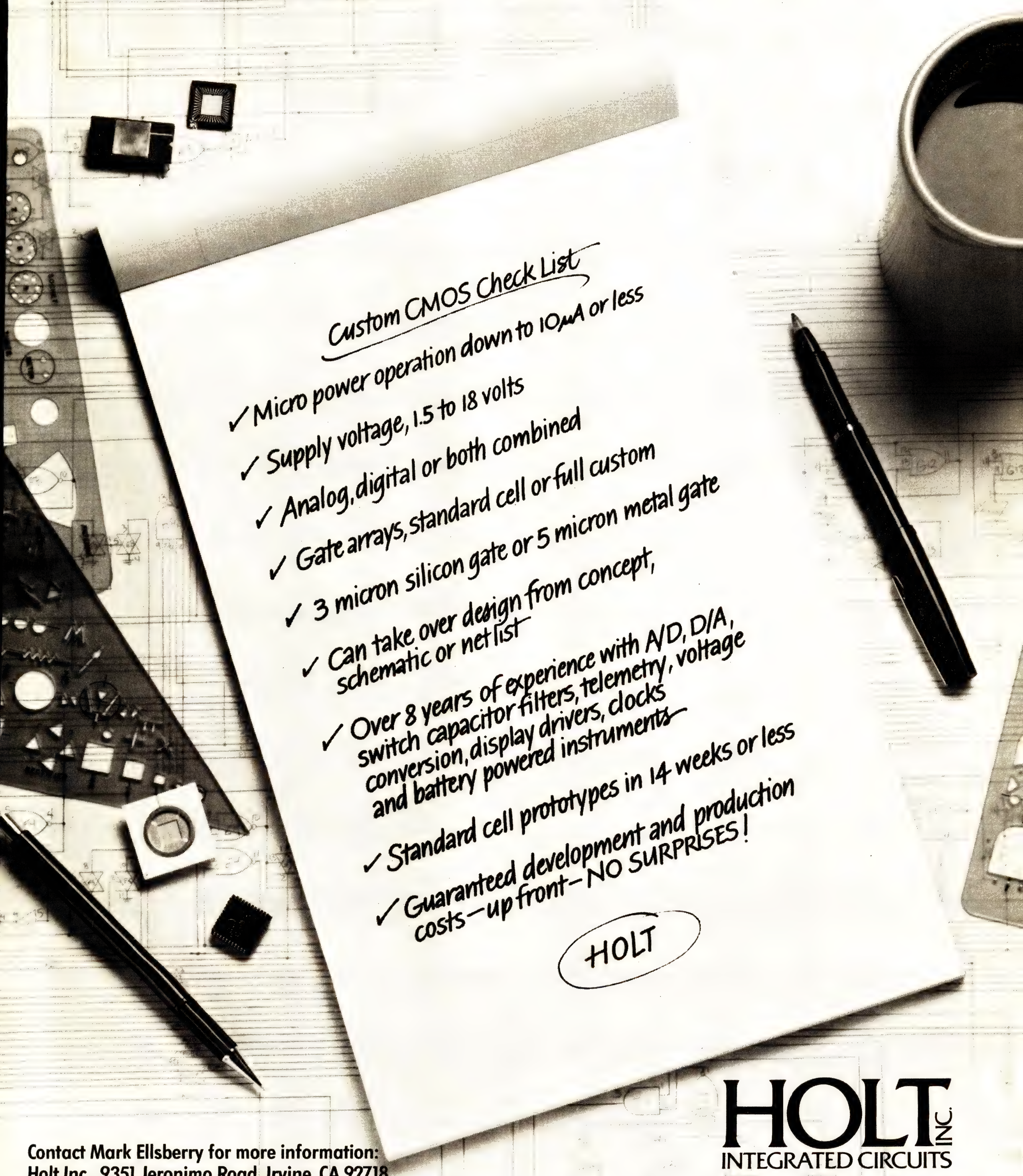

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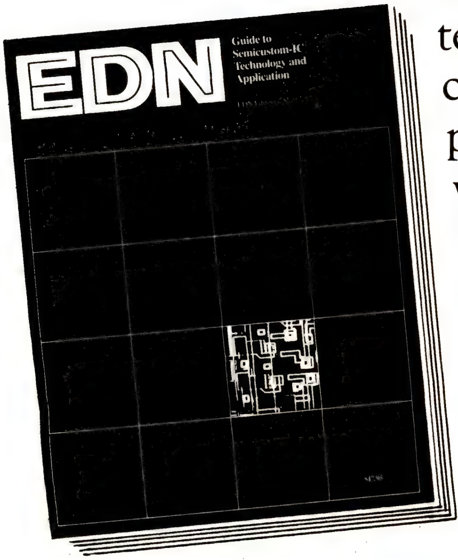

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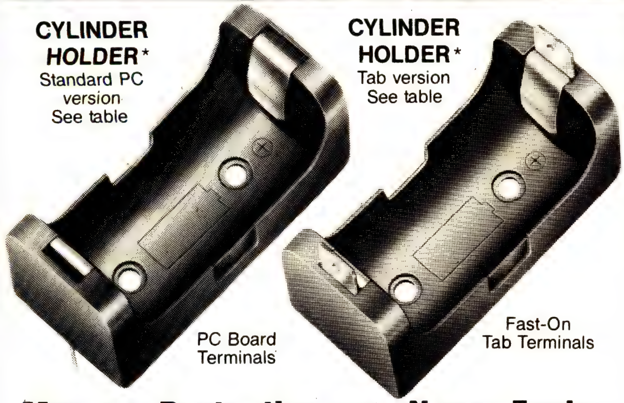

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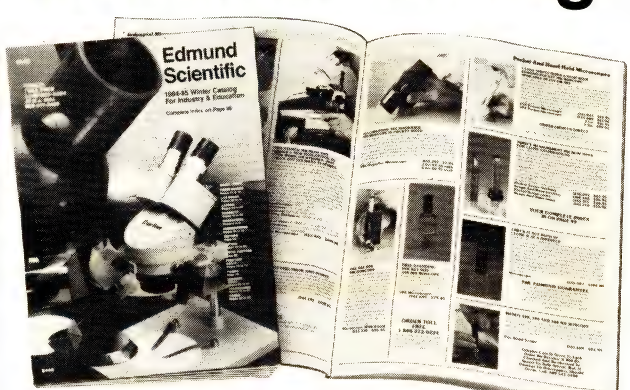

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EDN

A Guide to Electronics and Computer Industry Events

1985 Calendar

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January 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
		1 NEW YEAR'S DAY	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30	31		

- **2-4 18th Hawaii Int'l Conference on System Sciences**
Llikai Hotel, Honololu, HI. (Ralph H. Sprague Jr., Univ. of Hawaii, 2404 Maile Way Honolulu, HI 96822, 808/948-7430)
- **5-8 CES-Winter**
Las Vegas, NV (Consumer Electronics Show, 312/861-1040)
- **8 Invitational Computer Conference-ICC**
Irvine Marriott Hotel, Irvine, CA (Suzanne Hubner, B.J. Johnson and Associates Inc., 3151 Airway Ave. C-2,, Costa Mesa, CA 92625, 714/957-0171 Telex 188747 TAB Irvine)
- **8-10 Corporate Electronic Publishing Systems Conference and Showcase**
Hyatt Regency Hotel, Chicago, IL (Carol Hurley, Cahners Exposition Group 203/964-0000)
- **9-10 PC Fab Expo**
Sheraton Twin Towers Hotel, Orlando, FL (Frances Stewart, PMS-Industries 404/475-1818)
- **14-15 Symposium on Dielectric Phenomena**
Dept. of Chemistry-Brown University, Providence, RI (Edward F. Green, Brown University, Providence, RI 02912, 401/863-1192)
- **14-17 ATE West '85**
Convention Center, Anaheim, CA. (Jerry Pugh, ATE-Exhibit-Sales Morgan Grampian Exposition Group, 2 Park Ave., NY NY 10018, 212/340-9780)
- **15-16 Practical Integrated Circuit Fabrication**
Scottsdale, AZ (Pat Fruscello, ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **16 New Developments in Corporate Finance**
Airport Hilton Hotel, San Francisco CA (Georgyne Purcell, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **16-18 PC World Exposition**
Astro Hall, Houston, TX (Gene Bignami, Mitch Hall Associates, P.O. Box 860 Westwood, MA 02090, 617/329-7466)
- **16-21 AECT Commtex**
Anaheim, CA (AECT, 202/466-4780)
- **22 Basic IC Technology**
Sunnyvale, CA (Pat Fruscello, ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex 165-755 ICE, Scot)
- **22-24 1985 Annual Reliability & Maintainability Symposium**
Franklin Plaza Hotel Philadelphia, PA (H.C. Jones Westinghouse Electric Corp. MS3608 P.O. Box 1521 Baltimore, MD 21220, 301/765-7387)
- **22-24 Western Software Conference & Exposition**
San Francisco, CA (TCEI 714/661-3301)
- **22-25 UniForum**
InFomart, Dallas, TX (Marlan Stredwick, 214/655-6298)
- **23 STATUS '85**
Sunnyvale, CA (Pat Fruscello, ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **23-24 San Diego Electronics Show**
Del Mar Fairgrounds, Del Mar, CA (Electronic Representatives Association of San Diego & Epic Enterprises, 619/284-9268)
- **24 Semiconductor Purchasing Strategies**
Sunnyvale, CA (Pat Fruscello ICE, 15022 N. 75St., Scottscale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **24-26 SCS Multicon Conference**
San Diego, CA (Society for Computer Simulation 619/459-3888)
- **28-30 Office Automation Conference**
Chicago, IL (American Federation of Information Processing Societies Inc., 703/620-8900)
- **28-31 Communication Networks 1985**
Washington, DC (CW Conference Mgmt. Group, 617/879-0700)
- **28-31 Florida Instructional Computing Conference**
Orlando, FL (Educational Technology-Florida, 904/488-0980)
- **29 Invitational Computer Conference-ICC**
Adams Mark Hotel, Houston, TX (Suzanne Hubner, Joyce Cassidy, B.J. Johnson and Associates, 3151 Airway Ave., C-2, Costa Mesa, CA 92625, 714/957-0171)
- **30 Oregon High Tech Symposium**
Greenwood Inn, Beaverton, OR (Georgyne Purcell, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **30-31 IMC Pan American Conference**
Conference and Exposition on Advanced Micrographics and Office Automation, Caribe Hilton International Hotel, San Juan, Puerto Rico (International Information Management Congress, 301/983-0604)
- **31 Invitational Computer Conference**
The Lincoln Hotel, Dallas, TX (Suzanne Hubner, Joyce Cassidy, B.J. Johnson and Associates, 3151 Airway Ave., C-2, Costa Mesa, CA 92625, 714/957-0171)

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CIRCLE NO 51

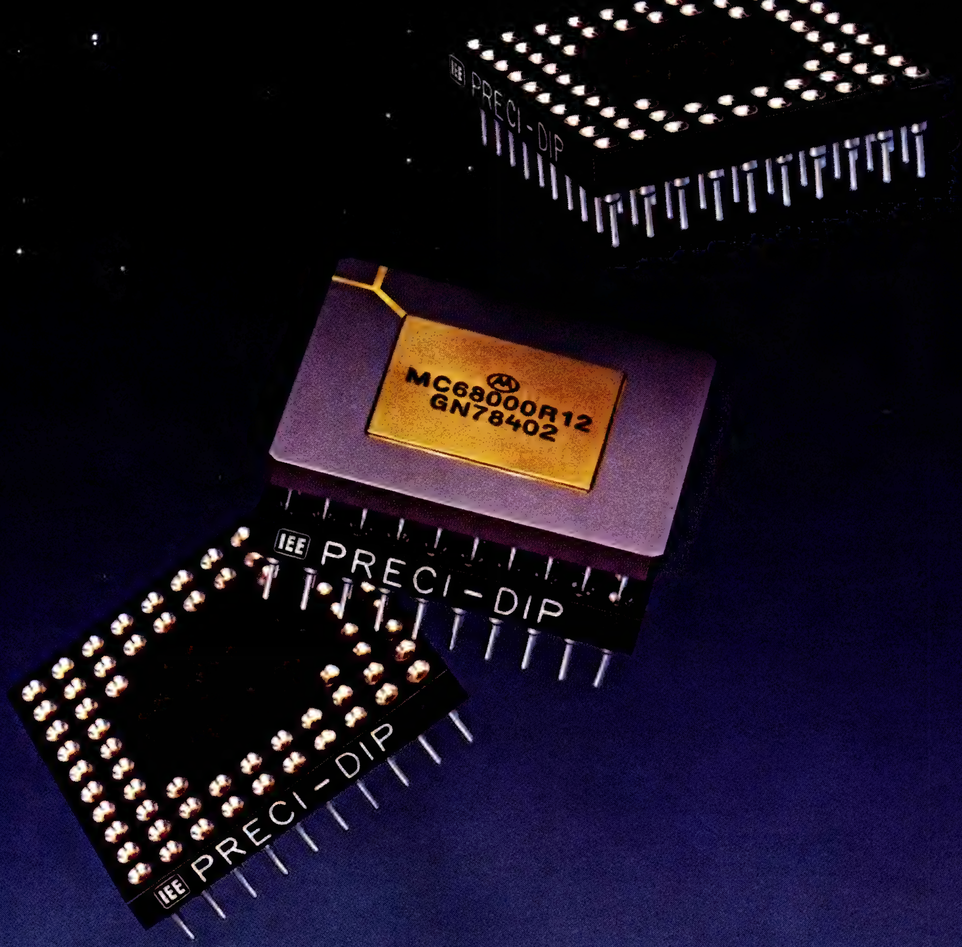
EDN

CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

February 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1	2
3	4	5	6	7	8	9
10	11	12 LINCOLN'S BIRTHDAY	13	14 VALENTINE'S DAY	15	16
17	18 WASHINGTON'S BIRTHDAY	19	20	21	22	23
24	25	26	27	28		

- **3-6 AEA Orlando Financial Conference for Public Companies**
Marriott Hotel, Orlando, FL (Florence Lewis, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **3-8 Power Engineering Society Winter Meeting**
New York Penta Hotel New York, NY (J.G. Derse 1030 Country Club Rd., Bedminster, NJ 07921, 201/725-4388)
- **4-6 Office Automation Conference**
Georgia World Conference Center, Atlanta, GA (American Federation of Information Processing Societies Inc., 703/620-8952 or 703/620-8926)
- **4-7 Mecom '85, Bahrain Communications Exhibition and Conference.**
Bahrain, Saudi Arabia (Kallman Associates, 201/652-7070)
- **5 Basic IC Technology**
Orlando, FL (Pat Fruscello, ICE, 15022 N. 75th St., Scottsdale, AZ 35260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **5-7 Mini/Micro West**
Hilton Exposition Center, Anaheim, CA (Nancy Hogan, Jerry Fossler, Electronic Conventions Management Inc., 213/722-2965-8100 Airport Blvd., LA., CA 90045)
- **5-8 Mexcom '85**
Mexico City, Mexico (Latcom, Inc., 703/685-0600)
- **6 STATUS '85**
Orlando, FL (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **7 SemiConductor Purchasing Strategies**
Orlando, FL (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **9-16 IEEE '85 Aerospace Applications Conference**
Snowmass, CO. Russell A. Gaspari, 6656 W. 87th Place, Los Angeles, CA 90045, 213/648-1325)
- **12-14 CADCON'85**
Pasadena, CA (Jerry Pugh, Morgan-Grampian Expositions Group, 2 Park Ave., NY, NY 10016, 212/340-9780)
- **13-15 Int'l Solid State Circuits Conference**
New York Hilton-New York, NY (Lewis Winner, 301 Almeria Ave., Coral Gables, FL 33134, 305/446-8193)
- **15-17 Rainbow Fest**
Newport Beach, CA (Falsoft, Inc., 502/228-4492)
- **18-19 Microcomputers & Media Exhibit & Show**
Las Vegas, NV (ATE, 815/753-1241)
- **19 Basic IC Technology**
Scottsdale, AZ (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **20 STATUS '85**
Scottsdale, AZ (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **20-22 Info/Central**
Computers & Communication Systems Show & Conference, O'Hare Exposition Center, Rosemont, IL (Info/Central, 203/964-8287 CEG)
- **20-22 Info/Software**
Information Management Exposition & Conference for Software, O'Hare Exposition Center, Rosemont, IL (Info/Software, 203/964-0000 Cahners Exposition Group)
- **20-23 Computer Business Graphics**
Bonaventure InterContinental Hotel, Ft. Lauderdale, FL (Carol Avery-Frost & Sullivan, 212/233-1080)
- **21 Semiconductor Purchasing Strategies**
Scottsdale, AZ (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **21-23 Mac World Exposition**
Brooks Hall. San Francisco, CA (Gene Bignami Mitch, Hall Associates, P.O. Box 860, Westwood, MA 02090, 617/329-7466)
- **23-24 Microcomputer Faire**
Von Braun Civic Center, Huntsville, AL (Willy Albanes P.O. Box, 5440, Huntsville, AL 35814, 205/883-1169)
- **25-28 COMPCON Spring '85**
Cathedral Hill Hotel, SanFrancisco, CA (Harry Hayman P.O. Box 639, Silver Spring, MD 20901. 301/589-8142)
- **25-28 Agri-Mation Conference & Exposition**
Chicago, IL (SME, 313/271-0023)
- **26 Invitational Computer Conference, ICE,**
Marriott Hotel, FT. Lauderdale, FL (Suzanne Hubner, Joyce Cassidy B.J. Johnson and Associates, Inc., 1351 Airway Ave., C-2, Costa Mesa, CA 92625, 714/957-0171)
- **26 Basic IC Technology**
Dallas, TX (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **26 Live Video Conference on Robot Dynamics**
F.O.B. Sky (Dr. R. Kahrmann, 445 Hoes Lane, Piscataway, NJ 08854, 201/981-0060, Ext. 327)
- **26-28 Automated Design & Engineering for Electronics**
Hilton and Towers, Anaheim, CA (Michael Indovina, Cahners Exposition Group, 312/299-9311 Telex: 256-148CEG CGO DSP)
- **26-28 NEPCON West**
Hilton and Towers,Anaheim, CA (Cahners Exposition Group, 312/299-9311 Telex: 256-148 Cahners CEG CGO DSP)
- **27 STATUS'85**
Dallas, TX (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **28 Invitational Computer Conference**
Paris International Hilton, Paris, France (Beatrice Labb, Joyce Cassidy, B.J. Johnson and Associates Inc., 3151 Airway Ave. Costa Mesa, CA 92626, 714/957-0171)



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March 1985

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					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17 ST. PATRICK'S DAY	18	19	20	21	22	23
24 / 31	25	26	27	28	29	30

- **4-7 FOSE'85 & Fose Software '85**
Office Automation Conference & Expo, Convention Center, Washington, DC (National Trade Productions, Jacqueline Vogt, 301/459-8383 or 800/638-8510)
- **4-7 Interface '85**
Georgia World Congress Center, Atlanta, GA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **5 Basic IC Technology**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **5-7 SOUTHCON/85**
High Technology Electronics Exhibition and Convention, Georgia World Congress Center, Atlanta, GA (Nancy Hogan or Jerry Fossler, Electronic Conventions Management Inc., 213/772-2965, 8110 Airport Blvd., LA, CA 90045)
- **5-7 Mini/Micro SOUTHEAST/85**
Computer Conference and Exhibition, Georgia World Congress Center, Atlanta, GA (Nancy Hogan or Jerry Fossler, Electronic Conventions Management Inc., 213/772-2965, 8110 Airport Blvd., LA, CA 90045)
- **6 STATUS '85**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **6-8 AEA Financial Conference for Emerging Growth Companies**
Hyatt Regency Monterey, Monterey, CA (David McKell, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **7 Invitational Computer Conference**
Frankfurt Sheraton, Frankfort, Germany (Beatrice Labbe, B.J. Johnson and Associates Inc., 3151 Airway Ave., C-2, Costa Mesa, CA 92626, 714/957-0171 Telex: 188-747 TAB Irin)
- **7 Semiconductor Purchasing Stragegies**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **7-10 Computer Showcase Expo**
Civic Plaza, Phoenix, AZ (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **7-10 Computer Showcase Expo**
New York Coliseum, New York, NY (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **9-10 AAHTC '85**
Asian American High Technology Convention, Convention Center, San Jose, CA (Regina Lau Asian American Manufacturers Association, 415/325-5499)
- **11-13 Flexible Manufacturing Systems (FMS)**
AMFAC Hotel, Dallas, TX (John McEachran, Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI. 48121, 313/271-1500 Ext. 382)
- **11-14 Nat'l Design Engineering Show & ASME Conference**
McCormick Place, Chicago, IL (American Society of Mechanical Engineers, 203/964-8287)
- **12 Basic IC Technology**
Zurich, Switzerland (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **12-13 Practical Integrated Circuit Fabrication**
Sunnyvale, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **12-14 Semicon/Europa '85**
Zurich, Switzerland (Mary Beth Kern, Semiconductor Equipment & Materials Inst., 625 Ellis St., Suite 212 Mt. View, CA 94043, 415/964-5111)
- **13 STATUS '85**
Zurich, Switzerland (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **19 Invitational Computer Conference**
Hyatt Palo Alto Hotel, Palo Alto, CA (Suzanne Hubner, Joyce Cassidy, B.J. Johnson and Associates Inc., 3151 Airway Ave., C-2, Costa Mesa, CA 92625, 714/957-0171)
- **19 Basic IC Technology**
Los Angeles, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **20 STATUS '85**
Los Angeles, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **20-22 4th Annual Phoenix Conference on Computers & Communications**
Arizona State University, Phoenix, AZ (Doug Powell Motorola Inc., P.O. Box 2953, Phoenix, AZ 85062, 602/244-3965)
- **20-22 IMTC '85 Instrumentation/MTC**
Hyatt Regency Hotel, Tampa, FL (Dr. J. Robert Ashley Sperry Corp., MS 214, P.O. Box 4648 Clearwater, FL 33518, 813/577-1900 Ext. 2228)
- **21 Semiconductor Purchasing Strategies**
Los Angeles, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **21-22 AIRCON 2**
Int'l Conference on Artifical Intelligence for Robotics, Stouffers Concourse, Crystal City, Arlington, VA (Dr. Diener, IIT Research Institute, 312/567-4376)
- **21-24 Comdex/Winter**
Anaheim Convention Center, Anaheim, CA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **24-29 AEA/UCLA Senior Management Program**
University of California at Los Angeles, Los Angeles, CA (Diane McIntyre, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **25-28 IEEE INFOCOM '85**
Hyatt Regency Crystal City, Washington, DC (Ms. Celia Desmond, Bell Canada, HQ Engineering, Room 1855, 160 Elgin St., Ottawa, Ontario, KIG3J4, Canada, 613/239-4510)
- **25-28 VISION '85 Conference & Expo**
Detroit, MI (Nancy Berg or Susan Buhr, SME Expositions, 313/271-1500, TWX 810-221-1232, SME DR BN)
- **25-28 Megatech**
Infomart, Dallas, TX (Megatech, 800/323-5155 or 312/299-3131)
- **25-29 IEEE Int'l Conference on Robotics & Automation**
Marriott's Pavilion Hotel, St. Louis, MO (Dr.K.S. Fu, Dept of Elect. Engrg. Purdue Univ., West Lafayette, IN 47907, 317/494-3433)
- **26-28 Comdex/Japan**
Harumi Exhibition Center, Tokyo, Japan (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **26-28 14th Convention of Electrical & Electronics Engineers**
Tel Aviv Fair Grounds, Tel Aviv, Israel (Dr. David Biran, 30 Trumpeldor St., Ramat, Hasharon, 47265 Israel Tel: 03/471542)
- **31-April 3 SOFTCON '85**
Georgia World Congress Center, Atlanta, GA (Gerry Milden, Northest Expositions Inc., 617/739-2000)
- **31-April 3 SOUTHEASTCON '85**
Mission Valley Inn, Raleigh, NC (G.E. Shuford Jr., P.O. Box 1551, Raleigh, NC 27602, 919/836-99)

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CIRCLE NO 53

EDN

CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

April 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1	2	3	4	5	6
7 EASTER	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30				

- **2 Invitational Computer Conference**
Sheraton-Tara Hotel, Nashua, NH (Suzanne Hubner, Joyce Cassidy, B.J. Johnson and Associates Inc., 1351 Airway Ave., C-2, Costa Mesa, CA 92625, 714/957-0171)
- **9-12 12th Int'l Reliability, Availability, Maintainability Conference**
For The Electric Power Industry (Inter-RAM) Hilton Hotel, Baltimore, MD (Mrs. Melissa Bradley, Baltimore Gas & Electric Co., FT. Smallwood Rd. Complex, P.O. Box 1475, Baltimore, MD 21203)
- **10-11 NEPCON SOUTHWEST '85**
Dallas Infomart (Janet Schafer, Cahners Exposition Group, 312/299-9311, Telex: 256-148 CEG CGO DSP)
- **14-18 Computer Graphics '85 Conference & Expo**
Dallas Convention Center (National Computer Graphics Association, 703/698-9600)
- **14-18 Chi '85 Human Factors in Computing Systems**
Hyatt Regency, San Francisco, CA (Lorraine Borman, Vogelback Computing Center N.W. Univ., 2129 Sheridan Rd., Evanston, IL 60201)
- **14-18 AEA International Financial Conference**
Loews Monte-Carlo Hotel, Monte Carlo, Monaco (Florence Lewis, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **14-19 AEA/Santa Clara Management Development Program**
Pajaro Dunes Conference Center, Watsonville, CA (Diane McIntyre, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **16 Basic IC Technology**
Newport Beach, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **16-18 ATE Silicon Valley '85**
San Mateo County Exposition Center, CA (Jerry L. Pugh, ATE Exhibit Sales, 212/340-9780, 2 Park Ave., NY, NY 10016 Morgan-Grampian Expo. Group)
- **16-18 IEEE Joint Rail Road Conference**
Roosevelt Hotel, New York, NY (A.P. Engel Gibbs and Hill Inc., 11 Penn Plaza NY, NY 10001, 212/760-4707)
- **17 Semiconductor Purchasing Strategies**
Newport Beach, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780 Telex: 165-755 ICE, Scot)
- **17-24 Hanover Fair '85**
Hanover, Germany (Delia Associates, 800/526-5978, 201/534-9044 Telex: 833493)
- **21-27 Semiconductor Int'l. China '85**
Shanghai Exhibition Centre, The People's Republic of China (John R. McCarus, Cahners Exposition Group, 7315 Wisconsin Ave., P.O. Box 70007, Washington, DC 20088, 301/657-3090 Telex: 908727)
- **22-24 American Power Conference**
Palmer House, Chicago, IL (Ralph E. Armington, Illinois Institute of Technology, Chicago, IL 60616, Bldg. E1-Room 218, 312/567-3406)
- **22-25 Digital Processing of Signals in Communications**
Univ. of Loughborough, England (Conference Dept., IERE 99 Gower St., London WCIE 6AZ, England, Tel: 01/388-3071)
- **23-25 ELECTRO/85**
High Technology Electronics Exhibition & Convention, N.Y. Coliseum & Sheraton Centre, New York, NY (Electronic Conventions Management Inc., Nancy Hogan or Jerry Fossler, 8100 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **23-25 MINI/MICRO NORTHEAST/85**
Computer Conference and Exhibition, New Yew Coliseum (Nancy Hogan or Jerry Fossler, Electronics Convention Management Inc., 8100 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **23-25 Federal DP Expo**
Washington, DC Convention Center, Washington, DC (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **23-25 NEPCON SOUTHEAST '85**
Orange County Convention Center, Orlando, FL (Cahners Exposition Group, 312/299-9311, Telex: 256148 CEG CGO DSP)
- **23-25 ELECTROTEST '85**
Exhibition of Testing Equipment, Methods & Technology for Electronics Design and Manufacturing, Orange County Convention Center, Orlando, FL (Cahners Exposition Group, 312/299-9311, Telex: 256148, CEG CGO DSP, Carol Fojtik, Cahner's Plaza, 1350 E. Touhy Ave., P.O. Box 5060, Des Plaines, IL 60018)
- **25-28 Computer Showcase Expo**
San Diego Convention Center, San Diego, CA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **26-28 Computer Showcase Expo**
A.J. Cervantes, St. Louis, MO (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **28-May 1 AEA Human Resources Symposium**
Americana Canyon Hotel, Palm Springs, CA (Debi Nason, American Electronics Association, 2670 Hanover Street, Palo Alto, CA 94303, 415/847-9300)
- **29-May 2 Intermag**
Radisson St. Paul, St. Paul, MN (E.J. Torok Sperry Univac, P.O. Box 3525 MS U2 P26, St. Paul, MN 55165, 612/456-2432)
- **30-May 2 Electronic Distribution Show & Conference**
Hyatt Regency Hotel, Chicago, IL (Electronic Industry Show Corp., 312/648-1140)
- **30-May 2 Electronic Production Efficiency Expo. '85**
NEC, Birmingham, England (Network Events LTD., (0280) 815226, Telex: 83111)
- **30-May 2 All Electronics/ECIF Show**
Olympia, London (British Trade Development, 212/593-2258, Tom Webb)

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UNITED TECHNOLOGIES
HAMILTON STANDARD
CONTROLS

CIRCLE NO 54

EDN CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

May 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
			1	2	3	4
5	6	7	8	9	10	11
12 MOTHER'S DAY	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27 MEMORIAL DAY	28	29	30	31	

- **2-4 The Byte Computer Show**
Anaheim Convention Center, Anaheim, CA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **6-9 COMDEX/SPRING '85**
Georgia World Congress Center, Atlanta, GA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **6-9 IEEE 1985 Int'l. Radar Conference**
Marriott Crystal Gateway, Arlington, VA (Robert T. Hill, 2802 Birdseye Lane, Bowie, MD 20715, 301/262-8792)
- **7-8 Practical Integrated Circuit Fabrication**
Minneapolis, MN (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **7-10 Power Industry Computer Applications PICA Conference '85**
Hyatt on Union St., San Francisco, CA (George Gross, Pacific Gas & Electric Co., 77 Beale St., Rm. 2459, San Francisco, CA 94106, 415/781-4211)
- **13-16 Industrial & Commercial Power Systems Conference 1 & CPS**
Denver Hilton Hotel, Denver, CO (Michael J. Foley, Public Service Co., of Colorado, 5929 E. 38th Ave., Denver, CO 80207, 303/571-6592)
- **13-16 Particle Accelerator Conference**
Hotel Vancouver, Vancouver, BC Canada (M.K. Craddock, Triumf University of BC, Vancouver BC, V6T, £A3, Canada, 604/228-4711)
- **13-17 5th Int'l Conference on Distributed Computing**
The Fairmont Hotel, Denver, CO (Dr. Earl Swartzlander TRW Defense Systems, One Space Park, Redondo Beach, CA 90278, 213/535-4177)
- **14-16 Test and Measurement World Show**
San Jose Convention Center, San Jose, CA (Meg Bowen (TMEW), 215 Brighton Ave., Boston, MA 02134, 617/254-1445)
- **15-17 1985 Carnahan Conference on Security Technology**
Carnahan House, University of Kentucky, Lexington, KY (Cheryl Banks, Office of Engineering Education, University of Kentucky, Lexington, KY 40506-0043, 606/257-3974)
- **16-19 Computer Showcase Expo**
Convention Center, Washington, DC (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **21-23 National Aerospace & Electronics Conference '85**
Dayton Convention Center, Dayton, OH (Naecon, 110 E. Monument Ave., Dayton, OH 45402, 513/223-6266)
- **21-23 SENSOR '85**
Schwarz Wald Halle & Nancy Halle The Karlsruhe Exhibition Centre, W. Germany (Network Events LTD (0280) 815226; Telex: 83111)
- **21-23 SEMICON/WEST '85**
San Mateo, CA (Susan Castillo, Semiconductor Equipment & Materials Inst., 625 Ellis St., Suite 212, Mt. View, CA 94043, 415/964-5111)
- **22-24 AEA Northeast Financial Conference for Emerging Growth Companies**
Copley Square Marriott, Boston, MA (David McKell, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **22-24 The Byte Computer Show**
Bayside Expo, Boston, MA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **24-26 Int'l Conference on Foundations of Data Organization**
Kyoto Univ. Sakyo, Kyoto, Japan (Yahiko Kambayashi, Kyushu Univ., Fukuoka 812, Japan, Tel: 75-751-2111, Ext. 5382)
- **23-26 IEEE Int'l Conference on Communications**
Palmer House, Chicago, IL (J.D. Johanneson, Midwest *College of Engineering*, P.O. Box 1147 ICC '85, Lombard, IL 60148, 312/627-6854)
- **24-26 Design Automation Conference**
Las Vegas (Harry Hayman, P.O. Box 639, Silver Spring, MD 20901, 301/589-8142, TWX: 7108250437, IEEE Compso)
- **24-28 Machine Processing of Remotely Sensed Data**
Stewart Center, Purdue University, W. Lafayette, IN (Douglas B. Morrison, Purdue Univ./Lars, 1291 Cumberland Ave., W. Lafayette, IN 47906, 317/494-6305)
- **24-28 IEEE Power Electronics Specialists Conference**
University Paul Sabatier, Toulouse, France (Dr. Antoine Capel, Thomson CSF, BP1009 Ave., Eisenhower 31037 Toulouse, Cedex/France, Tel: (61) 41-11-40)
- **24-29 Int'l Conference on Properties & Applications of Dielectric Materials**
Shaanxi Guesthouse Xian, China (Pre) (Kwan C. Kao, Dept. of Elect. Engineering., University of Manitoba, Winnipeg, Manitoba R3T 2N2, Canada, 204/474-9649)
- **28-30 15th Int'l Symposium on Multiple Valued Logic**
Queens University, Kingston, Ontario, Canada (Prof. H.T. Mouftah, Dept. of Electrical Engineering, Queens University, Kingston, Ontario K7L3N6, Canada, 613/547-3114)
- **29-31 39th Annual Frequency Control Symposium**
Marriott Hotel, Philadelphia, PA (Dr. John R. Vig, Electronics Technology & Device Lab., Delet-MQ Fort Monmouth, NJ 07703)

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CIRCLE NO 55

EDN

CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

June 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16 FATHER'S DAY	17	18	19	20	21	22
23 / 30	24	25	26	27	28	29

- **3-5 Eastern Design Engineering Show & ASME Conference**
Bayside Exposition Center, Boston, MA (American Society of Mechanical Engineers, 203/964-8287)
- **3-6 National Computer Conference (NCC '85**
New York, NY (AFIPS, 1899 Preston White Dr., Reston, VA 22091, 703/620-8900)
- **4-6 7th Symposium on Computer Arithmetic**
University of Illinois, Urbana, IL (Prof. D. Gajski, Dept. of Computer Science, University of Illinois, Urbana, IL 61801, 217/333-2822)
- **4-6 Int'l Microwave Symposium & Workshops, Stouffer's River Front Towers Cervantes**
Convention Center, St. Louis, MO (Dr. Fred J. Rosenbaum, Central Microwave Co., 12180 Pritchard Farm Rd., St. Louis, MO 63043, 314/291-5270)
- **4-6 COMPETA '85**
Computer & Peripherals Equip. Trade Association Show, Kensington Exhibition Centre, London (Network Events LTD., Buckingham 0280 815226, Telex: 83111)
- **5-7 1985 Int'l Symposium on Circuits & Systems**
Kyoto Hotel, Kyoto, Japan (Toshio Fujisawa, Dept. of Info. & Computer Sciences, Osaka University, Toyonaka 560, Japan, 06-844-1151 Ext. 4820)
- **6-9 Computer Showcase Expo**
Seattle Center, Seattle, WA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **6-9 Computer Showcase Expo**
Dallas Market Center, Dallas, TX (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **10-13 ATE EAST**
Sheraton Boston Hotel & Exhibit Hall, Prudential Center, Boston, MA (Jerry Pugh, Morgan Grampian Expo. Group, 2 Park Ave., New York, NY 10016, 212/340-9780)
- **11-13 6th Biennial University/Micro Electronics Symposium**
Electrical Engineering Dept., Auburn University (Richard C. Jaeger, 200 Broun Hall, Auburn University, Auburn, AL 36849, 205/826-4330)
- **12-13 Ohmcon High Tech Electronics Show & Convention**
Cobo Hall, Detroit, MI (Robert Barba Ohmcon, P.O. Box 699, Utica, MI 48087, 313/781-4551)
- **12-14 INFO/WEST**
Anaheim, CA (Cahners Exposition Group, 312/299-9311, Telex: 256-148, CEG CGO DSP)
- **12-14 PC World Exposition**
Convention & Performing Arts Center, San Diego, CA (Gene Bignami, Mitch Hall Associates, P.O. Box 860,Westwood, MA 02090, 617/329-7466)
- **13-16 Int'l Computer Show Cologne**
Cologne, W. Germany (U.S. Embassy, Bonn-John Lumborg or Koln Messe, 228-339-2047, Norbert Wysokowski or Frank Frielingsdorf, 221-821-2263/821 2489)
- **13-16 Computer Showcase Expo**
Civic Center, Philadelphia, PA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **16-21 1985 North American Radio Science Meeting & IEEE Int'l. APS Symposium**
University of British Columbia, Vancouver BC, Canada (Dr. E.V. Jull, Dept of E.E., University of BC Vancouver, BC V6T IW5, Canada, 604/228-3282)
- **17-18 Model Error Concepts & Compensation**
Boston, MA (R.E. Skelton, 331 Grissom Aero & Astro Purdue Univ., W. Lafayette, IN 47907, 317/494-5132)
- **17-19 PC Expo/New York**
New York Coliseum, NY (Ralph Ianuzzi Jr., PC Expo., 333 Sylvan Cliffs, NJ 07632, 201/569-8542)
- **18-20 Syntopican**
Washington, DC (Charlie Asmus, Prestige Expositions Inc., P.O. Box 424, Hohokus, NJ 07423, 201/444-0505)
- **18-20 NEPCON EAST**
Bayside Exhibition Center, Boston, MA (Cahners Exhibition Group, Dept 'M', P.O. Box 3833, Stamford, CT 06905, 203/964-0000)
- **19-21 1985 American Control Conference**
Boston Marriott Copley Place, Boston, MA (Prof. Yaakov, Bar shalom, Code 62X5 NPS Monterey, CA 93942, 408/646-2233)
- **19-21 NASECODE IV**
The Fourth Int'l Conference on the Numerical Analysis of Semiconductor Devices & Integrated Circuits, Trinity College, Dublin, Ireland (Prof. John Miller NCNAG., 39 Trinity College, Dublin 2, Ireland, Tel: 01 772941, Ext. 1485)
- **20-13 Computer Showcase Expo**
MECCA, Milwaukee, WI (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)

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Only Nicolet makes it easy and inexpensive to enhance *performance*—not just add channels—any time you need it. And the NPC-800 Series gives you *five* instruments to choose from, and more options than anyone else in the industry: Waveform Recorder, Performance Analysis, CT/SA, Computer/IEEE-488 Controller, Printer Software, Non-Volatile Memory, Dot Matrix Printer, and Second Disk Drive.

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When you really think about it, the only way to be sure is to let the best logic analyzers prove what they can do—for *you*. When it comes to capability, versatility, and performance, there's really only one choice. For a Logic Analyzer Comparison Chart, call: **(800) NICOLET** or **(415) 490-8300** (inside CA). Nicolet Paratronics Corporation, 201 Fourier Ave., Fremont, CA 94539.

Think of us!

Nicolet

The World's Three Great Logic Analyzers.

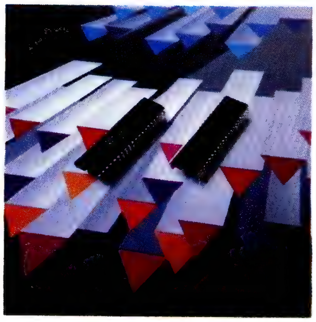
CIRCLE NO. 56

THE MASTER

FROM NEC, YOUR SINGLE-SOURCE SEMI SUPPLIER

The world's third largest semiconductor supplier has more ways to meet your needs. We offer one of the most diversified product lines in the industry. Uncompromising quality that gives you an extra margin of system reliability. And original technology that puts you on the inside track to tomorrow's markets.

V-Series Microprocessors



The V-Series is more than a new family of CMOS microprocessors. It's a strategy for success with your next generation of products. A strategy based on immediate performance gains with minimum engineering effort.

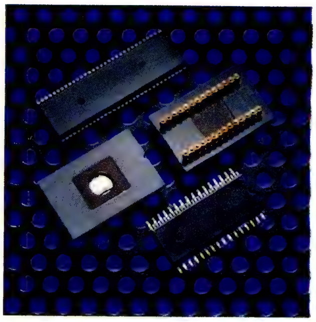
- ☐ 8- to 16-bit microprocessor family
- ☐ 32-bit will be available in future
- ☐ CMOS technology
- ☐ Advanced architecture for faster execution
- ☐ 101 instructions
- ☐ 8088/86 pin-replaceable
- ☐ 85% less power than NMOS products
- ☐ Greater power reductions in standby mode
- ☐ CMOS peripheral family
- ☐ Advanced development tools

Memory Products

NEC offers the world's broadest line of memory products, every one produced to exceptionally high quality standards. 100% burn-in and 200% electrical screening are among the ways we give you the best of memories.

- ☐ DRAMs: seven configurations in 256K
- ☐ SRAMs: broad choice of technologies
- ☐ Masked ROMs: high density in both CMOS and NMOS
- ☐ EPROMs: both UV and OTP
- ☐ Bipolar PROMs: shorted junction technology
- ☐ ECL RAMs: the fastest on the market

7800 Series Single-Chip Microcontrollers



The ultimate in design flexibility, the 7800 Series includes both CMOS and NMOS variations, A/D or comparator ports, full duplex USARTs, and up to 44 general purpose I/O lines. All based on a high-performance 8/16-bit architecture.

- ☐ Supported by sophisticated development tools
- ☐ Expandable to 64K x 8 RAM
- ☐ ROM-less, 4K x 8, or 8K x 8 ROM options
- ☐ Up to 256 byte RAM
- ☐ With 8K x 8 EPROM and piggyback versions available

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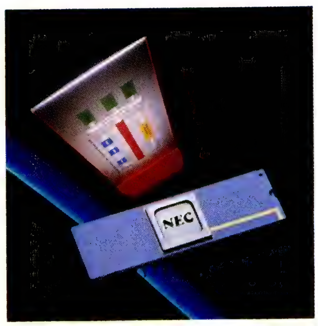
LIST

Linear

NEC offers a broad line of linear integrated circuits to help solve your design problems.

- ☐ Data Conversion
  - A/D 8-bit, 10-bit, 12-bit (CMOS)
    - Flash, SAR, Integrating
  - D/A 8-bit, 12-bit
- ☐ Consumer Circuits
  - Digital tuning circuits
  - Power amp ICs
  - Hybrid amps
  - Monolithic microwave ICs
  - I/R remote control ICs
- ☐ Standard Linear
  - Op amps
  - Comparators
  - Timers
  - Voltage regulators
- ☐ Opto products
  - Photo interruptors
  - Opto isolators

Complex Peripherals



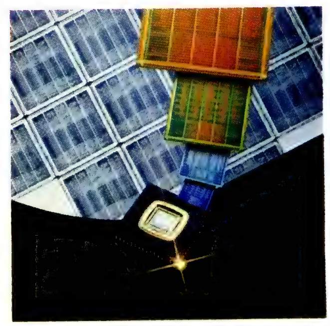
NEC is a leading supplier of high-quality, multi-functional peripheral and digital signal processing chips. Our devices are used in the leading personal computer systems, high performance color terminals, HPIB compatible instruments, speech, high performance modems and advanced video image processing systems. These devices reduce system design time and cost while increasing reliability.

- ☐ Multi-protocol serial controllers
- ☐ Floppy and hard disk controllers
- ☐ Graphic display controllers
- ☐ Intelligent GPIB interface controllers

Digital signal processors

- ☐ Image pipelined processor
- ☐ Speech recognition package
- ☐ Signal processing interface
- ☐ Voice synthesis LSIs

Gate Arrays



We are making a major commitment to provide full customer satisfaction in semi-custom ICs. User-friendly design tools and design centers across the country are part of the package.

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  - CMOS: 12 densities
  - TTL: 6 densities
  - ECL: 5 densities
- ☐ World leader in high-density arrays
  - 11,000-gate 2-micron CMOS
- ☐ Flexible, user-friendly CAD tools
- ☐ High quality and reliability

To master your design problems, give us a call about any item on our master list. Just specify the product area that interests you. And we'll respond with an information package.

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In California: 1-800-441-2345, ext 188.

CIRCLE NO 57

NEC

NEC Electronics Inc.

EDN CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

July 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1	2	3	4 INDEPENDENCE DAY	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

- **7-12 AEA Manufacturing Management Program**
University of California at Santa Cruz, Santa Cruz, CA (Debi Nason, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **9-11 CONTROL '85**
Univesity of Cambridge, United Kingdom (IEE Conference Dept., Savoy Place, London WC2R-OBL, UK, Tel: 01-240 1871, Ext. 222, Telex: 261176, IEE LDN G)
- **14-19 Power Engineering Society Summer Meeting**
Hotel Vancouver Hyatt, Vancouver, Canada (D.G. McFarlane, BC Hydro & Power Authority, Box 12121, 555 W. Hastings St., Vancouver, BC V6B 4T6, Canada, 604/663-2310)
- **14-19 AEA/Santa Clara Management Development Program**
University of Santa Clara, Santa Clara, CA (Diane McItyre, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **15-18 NCC '85 National Computer Conference**
McCormick Place, Chicago, IL (Helen Mugnier AFIPS, 703/620-8926)
- **15-18 AEA Financial Conference for Emerging Growth Companies**
Hyatt Regency Monterey, Monterey, CA (David McKell, American Electronics Association, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **22-25 IFAC Symposium on Planning & Operation**
Rio Palace Hotel, Rio De Janeiro, Brazil (Dr. Hugh Rudnick, Universidad-Catolica-Dechile Casilla 114-D, Santiage, De Chile, Tel: 513553)
- **22-26 SIGGRAPH**
San Francisco, CA (Cynthia Stark, Association for Computing Machinery, 312/664-6610)
- **22-26 '85 Int'l Symposium on Microwave Technology**
Sao Paulo, Brazil (Waldyr-Lucato, IEEE Sao Paulo Section RVA CEL. Xavier De Toledo, 23 01408, Sao Paulo, SP, Brazil, Tel: 011/239-6239, Telex: 1122582 ET BR)
- **31-Aug. 2 Third IFAC Symposium on Computer-Aided Design in Control & Engineering Systems**
The Technical University, Lyngby, Denmark (Danish Automation Society Bld. 229, Tech. University of Denmark, KE-2800)

TAKE A CLOSER LOOK AT MULTIFILAR® MAGNET WIRE.

Whenever two or more magnet wires travel together, MULTIFILAR magnet wire is worth a closer look. This parallel-bonded, color-coded magnet wire offers many benefits for both small and large users.

Engineers should specify it when they're concerned with space, weight and reliability. Where consistent capacitance and impedance characteristics are needed, MULTIFILAR magnet wire outperforms windings where two separate magnet wires are used.

Production users benefit from increased layer winding speeds, reduced labor and handling. Color-coding assists in conductor identification and reduces termination errors.

MULTIFILAR magnet wires are custom produced by MWS. We guarantee flat, parallel construction in an array of sizes 16 AWG and finer, with up to 20 conductors in some sizes.

Both round and flat constructions are available. Color-coded conductors are available in most insulations with up to 10 different colors in some sizes. Conductor separation is also guaranteed with certain bonding mediums.

For an even closer look, send for a free sample, specifications and ordering information. Production minimums are as low as 500 feet.

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Wire Industries

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In California 1 800 992-8553, In Los Angeles Area (818) 991-8553.

Multifilar® is a registered trademark of MWS Wire Industries.

CIRCLE NO 58

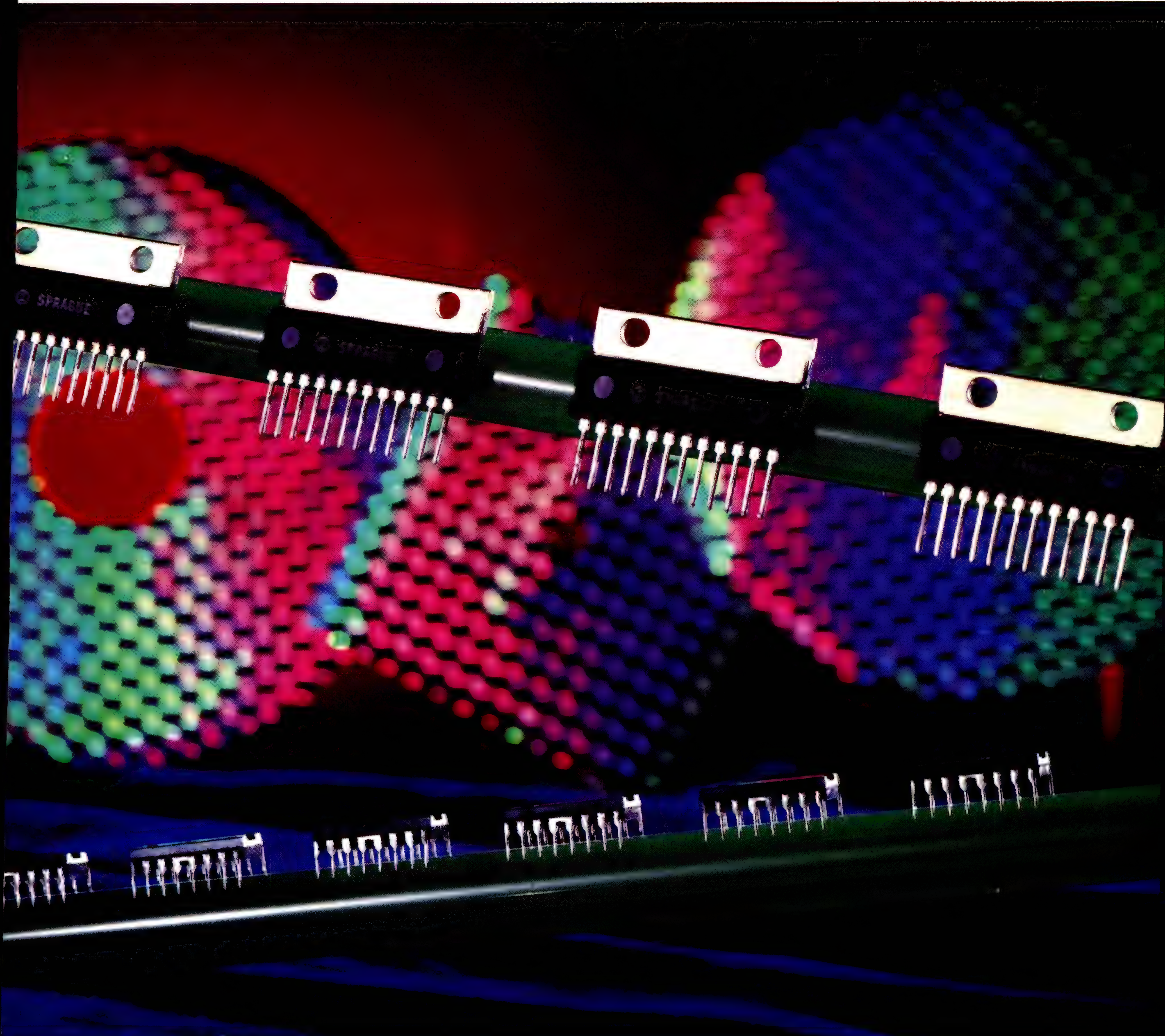
EDN CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

August 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

- **4-7 AEA Monterey Financial Conference**
Hyatt Regency Monterey, Monterey, CA (Florence Lewis, AEA, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **4-16 AEA/Stanford Executive Institute**
Stanford University, Stanford, CA (Diane McIntyre, AEA, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **18-23 Inter Society Energy Conversion Engineering Conference (IECEC)**
Fountainbleu Hilton, Miami Beach, FL (Floyd A. Wyczalek, Engineering Staff Div. G.M. Technical Center GM Corp., Warren, MI 48090, 313/575-1153)
- **19-20 Midwest Symposium on Circuits & Systems**
The Galt House Hotel, Louisville, KY (Dr. P. Aronhime, University of Louisville, Louisville, KY 40292, 502/588-6289)
- **20 Basic IC Technology**
Sunnyvale, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **20-22 1985 IEEE Int'l. Symposium on Electro Magnetic Compatibility**
Colonial Hilton Inn, Wakefield, MA (Dr. Chester L. Smith, The Mitre Corp., P.O. Box 208, Bedford, MA 01730, 617/271-7086)
- **21 Mid-Term STATUS '85**
Sunnyvale, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **21-23 Mac World Exposition**
Bayside Exposition Center, Boston, MA. (Gene Bignami, Mitch Hall Associates, P.O. Box 860, Westwood, MA 02090, 617/329-7466)
- **22 Semiconductor Purchasing Strageties**
Sunnyvale, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **26-30 Int'l. Conference on Magnetism ICM '85**
San Francisco, CA (J.F. Dillon Jr., AT &T Bell Labs ID-328, Murray Hill, NJ 07974, 201/582-3589)
- **26-31 7th Int'l Symposium on Computer Hardware Description & Languages**
Tokyo, Japan (Dr. Mario Barbacci, Carnegie Mellon University, Pittsburgh, PA 15213, 412/578-2578, Dept. of Computer Science)
- **27 Basic IC Technology**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **27-30 8th Int'l. Conference on Software Engineering (ICSE)**
Imperial College, South Kensington, England (8th ICSE, P.O. Box 639, Silver Spring, MD 20901, 301/589-8142, TWX: 7108250437, IEEE Compso)
- **28 Mid-Term STATUS '85**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **29 Semiconductor Purchasing Strategies**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)

COMMANDING.



4SS-3133R1

SPRAGUE ICs EXCEL AS D-C MOTOR DRIVERS.

Sprague's new UDN-2952B and UDN-2952W full-bridge motor drivers are designed for 2-phase bipolar control of stepper motors, brushless d-c motors, and some servo applications. Continuous output currents to 2 A at 40 V are allowed, and peak start-up currents as high as 3.5 A. For high-power requirements, the UDN-2952W in a 12-pin SIP power tab package is suggested. For lower power applications, the UDN-2952B in a 16-pin DIP is supplied. Both are compatible with standard logic families. Volume prices (50k) for the DIP version is less than $2, and the SIP version just over $2. Write for Engineering Bulletin 29319 to Technical Literature Service, Sprague Electric Co., a Penn Central unit, **491** Marshall Street, North Adams, Mass. 01247. For applications assistance, call Mark Heisig at 617/853-5000.

SPRAGUE
THE MARK OF RELIABILITY

CIRCLE NO 59

EDN

CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

September 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
1	2 LABOR DAY	3	4	5	6	7
8	9	10	11	12	13	14
15	16 JEWISH NEW YEAR	17	18	19	20	21
22	23	24	25 YOM KIPPUR	26	27	28
29	30					

- **4 Basic IC Technology**
Minneapolis, MN (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **4-6 5th Int'l Symposium on Electrets**
Koenigsaal Castle, Heidelberg, FRG (Dr. Gerhard, M. Sessler, Tech. Univ. of Darmstadt, Merck Strasse 25 D-6100, Darmstadt, FRG. Tel: 49-6151/16-2869)
- **5 Mid-Term STATUS '85**
Minneapolis, MN (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **5-7 The Byte Computer Show**
Convention Center, Dallas, TX (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **6 Semiconductor Purchasing Strategies**
Minneapolis, MN (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **9-11 Electronics & Aerospace Systems EASCON '85 Conference**
Shoreham Hotel, Washington, DC (Dr. Jack W. Hugus, General Elect. Co., Suite 900, 777 14th St., N.W. Washington, DC 20005, 202/637-4243)
- **9-12 Compint '85 Int'l Computer Conference & Exhibition**
Montreal Convention & Exhibition Center, Montreal, Quebec, Canada (Stephen G. Leahey, (Compint' 85) P.O. Box 577, Desjardins Postal Station, Montreal, Que. H5B 1B7, Canada, 514/870-2969)
- **10-12 CADCON**
Boston, MA (Morgan Grampian Expositions Group, 2 Park Ave., NY, NY 10016, 213/340-9780)
- **10-12 MIDCON/85**
O'Hare Exposition Center, Rosemont, IL (Jerry Fossler, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **10-12 MINI-MICRO MIDWEST/85 Computer Conference & Exhibition**
O'Hare Expo. Center, Rosemont, IL (Jerry Fossler, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **10-12 Industrial Productivity Conference & Exposition**
The Grand Center, Grand Rapids, MI (SME, One SME Drive, P.O. Box 930, Dearborn, MI)
- **11-12 Practical Integrated Circuit Fabrication**
Sunnyvale, CA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **11-13 PC World Exposition**
The Metro Toronto Convention Center, Toronto, Canada (Gene Bignami, Mitch Hall Associates, P.O. Box 860, Westwood, MA 02090, 617/329-7466)
- **17-19 Software/Expo**
InFomart, Dallas, TX (Marlan D. Stredwick, Professional Exposition Management Co., 214/655-6298)
- **18 Basic IC Technology**
Dallas, TX (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **18-20 SEMICON/EAST**
Boston, MA (Mary Beth Kern, Semiconductor & Equipment Materials Institute, 625 Ellis St., Suite 212, Mt. View, CA 94043, 415/964-5111)
- **19 Semiconductor Purchasing Strategies**
Dallas, TX (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **19-21 The Byte Computer Show**
New York Coliseum, New York, NY (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **19-22 Computer Showcase Expo**
Convention Center, Kansas City, MO (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **23-25 SPACE TECH '85**
Disneyland Hotel, Anaheim, CA (Society of Manufacturing Engineers, 313/271-1500)
- **27-29 The Byte Computer Show**
Brooks Hall, San Francisco, CA (The Interface Group, 300 First Ave., Needham, MA 02194, 617-449-6600)
- **27-29 Computer Showcase Expo**
Miami Beach Convention Center, Miami, FL (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **28-OCT. 4 Electrical Electronic Insulation Conference**
Sheraton Boston, Boston, MA (Dr. Harry Sheppard, Power Transformer Dept., Westinghouse Corp., 469 Sharpsville Rd., Sharon, PA 16146, 412/983-4335)
- **30-Oct. 2 IEEE Holm Conference on Electrical Contacts**
Palmer House, Chicago, IL (Sam Vaughn IEEE HQ. 345 E. 47th St., New York, NY 10017, 212/705-7405)

WE JUST GAVE THE IBM®-PC ANOTHER HAT.

Ziatech's Series 8800 is a complete family of IBM-compatible, industrial-strength board-level computers. These STD-8088 computers put high performance microcomputer power to work in factories and laboratories.

Works to your requirements

The Series 8800 include a wide variety of STD-8088 memory, processor and I/O boards that let you develop application solutions quickly and easily. More than 140 other STD manufacturers make complementary boards, further increasing your design options. The Series 8800 also includes our Prototype Development System. With this system you can write and debug your software at a fraction of the cost of other development systems.

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CIRCLE NO 60

EDN

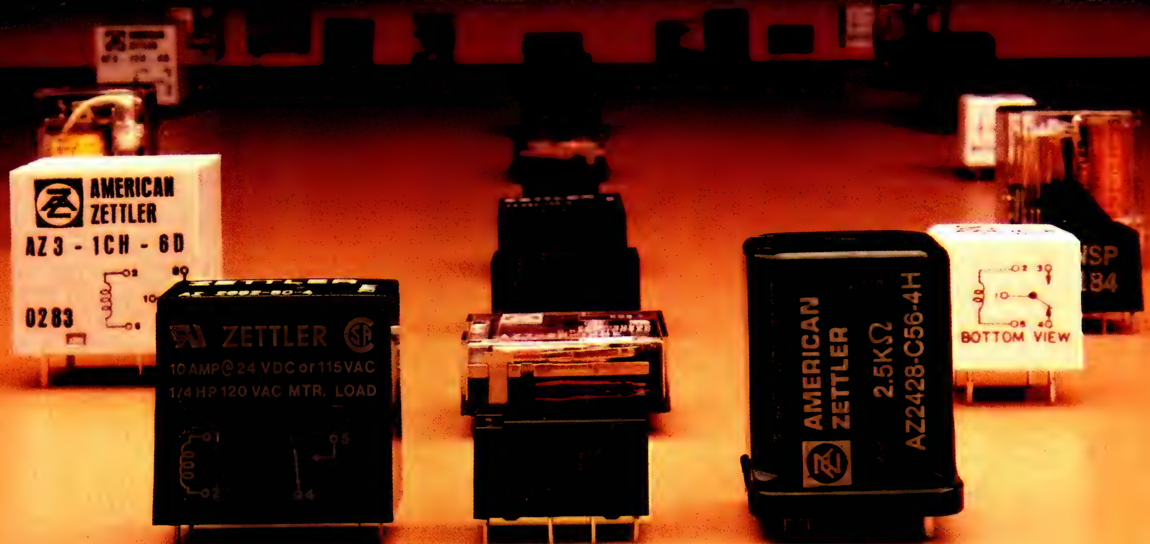
CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

October 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
		1	2	3	4	5
6	7	8	9	10	11	12
13	14 COLUMBUS DAY	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30	31 HALLOWEEN		

- **1-3 1985 Int'l. Test Conference (Cherry Hill '85)**
Franklin Plaza Hotel, Philadelphia, PA (Harry Hayman, P.O. Box 639, Silver Spring, MD 20901, 301/589-8142, TWX 7108250437 IEEE Compso)
- **6-11 Industry Applications Society Annual Meeting**
Royal York Hotel, Toronto, Ontario, Canada (Ajit Bapat Federal Pioneer Corp., Bramalea, Ontario L6T 1E6, Canada, 414/459-8805)
- **7-9 Int'l. Geo Science & Remote Sensing Symposium (IGARRSS '85)**
University of Massachusetts, Amherst, MA (Prof. Robert McIntosh, Engineering Bldg., East Elect. and Computer Engineering, Room 16, University of Mass., Amherst, MA 01003, 413/545-2591)
- **7-9 Electrical & Electronics Conference & Exposition**
Metro Toronto Convention Center, Toronto, Ontario, Canada (IEEE Canadian Region Office, 7061 Yonge St., Thornhill, Ontario, Canada, L3T 2A6, 416/881-1930)
- **8-10 MELECON '85 Third Mediterranean Electro Technical Conference**
Madrid, Spain (Prof. D.A. Luque, ETSI Telecommunication, Ciudad Universitaria Madrid 3, Spain, 314/449-5700)
- **8-10 Internepcon**
International Electronic Packaging & Production Equipment Conference & Exhibition, Metropole Exhibition Centre & Brighton Centre, Brighton, England (Tom Webb, British Trade Development Office, 212/593-2258)
- **8-10 NEPCON/NORTHWEST**
San Mateo, CA (CEG Dept. 'M', P.O. Box 3833, Stamford, CT 06905, 203/964-0000)
- **8-11 Barclay's Techmart**
Nat'l. Exhibition Centre, Birmingham, England (Tom Webb, British Trade Development Office, 212/593-2258)
- **9-11 Design Automation Workshop**
East Lansing, MI (Harry Hayman, P.O. Box, 639 Silver Spring, MD 20901, 301/589-8142, TWX 7108250437 IEEE Compso)
- **10-13 Computer Showcase Expo**
Cobo Hall, Detroit, MI (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **10-13 Computer Showcase Expo**
Civic Center, Atlanta, GA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **14-17 INFO '85**
New York Coliseum, New York, NY (Clapp & Poliak, 708 Third Ave., New York, NY 10017, 212/661-8010)
- **14-17 Int'l. Telecommunications Energy Conference (Intelec '85)**
Hilton Hotel, Munich, Federal Representative of Germany (Dr. Gunther Vau, Siemens A.G. Postfach, 3240 Erlangen 2, Fed. Rep. of Germany)
- **14-17 COMDEX/EUROPE**
RAI Congress & Exhibition Centre, Amsterdam, Netherlands (The Interface Group, 300 First St., Needham, MA 02194, 617/449-6600)
- **15-16 Practical Integrated Circuit Fabrication**
Boston, MA (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **15-20 Joint Power Generation Conference**
Hyatt Regency Hotel, Milwaukee, WI (Scott Patulski, WI Elect. Power Co., 231 W. Michigan Ave., Milwaukee, WI 52303, 414/277-2315)
- **16-18 1985 Ultrasonics Symposium**
Cathedral Hill Hotel, San Francisco, CA (W.R. Shreve, Hewlett Packard, 1501 Page Hill Rd., Palo Alto, CA 94304, 415/857-1501)
- **16-18 PC World Exposition**
Dallas Convention Center, Dallas, TX (Gene Bignami, Mitch Hall Associates, P.O. Box 860, Westwood, MA 02090, 617/329-7466)
- **17-20 PC Faire**
Civic Auditorium & Brooks Hall, San Francisco, CA (Computer Faire Inc., 570 Price Ave., Redwood City, CA 94063, 415/364-4294)
- **20-23 AEA Monterey Fall Financial Conference**
Hyatt Regency Monterey, Monterey, CA (Florence Lewis, AEA, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **20-Nov. 2 ITAME**
International Test & Measurement Exhibition and Conference, Olympia, London (British Trade Development Office, Tom Webb, 212/593-2258)
- **21-23 IEEE Military Communications Conference (Milcom '85)**
Stouffer's Bedford Glen, Bedford, MA (Frank Gicca, GTE *Products Corp.*, 77 A St., Needham Heights, MA 02194, 617/449-2000 Ext. 595)
- **21-24 AUTOTESTCON '85**
Long Island, NY (Louis A. Luceri, 660 Grand Ave., Lindenhurst, NY 11757, 516/567-9172)
- **22-24 NORTHCON/85**
High Technology Electronics Exhibition & Convention, Portland Memorial Coliseum, Portland, OR (Nancy Hogan, Jerry Fossler, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **22-24 MINI/MICRO NORTHWEST/85**
Computer Conference & Exhibition, Portland Memorial Coliseum, Portland, OR (Nancy Hogan, Jerry Fossler, Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **23-25 IEEE Professional Communication Conference (FCC '85)**
Annapolis, MD (Lois K. Moore, John Hopkins University, Room 14-132M, John Hopkins Rd., Laurel, MD 20707, 301/953-7100, Ext. 406)
- **23-25 Nuclear Science Symposium**
Sheraton Palace, San Francisco, CA (R.S. Larsen Stanford Linear Accelerator Center., Stanford University, P.O. Box 4349, Stanford, CA 94305, 415/854-9300, Ext. 2726, FTS: 461-9300, Ext. 2726)
- **23-25 Symposium on Nuclear Power Systems**
sheraton Palace, San Francisco, CA (R.S. Larsen Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, CA 94305, 415/854-9300, Ext. 2726, FTS: 461-9300, Ext. 2726)
- **24-27 Computer Showcase Expo**
McCormick Place, Chicago, IL (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **28-Nov. 1 Systems '85**
Munich, Germany (Jerry Kallman, Kallman & Associates, 212/652-7070)
- **29-31 Test**
Electronic Test & Measuring Instrumentation Exhibition, Wembley Conference Centre, London (Tom Webb, British Trade Development Office, 212/593-2258)
- **29-31 Landmobile Communications Showcase**
Convention Center, New Orleans, LA (Electronic Industries Associations Telecommunications Group, 202/457-4935)
- **29-31 ATE Central**
O'Hare Exposition Hall, 9291 West Bryn Mawr, Rosemont, IL (Jerry L. Pugh, Morgan Grampian Expo. Group, 2 Park Ave., New York, NY 10016, 212/340-9780)

RELAYS FROM "A-Z"



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CIRCLE NO 61

EDN

CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

November 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1	2
3	4	5 ELECTION DAY	6	7	8	9
10	11 VETERAN'S DAY	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28 THANKSGIVING DAY	29	30

- **1-3 Computer Showcase Expo**
Curtis-Hixon, Tampa, FL (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **4-8 Composants**
Paris, France (Pierre Wagner, 212/869-1720)
- **7-10 Computer Showcase Expo**
Convention Center, Los Angeles, CA (The Interface Group, 300 First Ave., Needham, MA 02194, 617/449-6600)
- **11-13 Conference on Software Maintenance '85**
Sheraton Inn, Washington N.W. Silver Spring, MD (Software Maintenance, P.O. Box 639, Silver Spring, MD 20901, 301/589-8142, TWX 7108250437, IEEE Compso)
- **12-13 Practical Integrated Circuit Fabrication**
Scottsdale, AZ (Pat Fruscello ICE, 15022 N. 75th St., Scottsdale, AZ 85260, 602/998-9780, Telex: 165-755 ICE, Scot)
- **12-16 Productronica**
Munich, Germany (Jerry Kallman, Kallman & Associates, 201/652-7070)
- **18-22 11th Symposium on Fusion Engineering**
Hyatt Regency Austin, Austin, TX (Harlan Ward Harris (RLM 12.208) Fusion Research Center, University of Texas, Austin, TX 78712, 512/471-4576-4698)
- **19-21 Wescon/85**
Moscone Center, San Francisco, CA (Jerry Fossler, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)
- **20-24 COMDEX/FALL '85**
Las Vegas Convention Center, Las Vegas, NV (The Interface Group, 300 First St., Needham, MA 02194, 617/449-6600)

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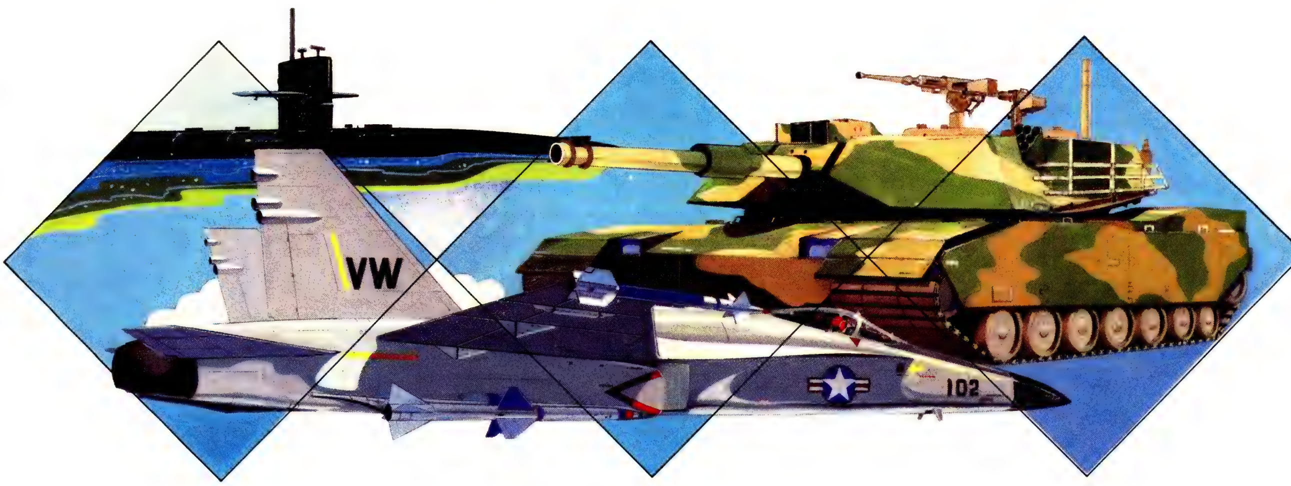

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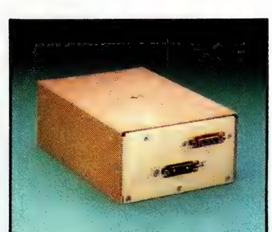
150W Single
5/12/15/24/28 VDC @
30/12.5/10/6.3/5.3A†
7″L x 3.5″W x 2.625″H



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CIRCLE NO 62

EDN

CALENDAR OF ELECTRONICS AND COMPUTER INDUSTRY EVENTS

December 1985

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25 CHRISTMAS DAY	26	27	28
29	30	31				

- **2-5 Global Telecommunications Conference '85**
Hyatt Regency, New Orelans, LA (G.A. Ledbetter, South Central Bell, 365 Canal Street, New Orleans, LA 70140, 504/528-7350)
- **3-5 Semicon/Japan**
Tokyo Int. Trade Center, Tokyo, Japan (Semiconductor Equipment & Materials Institute, 625 Ellis St., Suite 212, Mt. View, CA 94043, 415/964-5111)
- **4-6 AEA Financial Conference for Emerging Growth Companies**
Bonaventure Hotel, Fort Lauderdale, FL (David McKell, AEA, 2670 Hanover Street, P.O. Box 10045, Palo Alto, CA 94303, 415/857-9300)
- **8-13 10th Annual Int'l. Conference on Infrared & M/M Waves**
Lake Buena, Vista, FL (Prof. Kenneth J. Button, MIT Nat'l. Magnet Lab. Bldg., N.W. 14 Cambridge, MA 02139, 617/253-5561)
- **10-12 The First Int'l. Conference on Super Systems**
Hilton Inn, St. Petersburg, FL (Supersystems, P.O. Box 639, Silver Spring, MD 20901, 301/589-8142, TWX 7108250437, IEEE Compso)
- **11-13 DEXPO/WEST**
Anaheim, CA (Expoconsul International)

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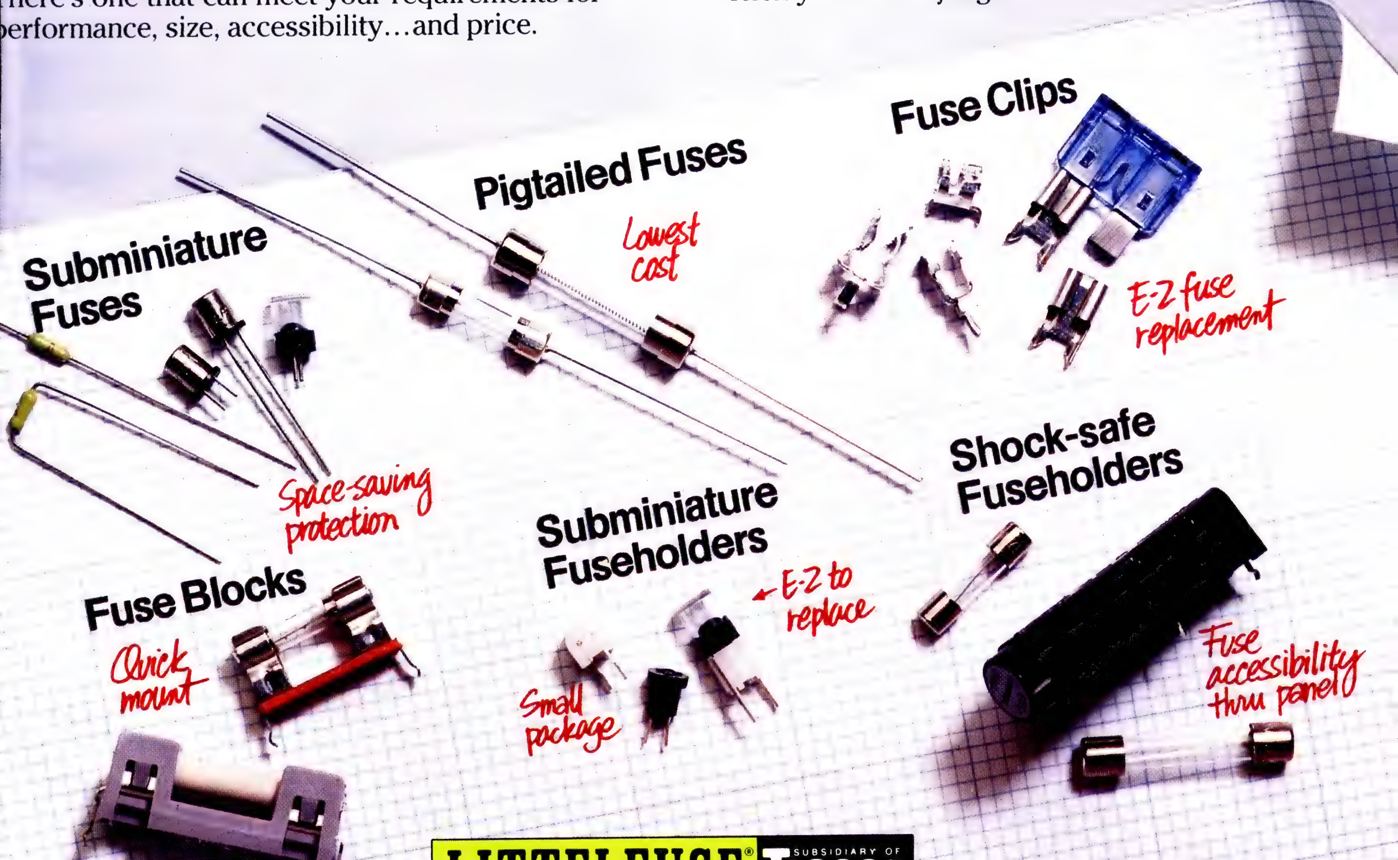

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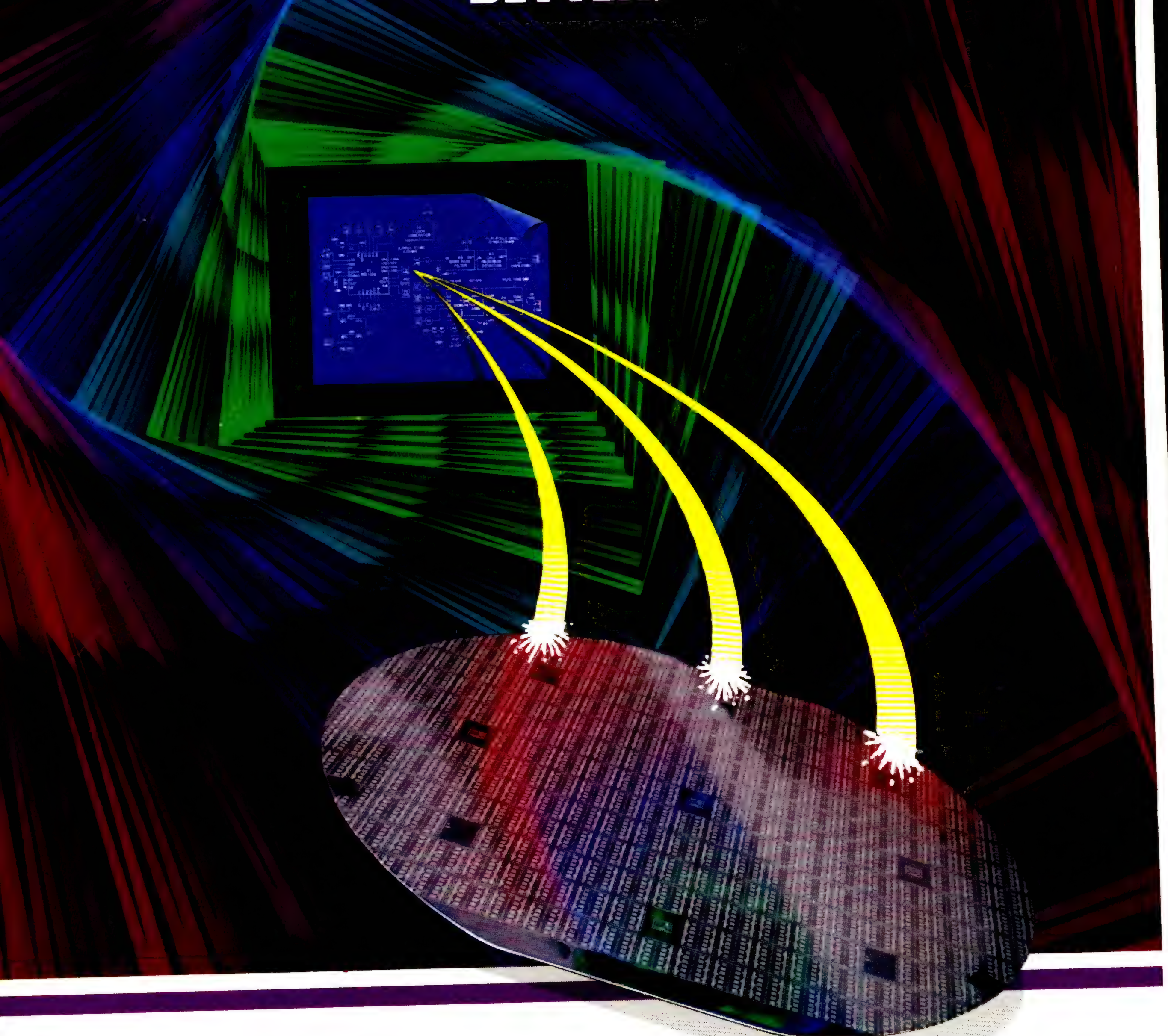

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CIRCLE NO 201

EDITED BY ROBERT M CLARKE

Algorithm produces base-2 logarithms

Robert D Grappel,
Compdata Services Corp, Wellesley, MA

To most programmers, an algorithm that computes a logarithm is something hidden in the bowels of a compiler or math package. Typically, the computation involves floating-point operations and series expansions. Nevertheless, an algorithm exists that lets you quickly and easily calculate base-2 logarithms, even using μPs.

The algorithm uses the fact that a binary number can be represented as the sum of a series of powers of two in which each power is multiplied by either a zero or one coefficient. Thus, you can represent the number as a series of bits, each zero or one, with each bit's position corresponding to a power of 2. For example, the binary string 0110 represents

$$0\times2^3+1\times2^2+1\times2^1+0\times2^0.$$

(For further theory, see "Exponential and Logarithm by Sequential Squaring," *IEEE Transactions on Computers*, Vol C-33, No 5, May 1984.)

Consider a subroutine example that implements the algorithm. First, note that this example uses a scaled integer representation for the arguments for the logarithm subroutine. The assumed decimal point lies between bits 14 and 15 of a 16-bit value. Assume that the real argument value has been multiplied by 2^{14} (16,384) and is now an integer. The subroutine uses 16- and 32-bit integer operations. Its output is a scaled 16-bit fraction whose assumed decimal point is to the left of bit 16. Hence, the subroutine produces results significant to about 16 places.

Second, the example requires that the argument be between 1.0 and 2.0. This isn't a great hardship, because values outside this range can be scaled to fit, and the return value from the logarithm routine can be adjusted. Scaling base-2 values requires only shifting and adding, which isn't too difficult to accomplish. The scaling code is not shown here.

The code in **Fig 1** shows how you can implement the algorithm in C. Integers are assumed to be represented in 32 bits. The array "L" stores the bits of the 16-bit logarithm.

You can also implement the algorithm on a μP. **Fig 2**'s code shows how simply you can write the subroutine in Motorola 68000 assembly language. Note that with the scaling factor chosen, there's no danger of overflow in the multiplication step. Shifts do all the divisions. The order of bits is reversed to match Motorola's format.

You can calculate logarithms in other bases by multiplying the base-2 logarithms by the appropriate constant, which is simply the base-2 logarithm of the desired base. This multiplication requires 32 bits of precision because the constant scaled will exceed 16 bits. **EDN**

```
#define SCALE 16384      /* 14-bit scaling constant */

int x;          /* the argument, whose base-2 log. is desired */
int i;          /* bit counter index for L */
char L[16];     /* bits of the logarithm base-2 of x */

for (i=0;  i  <  16;  i++)
    {/*  loop through 16 bits of L  */
     L[i] = 0;          /* initialize bit */
     x *= x;            /* square x */
     x /= SCALE;        /* re-scale its value */
     if (x >= (2 * SCALE))
       {
        L[i] = 1;       /* set bit in logarithm */
        x /= 2;         /* ready for next position */
       }
```

*Fig 1—**Calculate base-2 logarithms** to about 16 bits of precision using the algorithm implemented in this C code.*

```
    }
*   Rodister usage:  D0 argument (input) and logarithm base-2 (output)
*                    D1 logarithm temporary
*                    D2 bit index
*                    D3 scale factor
*
LOG0    MOVEM.L D1-D3,-(A7)      SAVE REGISTERS
        MOVEQ #0,D1              INIT. LOG. TEMP.
        MOVEQ #15,D2             INIT. BIT INDEX
        MOVEQ #14,D3             INIT. SCALE FACTOR
*
LOG1    MULU D0,D0               SQUARE ARGUMENT
        LSR.L D3,D0              RE-SCALE ARGUMENT
        CMPI.W #32768,D0         ARG < BASE-2?
        BLO.S LOG2               YES
*
        BSET D2,D1               NO, SET BIT IN LOGARITHM
        LSR.W #1,D0              READY FOR NEXT POSITION
*
LOG2    DBRA D2,LOG1             LOOP THROUGH THE 16 BITS
*
        MOVE.L D1,D0             RETURN LOGARITHM IN D0
        MOVEM.L (A7)+, D1-D3     RESTORE WORKING REGISTERS
        RTS
```

*Fig 2—**You can easily** calculate base-2 logarithms on a μP, as this Motorola 68000 assembly-language subroutine shows.*

To Vote For This Design, Circle No 746

Build a quick and easy cable checker

Ed Chapman,
Eastman Kodak Co, Rochester, NY

The circuit in **Fig 1** gives you a quick and easy way to test cables. It performs two separate checks: It tests for cable continuity and for short circuits between adjacent conductors. The circuit tests 8-conductor cables, but you can build a checker for any size cable.

The checker can detect one or more problems in a cable. If a short or open circuit exists, then one of the checker's hexadecimal displays will display a digit corresponding to the problem. The **table** lists the digits displayed and the corresponding open- or short-circuited conductors.

To check continuity, you connect the cable under test

TABLE—CABLE CHECKER HEXADECIMAL DISPLAYS

DISPLAY (HEX)	CONTINUITY TEST	SHORT TEST
F	1,2,3,4,5,6,7,8	GOOD
E	3,4,5,6,7,8	1,2,3
D	1,2,5,6,7,8	3,4,5
C	5,6,7,8	1,2,3,4,5
B	1,2,3,4,7,8	5,6,7
A	3,4,7,8	1,2,3,5,6,7
9	1,2,7,8	3,4,5,6,7
8	7,8	1,2,3,4,5,6,7
7	1,2,3,4,5,6	7,8
6	3,4,5,6	1,2,3,7,8
5	1,2,5,6	3,4,5,7,8
4	5,6	1,2,3,4,5,7,8
3	1,2,3,4	5,6,7,8
2	3,4	1,2,3,5,6,7,8
1	1,2	3,4,5,6,7,8
0	GOOD	1,2,3,4,5,6,7,8

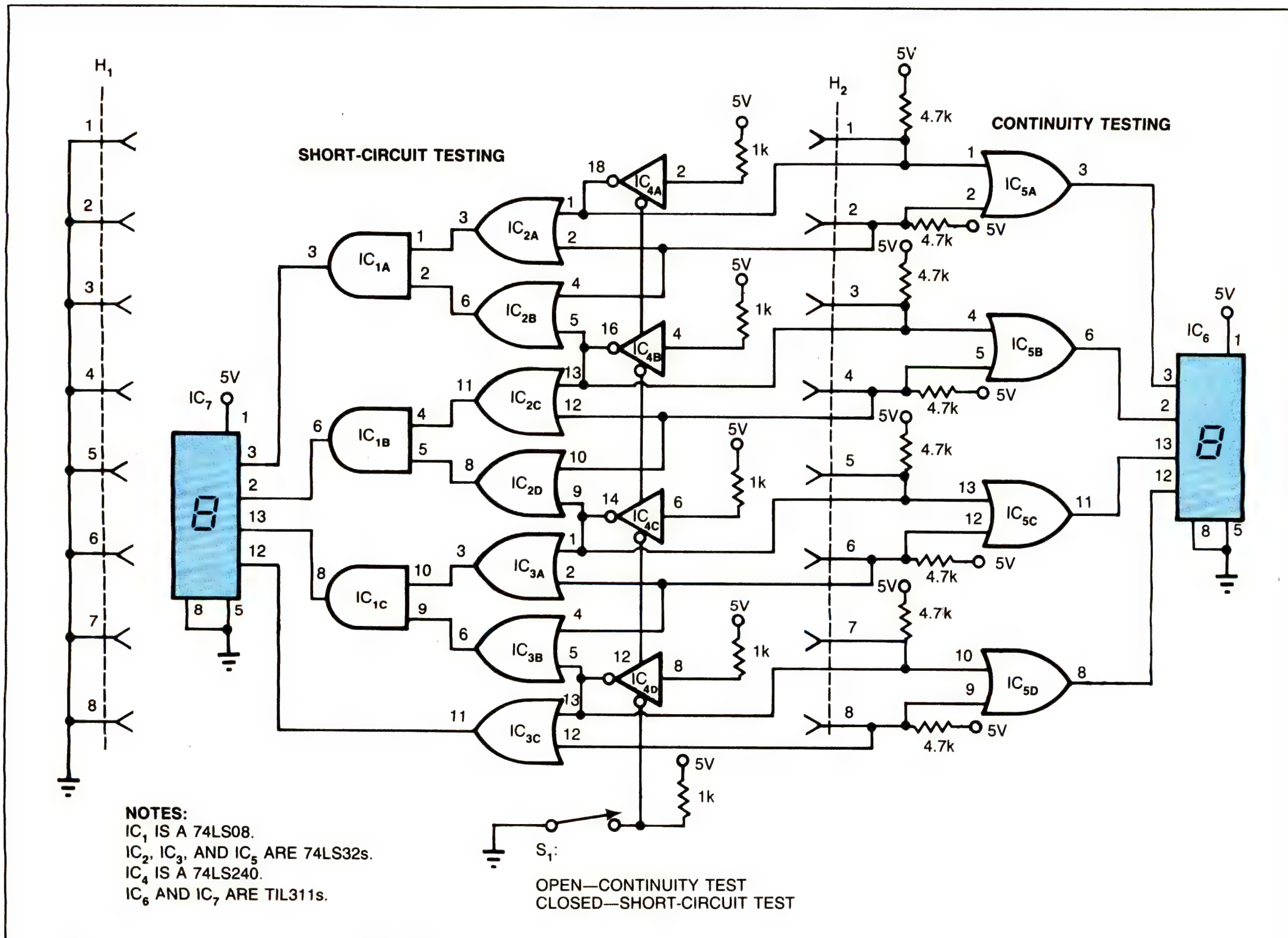

***Fig 1—This cable checker** identifies open conductors and shorts between adjacent conductors in multiconductor cables. It uses a hexadecimal display to indicate the detected problems.*

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SBL-1	world's lowest cost industrial mixer, only $4.50, metal case	1-500	DC-500	5.5 typ.	6.5 typ.	50 typ.	45 typ.	35 typ.	3.95 (100) 4.50 (10-49)
SBL-1X	industrial grade, rugged all-metal construction	10-1000	5-500	6.0 typ.	7.0 typ.	50 typ.	40 typ.	30 typ.	11.95 (1-9)
ASK-1	world's smallest DBM flatpack mounting, plastic case	1-600	DC-600	5.5 typ.	6.0 typ.	50 typ.	35 typ.	30 typ.	5.95 (10-49)
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CIRCLE NO 145

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to headers H_1 and H_2. Then you open switch S_1, which places IC_4's 3-state buffers into the high-impedance-output state and protects them from being directly short-circuited to ground through H_2. If the cable has no open-circuited conductors, then hexadecimal display IC_6 will read 0. An open conductor in the cable will prevent the ground in H_1 from pulling one of the inputs to IC_5's OR gates low, and IC_6 will show the hexadecimal code corresponding to the problem.

The short-circuit test checks for shorts between adjacent conductors. To perform this test, connect the cable under test to H_2 only. Then close switch S_1; this action pulls one input to each of the OR gates in IC_2 and IC_3 low. The other input of each of the OR gates, assuming open-circuited inputs to H_2, should be high. If there are no short circuits between adjacent pins in the cable, then IC_7 will display F_{HEX}. A short circuit in the cable will cause both inputs to the OR gate to be pulled low, and IC_7 will display the hexadecimal code identifying the cable's condition. **EDN**

To Vote For This Design, Circle No 748

Improve voltage-controlled current source

Giovanni Stocchino,
FATME, Rome, Italy

Although you can use various methods to design voltage-controlled current sources, the design you use to eliminate one problem can easily lead to other problems. By using op amps and feedback, though, you can build a circuit that furnishes high precision, wide output-current range, high ac/dc output impedance, good temperature stability, low noise, and high input impedance.

As **Fig 1** shows, you can use an emitter follower and various circuit techniques to compensate for the inaccuracies introduced by parameters such as the transistor's base current and wiring resistance (see "Op amps compensate current source," EDN, September 15, 1983, pg 227). This approach, however, introduces the problems of lower input impedance and higher equivalent input-noise-voltage contribution from input resistors R_{IN}. Moreover, the op amp's input-offset current produces a temperature-dependent offset voltage across R_{IN} that increases the total output-current error. Finally, the error introduced by the transistor's temperature-dependent input impedance also reduces

Continued on pg 294

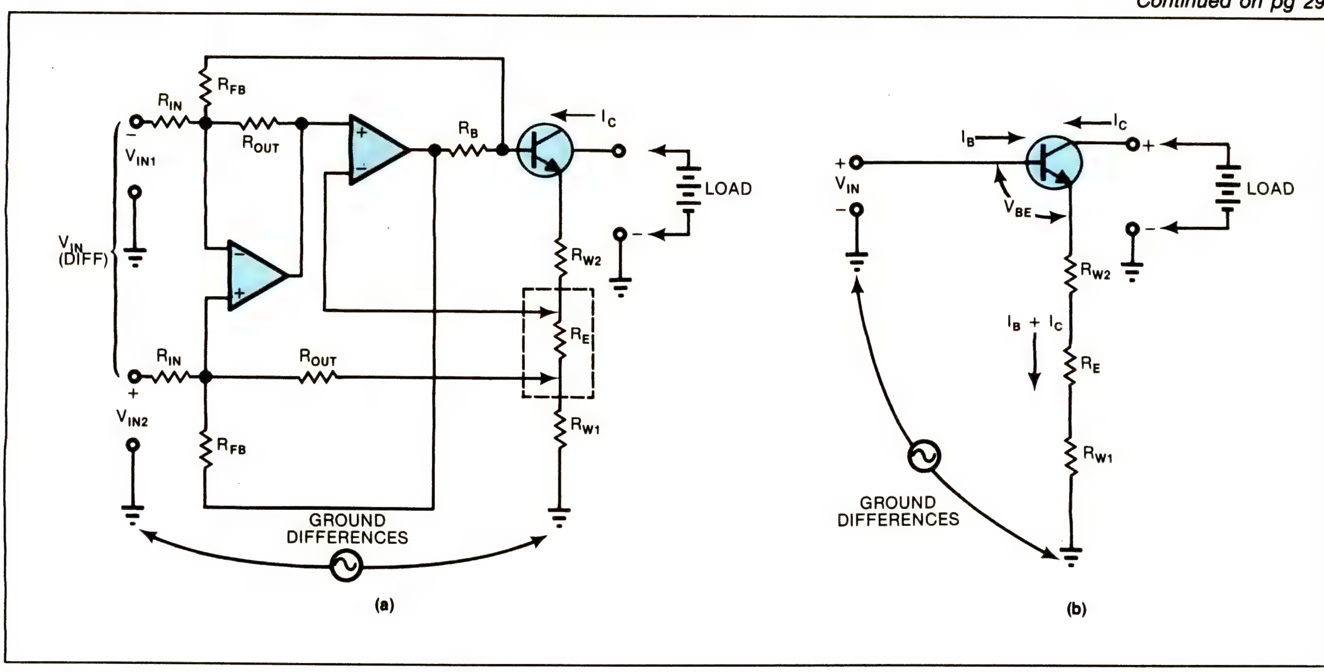

*Fig 1—**A circuit (a) incorporating several modifications** to a basic emitter-follower current source **(b)** eliminates errors caused by wiring resistance, common-mode signals, and the transistor's finite base current. However, the modifications introduce offset-current and equivalent input-noise errors and give the circuit a low input impedance.*

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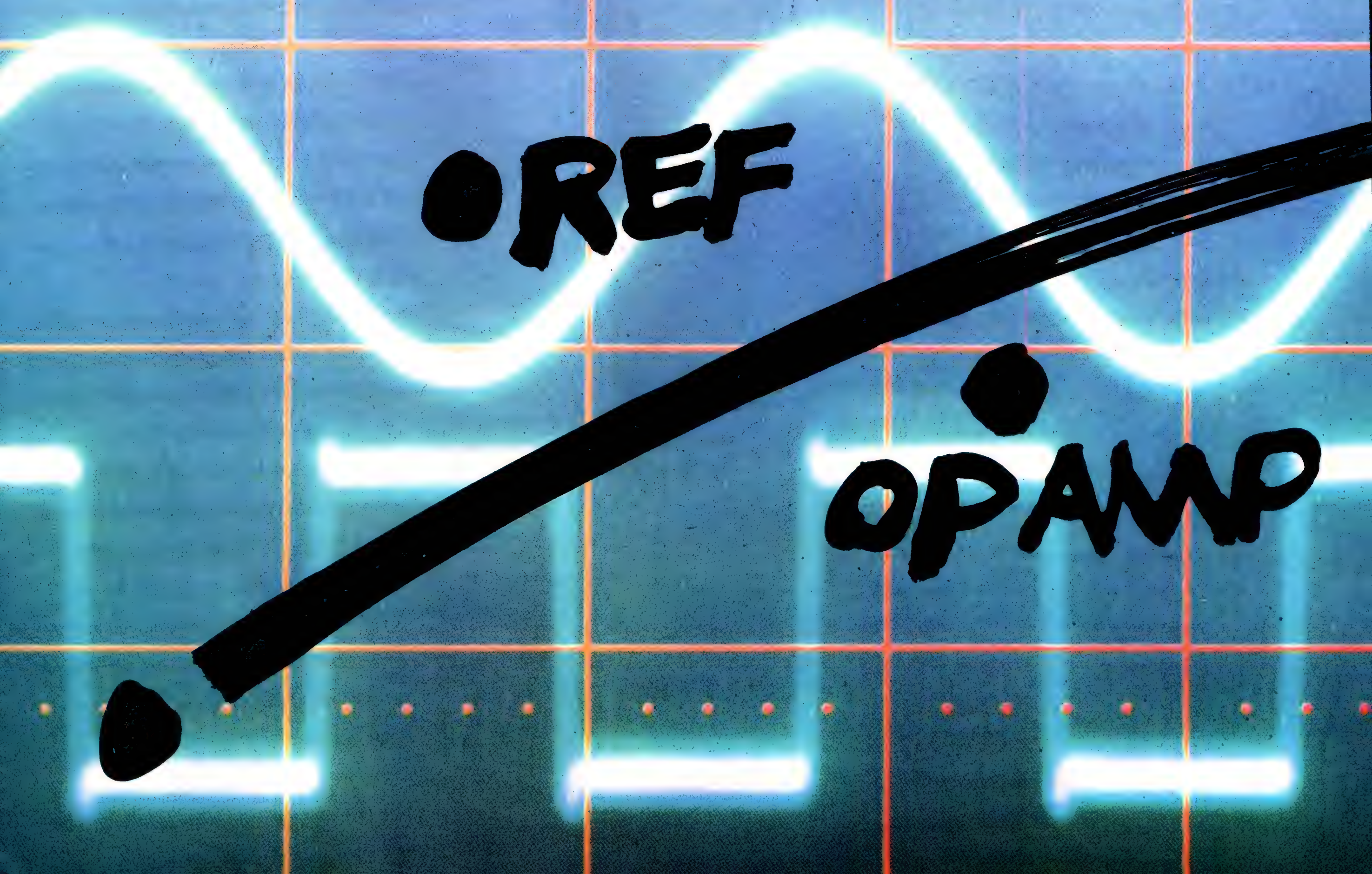

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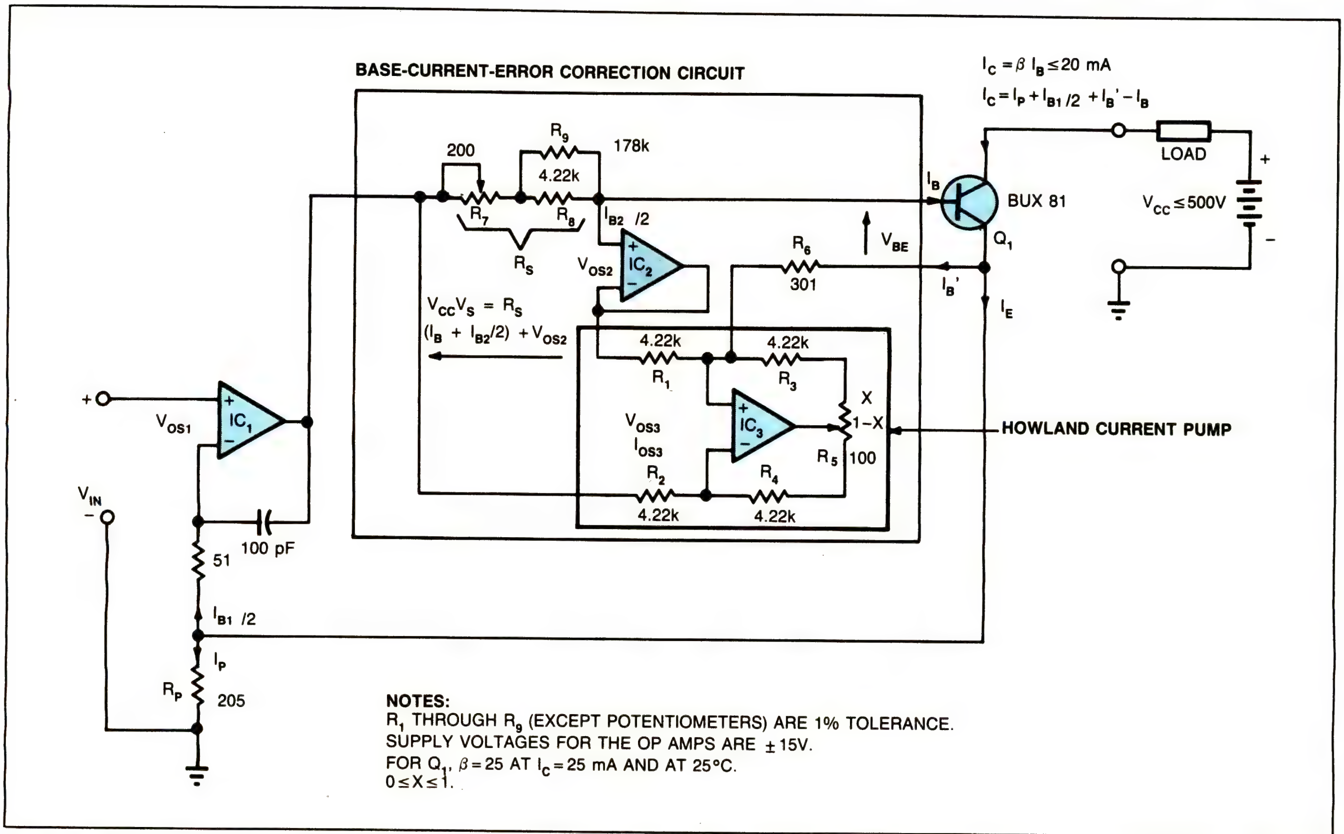

Fig 2—This improved voltage-controlled current source *almost completely cancels base-current-induced error, has high input and output impedances, and features excellent compliance and a wide output range.*

circuit accuracy. You can reduce this last error contribution by inserting a voltage follower between the transistor's base and feedback resistor R_{FB}.

Fig 2's voltage-controlled-current source uses a technique that almost completely cancels the error caused by the transistor's finite base current. The technique neither affects the circuit's input characteristics nor increases the error contributions from other sources. The circuit consists of the standard op-amp-plus-transistor current source (Q_1 and IC_1) plus the insertion of a base-current error-correction circuit (IC_2 and IC_3). The circuit's output current is given by the expression

$$I_C = \frac{V_{IN}}{R_p}.$$

The circuit corrects the base-current error as follows. Q_1's base current, I_B, causes a voltage drop across R_S. This drop ($I_B R_S$), through noninverting-buffer IC_2, drives a Howland current pump consisting of IC_3 and resistors R_1 through R_6 (see "Improve circuit performance with a 1-op-amp current pump," EDN, January 20, 1983, pg 85). The Howland current pump's output,

$$I_B \approx I_{B'},$$

is then summed with the transistor's emitter current to cancel the emitter current's base-current component and thus leaves only the collector-current contribution. This process makes the voltage drop across R_P and the feedback to IC_1 independent of base current. Thus, the circuit eliminates the base-current contribution error.

The expression for I_B' is

$$I_B = \frac{R_S}{R_1} I_B + \frac{V}{R_S + XR_5}\left\{\frac{R_4 + (1-X)R_5}{R_2} - \frac{R_3 + XR_5}{R_1}\right\} \pm \epsilon \pm \gamma I_B, \quad (1)$$

where

$$V \approx \frac{R_6 R_5 I_B}{R_1} - V_{BE},$$

$$\epsilon \le \frac{R_S}{R_1} \cdot \frac{I_{B2}}{2} + I_{OS3} + \frac{1}{R_1}(V_{OS2} + V_{OS3}),$$

$$\gamma \le \frac{R_6}{R_1}\left(\frac{1}{A_0} + \frac{1}{CMRR}\right),$$

and

I_B = input bias current,
I_{OS} = input offset current,
V_{OS} = input offset voltage,
A_0 = op amp open-loop gain,
CMRR = common-mode rejection ratio.

Because the circuit incorporates precision op amps, ϵ and γ have very low values; for example, $\epsilon \le 50$ nA and $\gamma \le 10^{-6}$.

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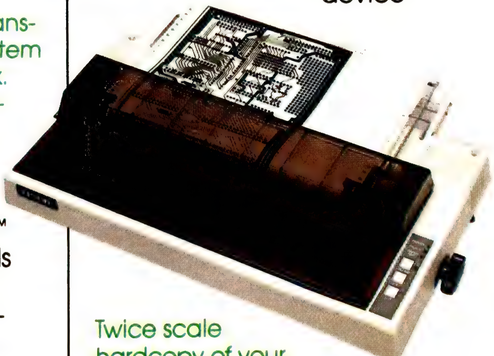

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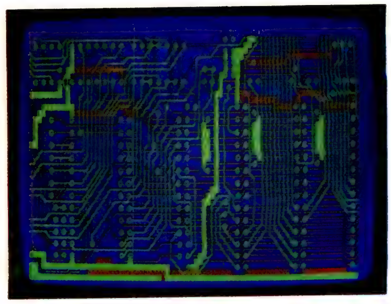

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For the circuit to operate properly, you must use low-temperature-coefficient resistors. Also, you have to adjust R_5 and R_7 to meet the following conditions:

$$R_S = R_1 \tag{2}$$

and

$$\frac{R_4 + (1 - X)\,R_5}{R_2} = \frac{R_3 + XR_5}{R_1}. \tag{3}$$

When these conditions are satisfied, **Eq 1** reduces to

$$I_{B'} = I_B \pm \epsilon \pm \gamma\, I_B$$

and the circuit's output current is

$$I_C = I_P + \frac{I_{B1}}{2} + I_{B'} - I_B = I_P + \frac{I_{B1}}{2} \pm \epsilon \pm \gamma\, I_B. \tag{4}$$

Bearing in mind that

$$I_B = \frac{I_C}{\beta},$$

where β is Q_1's current gain, and that

$$I_P = \frac{(V_{IN} \pm V_{OSI})}{R_P},$$

then you can express d, the maximum deviation of the circuit's output current I_C from the ideal value

$$I_P = \frac{V_{IN}}{R_P},$$

using the expression

$$d = I_C - \frac{V_{IN}}{R_P} = \pm\left\{\frac{\gamma}{\beta}\frac{V_{IN}}{R_P} + \frac{V_{OSI}}{R_P} + \frac{I_{B1}}{2} + \epsilon\right\} \tag{5}$$
$$= \pm\, 5 \times 10^{-8}\,\frac{V_{IN}}{R_P} \pm 90\ \text{nA}.$$

Note that this expression holds only when the conditions of **Eqs 2** and **3** are met. The prototype of this circuit has shown an accuracy better that 0.002% of full output (20 mA), with a ±20 mA residual error. **EDN**

To Vote For This Design, Circle No 749

Inter-IC bus addresses individual devices

Hans Wijnen,
Philips Elcoma, Eindhoven, The Netherlands

Once you've written the software to address an IC on the Inter-IC (I^2C) bus, you don't have do an extensive rewrite to add other devices to the bus. This example shows how you can write two bytes of data at a time to a CMOS serial RAM using the 8-line bus.

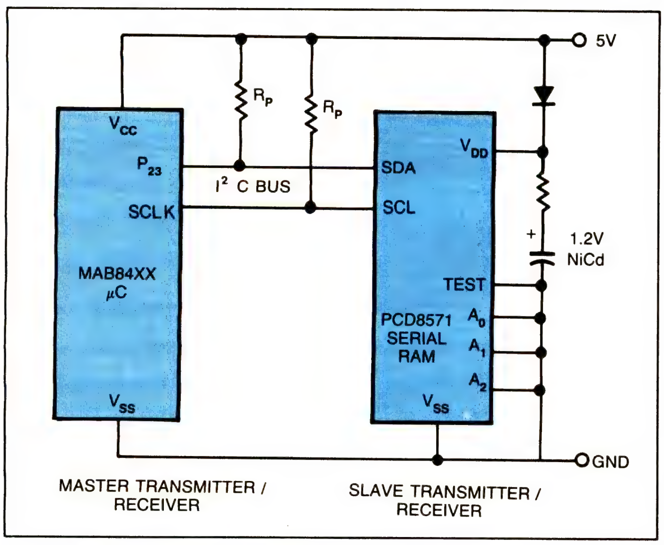

***Fig 1—The Inter-IC (I²C) bus** lets you individually address each device connected to it, allowing you to write modular programs.*

SERIAL I/O STATUS WORD, REGISTER S_1

	BIT 7							BIT 0
WRITE					ES0	BC2	BC1	BC0
READ	MST	TRX	BB	PIN	AL	AAS	AD0	LRB

MNEMONIC	MEANING
MST	- UNITS ON THE I^2C BUS CAN EITHER BE MASTER (1) OR SLAVE (0)
TRX	- UNITS CAN EITHER BE TRANSMITTER (1) OR RECEIVER (0)
BB	- BUS BUSY
PIN	- PENDING INTERRUPT NOT (FOR SERIAL INTERRUPT REQUEST)
ES0	- ENABLE SERIAL OUTPUT
BC0,1,2	- NUMBER OF DATA BITS TRANSMITTED OR RECEIVED IN THE SERIAL DATA STREAM
AL	- ARBITRATION LOST
AAS	- ADDRESSED AS SLAVE
AD0	- ADDRESS ZERO - DETECTS GENERAL CALL TO ALL UNITS ON THE BUS
LRB	- LAST RECEIVED BIT (EITHER LAST BIT RECEIVED OR, FOR TRANSMIT, THE ACKNOWLEDGE BIT).

***Fig 2—This status word** lets you determine what the I²C bus is doing.*

In **Fig 1**, the I^2C bus connects an MAB8400 Series µC and a PCD8571 128×8-bit static RAM. The bus has eight lines: two for serial data transfer, three for addressing, one for a test input, and two for the power supply. Register S_1 in the µC can either monitor or set the bus's status using a serial-I/O status word (**Fig 2**). Devices attached to the bus interact in a master-slave relationship with each device functioning as a bus

Continued on pg 300

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HC-5504	SLIC	Ring generator referenced to negative battery supply
HC-5508	SLIC	Reconfigured and enhanced version of HC-5504
HC-5510/11	PCM CODECs	μlaw/A-law coding with signaling capabilities
HC-5512/12A	PCM Filters	Exceed all D3/D4 CCITT specifications
HC-5512D	PCM Filter	MIL spec
HC-5554/57	CODEC/Filters	μlaw/A-law COMBOs
HC-5541A	Dialer	Pulse-tone dialer
HC-55536/64	CVSD	Real-time speech processors
HF-10	UAF	Univ. Act. Filter, MIL Temp.

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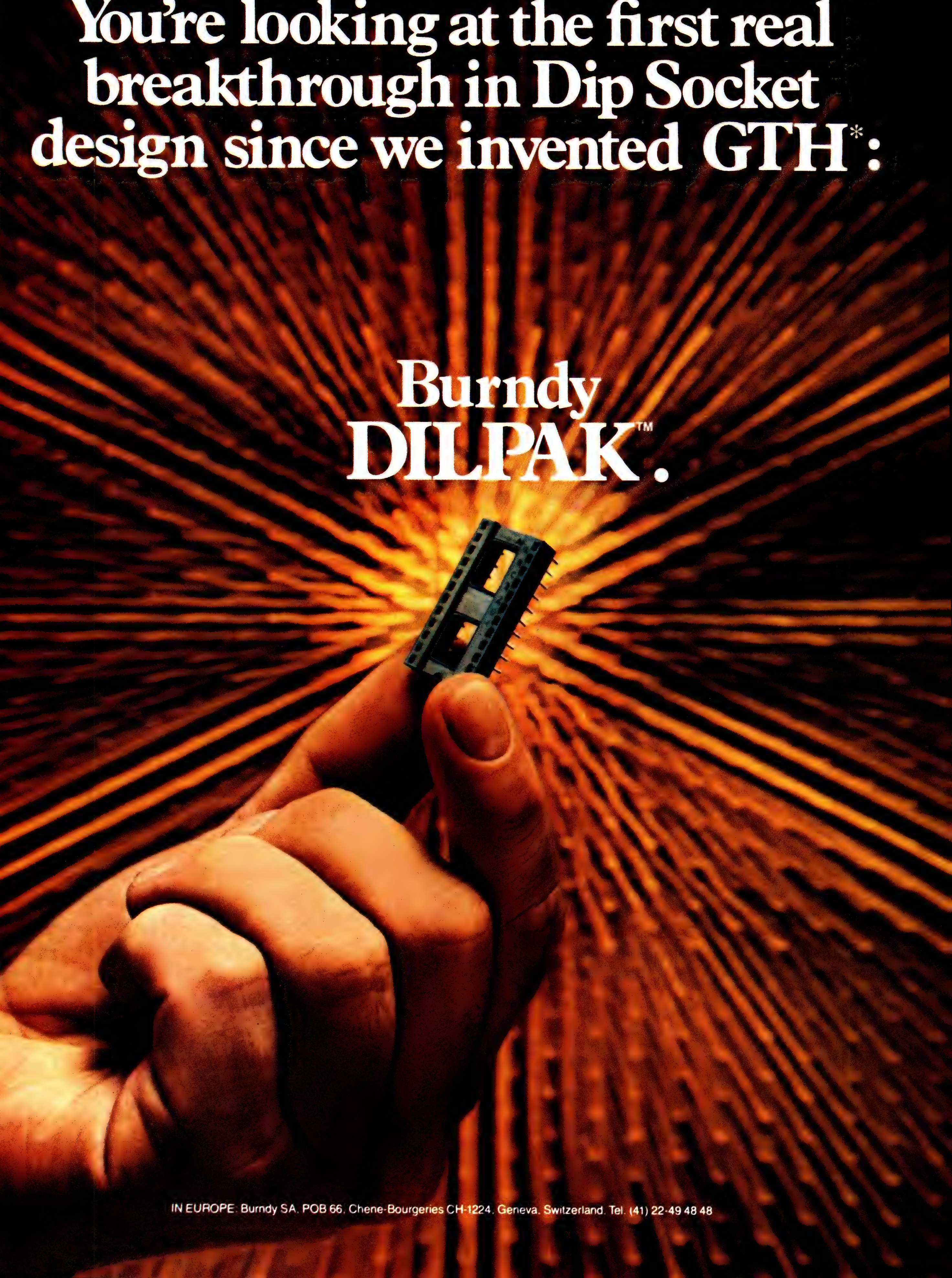
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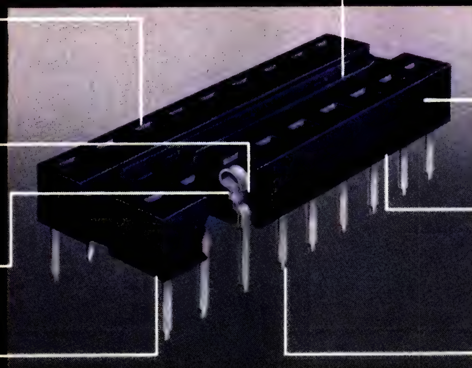

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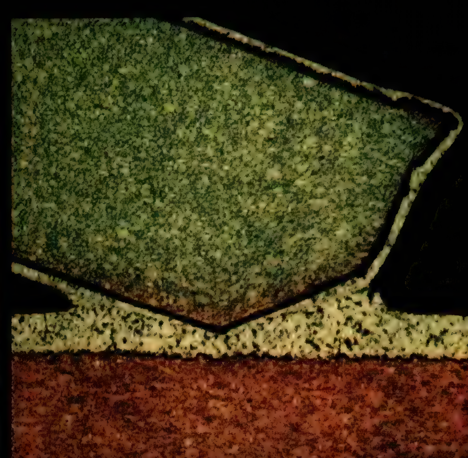

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transmitter or a bus receiver as the situation demands. In this example, one µC acts as the bus controller or master and a RAM acts as the slave.

Fig 3a lists a subroutine that causes a single master µC to write two bytes to memory. This subroutine first sets the PIN (pending interrupt not) and ESO (enable serial output) bits, which reset the I^2C bus logic and enables the serial I/O, respectively. It then loads the memory address and the direction bit into data shift register S_0. Then the µC, acting as the master transmitter, occupies the bus by writing $F8_{HEX}$ into S_1.

Once the bus is occupied, the subroutine calls yet another subroutine—designated MTTBS and shown in **Fig 3b**—to test the bus's status. Two conditions can cause the master to retire and try the bus later: either a negative acknowledge (bus high) or a discrepancy between the data which the bus master has placed on the bus via S_0 and the data actually on the bus. If, however, the MTTBS receives a positive acknowledge and finds no discrepancies, it returns to the top-level subroutine.

Continued on pg 307

SINGLE-MASTER SYSTEM ROUTINE:

```
ADDR    HEX                  MNEM   INSTR.        NOTES

00011B  9D18   WMEM          MOV    S1, #PIN+ESO  RESET BUS STATUS
00011D  9CA0                 MOV    S0, #MEMAD    LOAD MEMORY SLAVE ADDRESS AND WRITE BIT
00011F  9DF8                 MOV    S1, #STRTC    OUTPUT START COND, SLAVE ADDRESS AND WRITE BIT
000121  3438                 CALL   MTTBS         TEST BUS STATUS
000123  9635                 JNZ    WMEM1         JUMP IF NO ACKN. RECEIVED OR ERROR
000125  FD                   MOV    A,R5          FETCH POINTER VALUE
000126  3C                   MOV    S0,A          TRANSMIT POINTER VALUE
000127  3438                 CALL   MTTBS         TEST BUS STATUS
000129  9635                 JNZ    WMEM1         JUMP IF NO ACKN., RECEIVED OR ERROR
000128  F9                   MOV    A,R1          FETCH FIRST DATA BYTE
00012C  3C                   MOV    S0,A          TRANSMIT DATA BYTE 1
00012D  3438                 CALL   MTTBS         TEST BUS STATUS
00012F  9635                 JNZ    WMEM1         JUMP IF NO ACKN. RECEIVED OR ERROR
000131  FA                   MOV    A,R2          FETCH SECOND DATA BYTE
000132  3C                   MOV    S0,A          TRANSMIT DATA BYTE 2
000133  3438                 CALL   MTTBS         TEST BUS STATUS
               *
000135  9DD8   WMEM1         MOV    S1,#STOPC     OUTPUT STOP CONDITION
000137  83                   RET
```

(a)

MASTER TRANSMITTER TEST BUS STATUS SUBROUTINE:

```
000138  OD     MTTBS         MOV    A,S1          FETCH BUS STATUS
000139  F23C                 JB7    MTTBS1        JUMP IF MST = 1
00013B  83                   RET
               *
00013C  9238   MTTBS1        JB4    MTTBS         JUMP IF PIN = 1
00013E  D3E0                 XRL    A,#MTTST      TEST MST/TRX BUS STATUS
000140  83                   RET
```

(b)

CALL ADDRESS:	SUBROUTINE CALL $[A_{10}A_9A_8 1\ 0100\ A_7A_6A_5A_4\ A_3A_2A_1A_0]$
JB ADDRESS:	JUMP IF ACCUMULATOR BIT IS SET $[B_2B_1B_0\ 1\ 0010\ A_7A_6A_5A_4\ A_3A_2A_1A_0]$
JNZ ADDRESS:	JUMP IF ACCUMULATOR IS NOT ZERO $[1001\ 0110\ A_7A_6A_5A_4\ A_3A_2A_1A_0]$
MOV A,R_R:	MOVE REGISTER CONTENTS TO ACCUMULATOR [1111 1RRR]
MOV A,S_N:	MOVE SERIAL I/O REGISTER CONTENTS TO ACCUMULATOR [0000 11NN]
MOV S_S**,A:**	MOVE ACCUMULATOR CONTENTS TO SERIAL I/O REGISTER [0011 11SS]
MOV S_S, #DATA:	MOVE IMMEDIATE DATA TO SERIAL I/O REGISTER $[1001\ 11SS\ D_7D_6D_5D_4\ D_3D_2D_1D_0]$
RET:	RETURN WITHOUT PSW RESTORE [1000 0011]
XRL A, #DATA:	LOGICAL XOR ACCUMULATOR WITH IMMEDIATE MASK $[1101\ 0011\ D_7D_6D_5D_4\ D_3D_2D_1D_0]$

(c)

Fig 3—You can tranfer data on the bus *using the subroutine in* ***a****. Using* ***b****'s subroutine, you can check the bus's status. The program's mnemonics and data formats are listed in* ***c****.*

S	MEM ADR	W	A	POINT	A	DATA1	A	DATA 2	A	P

SERIAL-DATA FORMAT MNEMONIC MEANING

S = START CONDITION
MEM ADR = SLAVE ADDRESS
A = ACK
W = WRITE BIT (WRITE = 0)
POINT = ADDRESS AT WHICH DATA IS TO BE WRITTEN
P = STOP

S = START CONDITION
MEM ADR = SLAVE ADDRESS
A = ACK
W = WRITE BIT (WRITE = 0)
POINT = ADDRESS AT WHICH DATA IS TO BE WRITTEN
P = STOP

Fig 4—This data-transfer format *shows how information is passed along the I²C bus.*

Fig 3c lists the assembly-language mnemonics and their data formats.

Fig 4 shows the data-transfer format. At this point, the accumulator is 0, and R_5 holds the pointer to the address where the data is to be stored. The top-level subroutine now transmits the pointer value to the RAM and again tests the bus's status. If the bus passes, the μC transmits bytes 1 and 2 (stored in registers R_1 and R_2, respectively) to the RAM. The subroutine then signals the output-stop condition by loading $D8_{HEX}$ into register S_1. Hardware clears bits MST and TRX if the stop condition is executed.

If the bus is free (SDA and SCL are both high), the μC can transmit on the bus by first generating a start condition and then writing the device's address and the direction bit to the device being addressed—in this case, the serial RAM.

The RAM (now acting as a slave receiver) recognizes the start condition, reads the slave address and direction bit, and produces an acknowledge signal (low) when it receives its own address. The second byte transferred is the pointer (the address where the data is to be stored); the memory holds this in an internal address register. The third and subsequent bytes transferred are the data to be stored. The address register is incremented after the reception of each data byte. **EDN**

To Vote For This Design, Circle No 750

PLD implements 1-chip password decoder

Philippe Larcher,
CIMSA, Velizy, France

A programmable logic device (PLD) proves to be nearly ideal for implementing secret-code or access-key protection schemes. Usable in systems with restricted access to physical resources, PLDs are compact size and inexpensive, and they furnish a high level of security.

The design outlined in the accompanying **table** and **figures** uses an AmPAL22V10 PAL device; you can access the secret code programmed in the PAL only by using the correct sequence of input variables and internal states. Three successive decoding laws control the internal state transitions, and the transitions are invisible from outside the PAL.

Fig 1 shows the PAL's block diagram. During the decoding process, the PAL acts as a finite-state machine, as **Fig 2** shows. Registers program its 10 outputs: A decoding register, which holds the secret code, determines eight of the outputs, and a state register determines the other two. There are four states: States 0, 1, and 2 are decoding states, during which three different decoding laws are applied; state 3 enables the PAL's outputs and the secret code.

At power on, the decoding and state registers are automatically reset, state 0 is selected, and the PAL's outputs are disabled. On every clock pulse, a program-decoding law uses a combination of input variables D_0 through D_{10} and previous-state variables Q_0 through Q_7 to determine the next state.

The detection of a programmed combination of D_0 through D_{10} and Q_0 through Q_7 causes a transition from state 0 to state 1. The transitions from states 1 to 2 and from 2 to 3 proceed in the same manner but in accordance with different decoding laws.

When the state register reaches state 3, it enables the PAL's outputs and releases the PAL's programmed secret-code contents from the decoding register to the output lines. The decoding laws may be data dependent (eg, $Q_{7\text{-}0}=D_{7\text{-}0}$ XOR $Q_{7\text{-}0}$), time dependent (eg, $Q=Q+1$), or both. The only restriction comes from the number of product terms available in the PAL.

Consider an example that uses the simple decoding laws shown in the **table**. The first decoding law is a function of input variables only, the second is a function of output variables only, and the third is a function of both. To reinforce protection, the internal Reset function is programmed to detect a trap combination and initialize the registers in the case of an incorrect

sequence of input variables. Other equations include

$$S_0 = \overline{S}_0\,\overline{S}_1\,ST_0 + S_0\,\overline{S}_1 + S_0\,S_1\,\overline{ST}_2,$$

$$S_1 = S_0\,ST_1 + S_1,$$

$$\text{OUTPUT ENABLE} = \overline{S}_0\,S_1,$$

and

$$\text{RESET} = 40_{16} \leq Q_0 \text{ TO } Q_7 \leq 4F_{16}.$$

Fig 3 shows the programming of the PAL with the logic equations listed in the **table**.

This example uses a double code—one real and one false—so that even if someone should enable the PAL's output by chance, he can't be sure that the code he reads is correct. The use of the double code also lets you reduce the number of terms needed for the state 1 to state 2 transition equation (see the state 0 equation).

Continued on pg 314

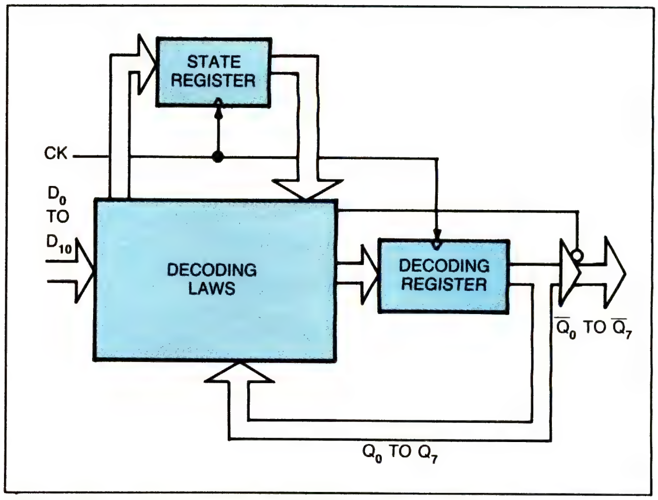

***Fig 2—By using an AmPAL22V10's state and decoding registers,** you can make the PAL into a finite-state machine that decodes sequential inputs.*

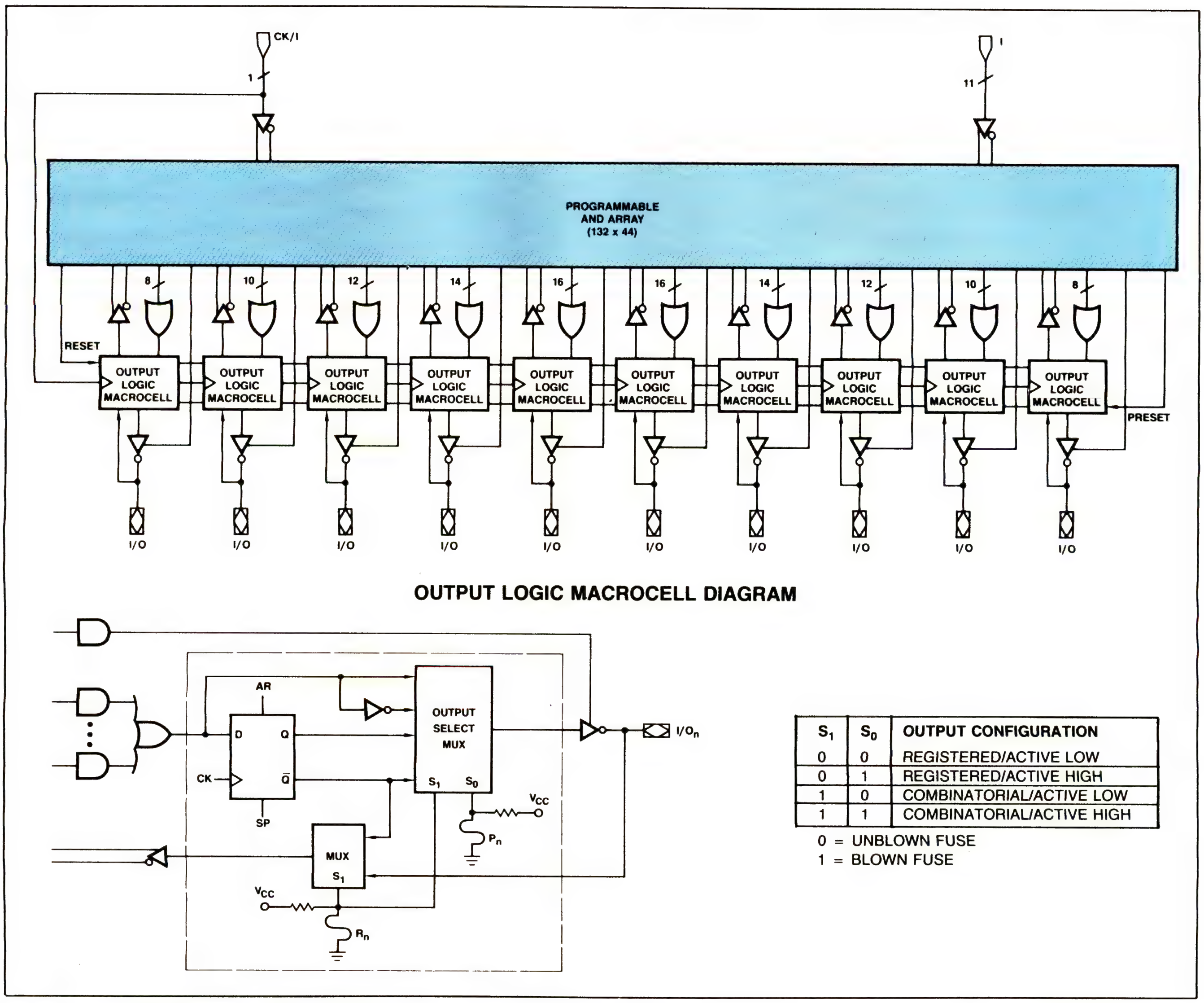

***Fig 1—An AmPAL22V10's ability to handle sum-of-products terms** via its programmable-AND array and its multiple inputs and outputs make it an ideal decoding tool to protect reserved and restricted-access systems.*

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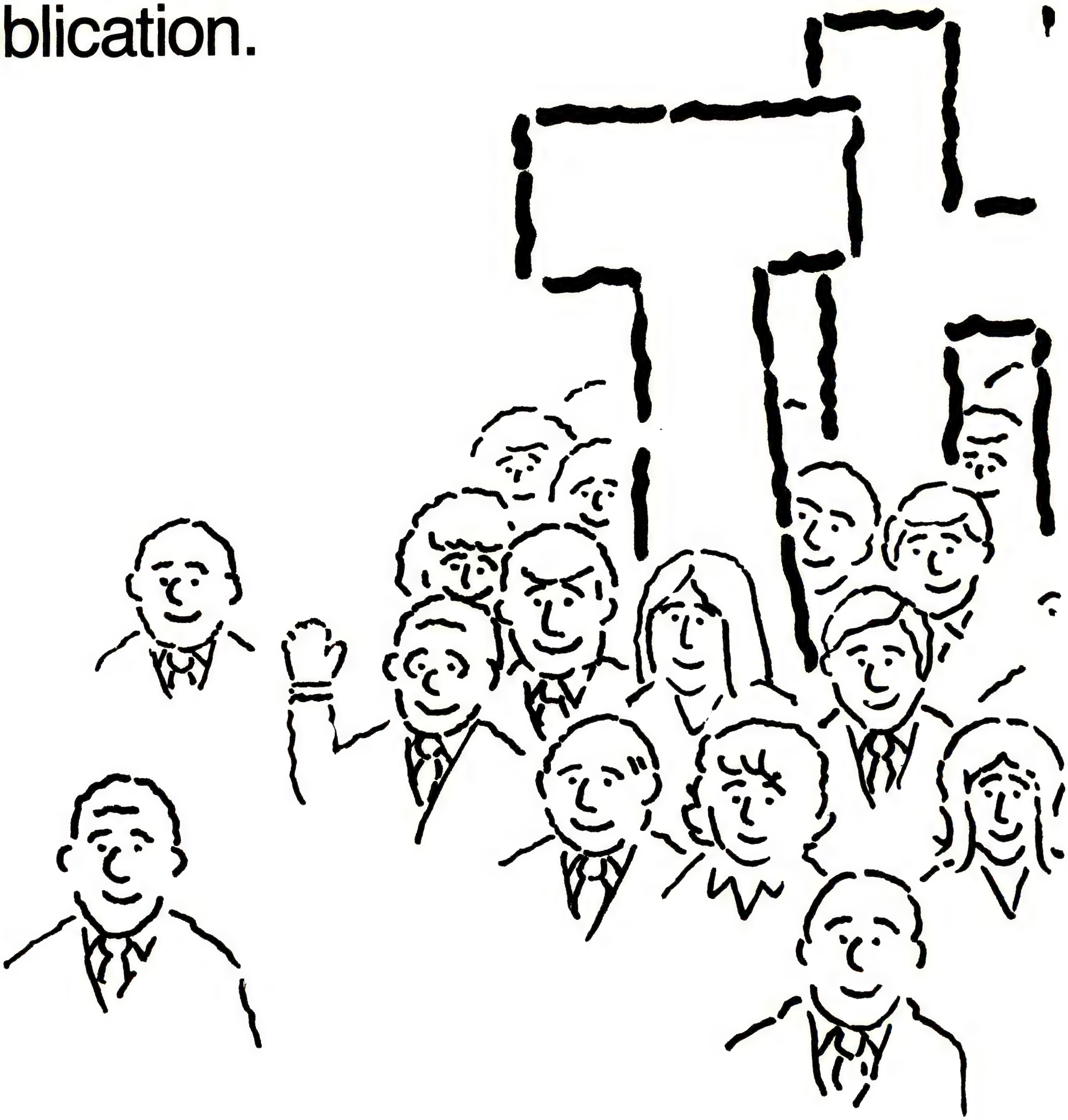

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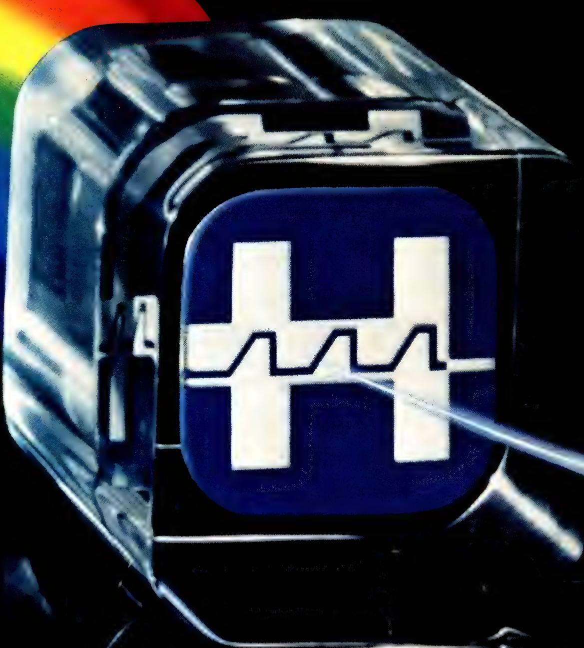

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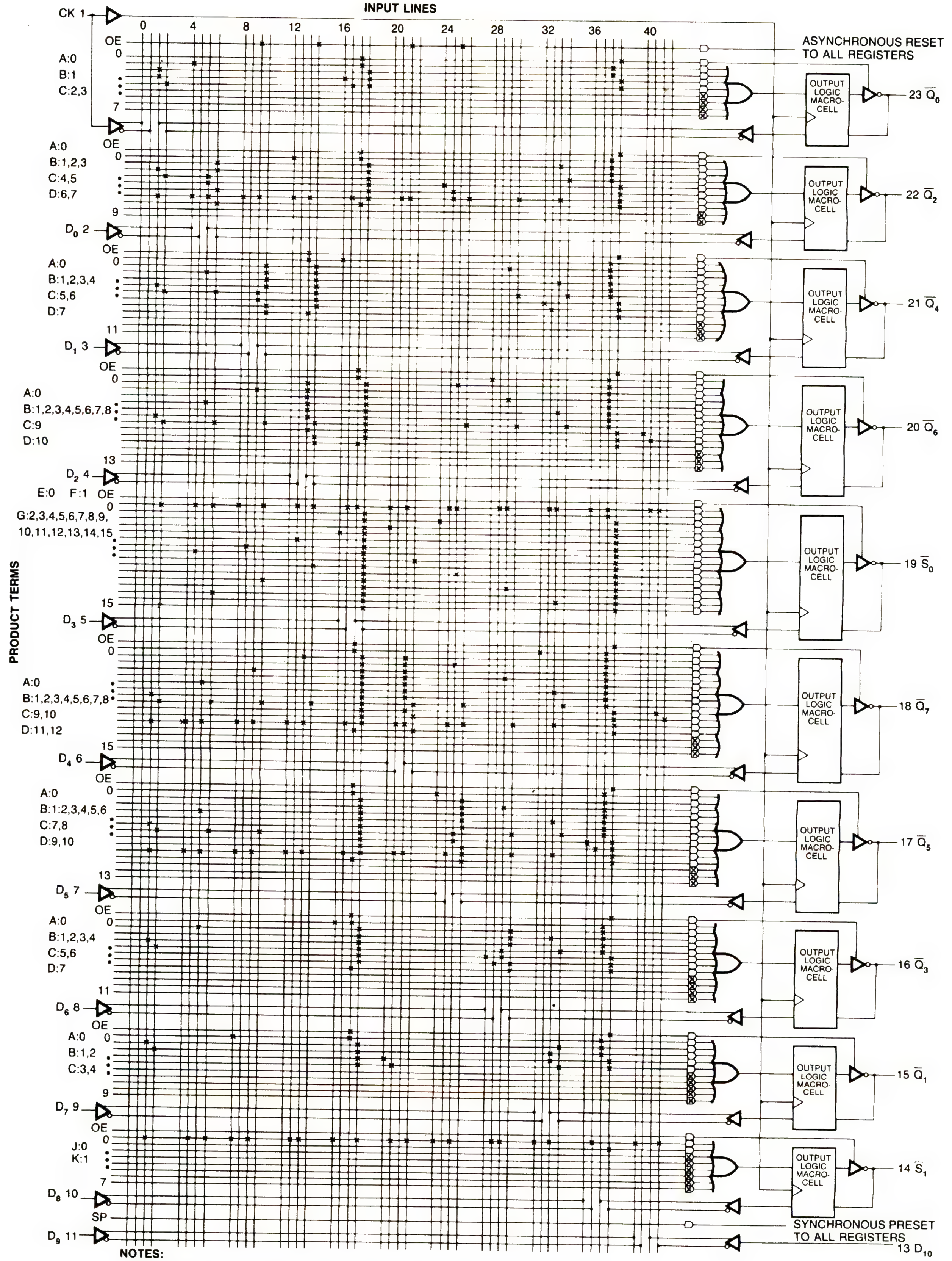

NOTES:
LINES MARKED 'A' REPRESENT THE LOGIC EQUATION OF THE FIRST DECODING LAW.
LINES MARKED 'B' REPRESENT THE LOGIC EQUATION OF THE SECOND DECODING LAW.
LINES MARKED 'C' REPRESENT THE LOGIC EQUATION OF THE THIRD DECODING LAW.
LINES MARKED 'D' REPRESENT THE LOGIC EQUATION OF THE REAL SECRET CODE.
LINES MARKED 'E' REPRESENT THE LOGIC EQUATION OF THE FALSE SECRET CODE.
LINES MARKED 'F', 'G', AND 'H' REPRESENT THE THREE TERMS OF THE S_0 LOGIC EQUATION.
LINES MARKED 'J' AND 'K' REPRESENT THE TWO TERMS OF THE S_1 LOGIC EQUATION.

Fig 3—This logic diagram *for an AmPAL22V10 device shows the practical implementation of the decoding laws listed in the* ***table.***

PAL DECODING LAWS

STATE	LOGIC EQUATIONS
0 $S_1 = 0$ $S_0 = 0$	CODING LAW: Q_0 TO Q_7 = D_0 TO D_{10} STATE TRANSITION (ST_0): D_0 TO D_{10} = 512_{16} Q_0 TO Q_7 = 55_{16}
1 $S_1 = 0$ $S_0 = 1$	CODING LAW: Q = Q + 1 (COUNTING) $Q = \overline{Q}_0$ $Q_1 = Q_1\overline{Q}_0 + \overline{Q}_1Q_0$ $Q_2 = Q_2\overline{Q}_1 + Q_2\overline{Q}_0 + \overline{Q}_2Q_1Q_0$ $Q_3 = Q_3\overline{Q}_2 + Q_3\overline{Q}_1 + Q_3\overline{Q}_0 + \overline{Q}_3Q_2Q_1Q_0$ $Q_4 = Q_4\overline{Q}_3 + Q_4\overline{Q}_2 + Q_4\overline{Q}_1 + Q_4\overline{Q}_0 + \overline{Q}_4Q_3Q_2Q_1Q_0$ $Q_5 = Q_5\overline{Q}_4 + Q_5\overline{Q}_3 + Q_5\overline{Q}_2 + Q_5\overline{Q}_1 + Q_5\overline{Q}_0 + \overline{Q}_5Q_4Q_3Q_2Q_1Q_0$ $Q_6 = Q_6\overline{Q}_5 + Q_6\overline{Q}_4 + Q_6\overline{Q}_3 + Q_6\overline{Q}_2 + Q_6\overline{Q}_1 + Q_6\overline{Q}_0 + \overline{Q}_6Q_5Q_4Q_3Q_2Q_1Q_0$ $Q_7 = Q_7\overline{Q}_6 + Q_7\overline{Q}_5 + Q_7\overline{Q}_4 + Q_7\overline{Q}_3 + Q_7\overline{Q}_2 + Q_7\overline{Q}_1 + Q_7\overline{Q}_0 + \overline{Q}_7Q_6Q_5Q_4Q_3Q_2Q_1$ STATE TRANSITION (ST_1): D_0 TO D_{10} = $2AA_{16}$ Q_0 TO Q_7 = 84_{16}
2 $S_1 = 1$ $S_0 = 1$	CODING LAW: $Q_I = D_J \oplus Q_I$, I = 0 TO 7, J = 3 TO 10 STATE TRANSITION (ST_2): D_6 TO D_{10} = DON'T CARE D_0 TO D_5 = 07_{16} Q_0 TO Q_7 = 28_{16}
STATE . . .	LOGIC EQUATIONS . . .
3	CODE VALUES: REAL CODE: Q_0 TO Q_7 = AC_{16} IF SC_2 TRUE AND D_6 TO D_{10} = 04_{16} FALSE CODE: Q_0 TO Q_7 IRRELEVANT IF SC_2 TRUE BUT D_6 TO $D_{10} \neq 04_{16}$

The maximum number is 16 product terms for the '22V10. Thus, the third term of the state zero equation can't exceed 14 product terms.

Once you've programmed the PAL and have blown the safety fuse, the PAL's resistance to fraudulent access is nearly perfect. Consider, for example, calculation of the number of cycles necessary to decode the PAL when you know the decoding laws.

For each state, the combination of D_0 through D_{10} and Q_0 through Q_7 gives 2^{19} possible values. Because the decoding laws for each state are independent of those for any other state, the total number of possible combinations is $2^{19}\times2^{19}\times2^{19}$ or 2^{57}. With a 50-nsec cycle time, it would take 203 years to decode the PAL—without taking into account the effect of a trap combination on the internal Reset. Now imagine trying to decode the PAL if you don't know the decoding laws.

You can expand the number of bits in the secret code: Just place similar PALs in parallel. Use the same decoding laws and state transitions but different code values. **EDN**

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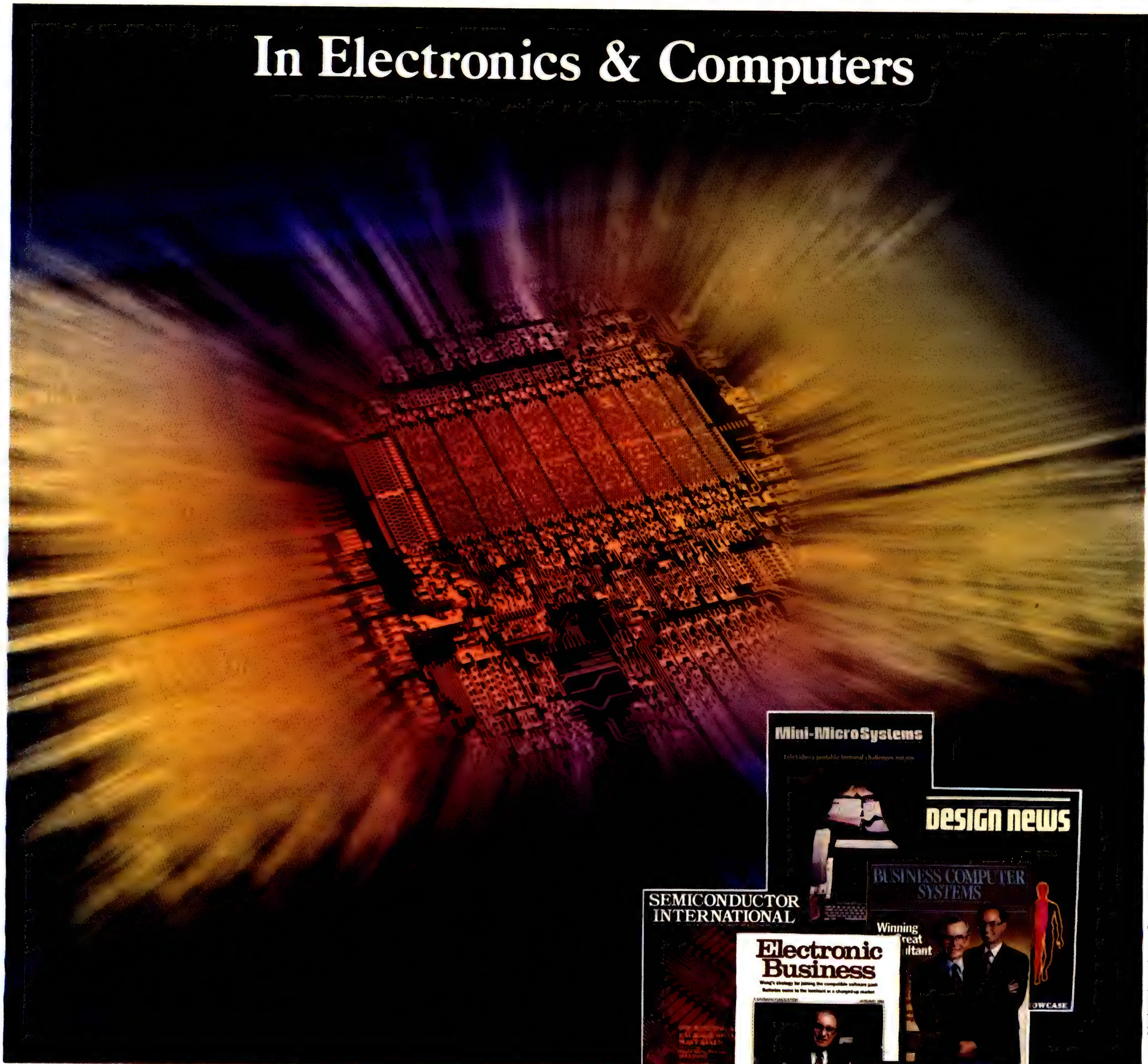

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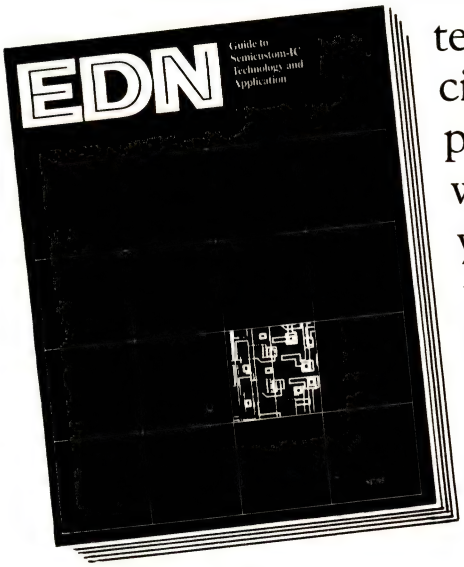

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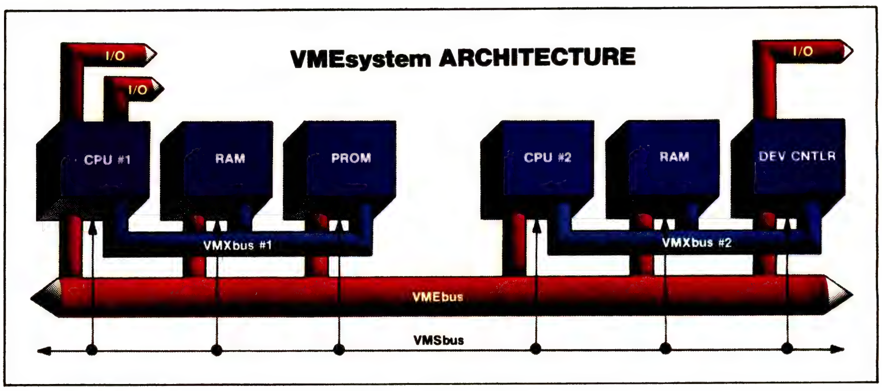

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Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (800) 426-1045; in WA, (206) 881-6444.

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MODELING LANGUAGE

Lasar Version 6 now includes optional packages for gate-array test generation and circuit-behavior modeling. Adlib performs mixed-mode simulation at levels ranging from device submodules to systems. This language is a 4-state simulator that propagates one, zero, 3-state, and unknown states through circuits. With the unknown-state handling ability, the simulator identifies uninitialized latches, registers, and other logical elements. Prosecutor automatically tests for CMOS, TTL, and ECL gate arrays, standard SSI/MSI parts, and fuse-programmable logic arrays. Its algorithm looks for paths that permit circuit node faults to propagate to primary outputs. The program also generates self-initializing input vectors that find critical paths, causing faults to express themselves at output pins. On Valid and Apollo workstations, Prosecutor starts at $5000; on the VAX 11-785, the program costs $50,000. Adlib is free to Lasar subscribers.

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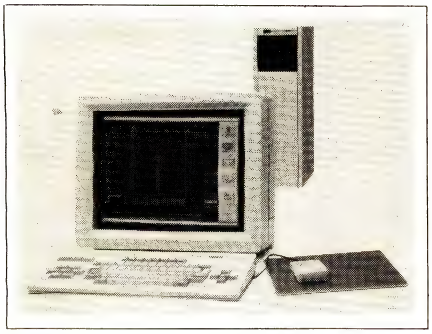

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These three CAE workstations aid in the design of pc boards. Based on a 32-bit internal architecture, the CDX-5000A includes 1.5M bytes of internal memory and a virtual-memory operating system. The software contains an object-oriented user interface, net-list input, automatic placement and routing, and a tooling and documentation package. For higher performance requirements, the CDX-50000 boasts a graphics accelerator, which makes 400,000 clip-and-transform operations/sec. Standard memory is 2M bytes. For complete electronic systems design, the CDX-59000 furnishes a 12-state logic simulator, a timing analyzer, and a waveform editor. CDX-5000A, $49,900; CDX-50000, $79,900; CDX-59000, $94,900.

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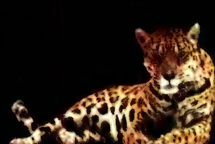

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WORKSTATION UPGRADE

These two hardware packages are upgrades for the company's workstations. The first package doubles the speed of the 700 Series workstations. It contains an improved CPU and disk controller. The second upgrade, the MS200, is a mass-storage subsystem that features one or two 420M-byte Winchester disk drives or one Winchester and one Cipher tape drive. Access times average 18 msec, and data-transfer rates spec at 1.86M bytes/sec. 420M-byte Winchester, $27,500; with Cipher drive, $35,000; 700 Series upgrade, $15,000.

Metheus-Computervision, Box 959, Hillsboro, OR 97123. Phone (503) 640-3311.

Circle No 529

BOARD LAYOUT

Running on either IBM PC-compatible machines or the NEC APC, FastWire lays out and routes pc boards and plots final artwork. Single- or double-sided boards have a maximum size of 163 in². The symbolic-graphics editor defines each board module functionally and physically. The layout program computes a wire-density map from a ranked wire list. A net-list compiler ranks files to optimize routing, and a re-entrant board-routing program supports manual, automatic, or semiautomatic wire routing. Manual editing capabilities include rip-up for rerouting, on-line checking of wire continuity, and additions or deletions in the wire list. Plots use the DM/PL protocol. $2500.

Pitch Instruments Inc, 19 Admiral Rd, Toronto, Ont, Canada M5R 2L4. Phone (416) 960-6122.

Circle No 530

UNIX™ MASTER

Single board UNIX™ — Battle Proven

Designed for maximum power at minimum cost, the HK68™ — UNIX™MASTER — is a proven leader providing Multibus™ users more space, more speed, and more flexibility to apply to difficult design problems.

Powerful and versatile, the Heurikon HK68™, sports 68000/68010 CPU (8Mhz or 10Mhz), quad channel DMA controller, MMU, 128K, up to 1M byte of dual access RAM with parity, up to 64K bytes of EPROM, four RS-232-C ports (optional RS-422 on one port), winchester I/F, streamer tape drive I/F, eight user definable LED's, four dipswitches, and two iSBX™ connectors for further I/O expansion — all on a single board. Other operating systems available include PolyFORTH™, CP/M-68K™, Regulus™, and VRTX™.

Make your tough decision an easy choice. Call Heurikon direct 1-800-356-9602, in Wisconsin 608-271-8700

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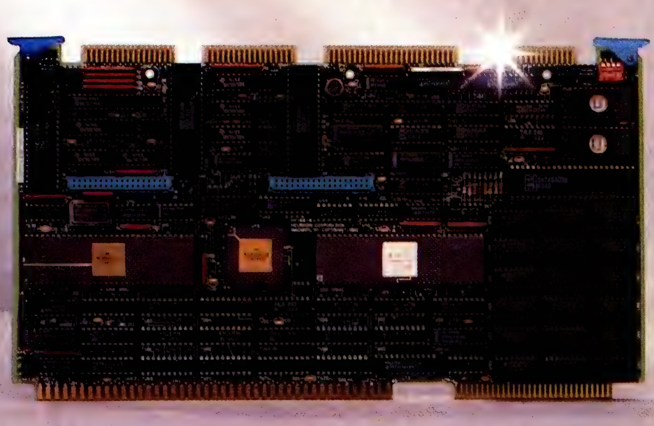

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In Wisconsin 608·271·8700
Telex 469532

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3201 Latham Dr., Madison, WI 53713

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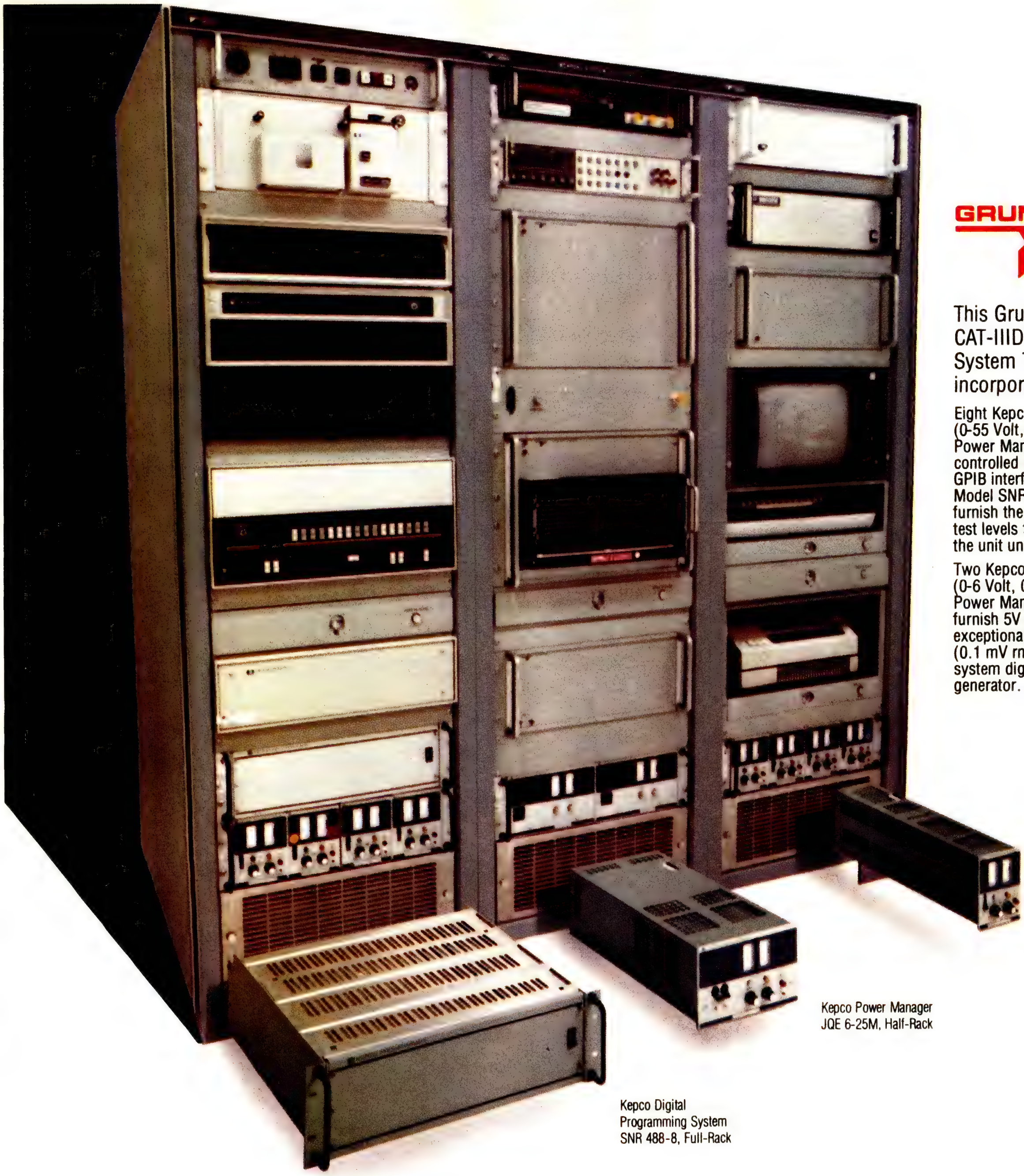

GRUMMAN

This Grumman CAT-IIID Weapons System Test Station, incorporates:

Eight Kepco ATE 55-1M (0-55 Volt, 0-1 Ampere) Power Managers controlled by an 8-channel GPIB interfacing a Model SNR 488-8, to furnish the programmable test levels that exercise the unit under test.

Two Kepco JQE 6-25M (0-6 Volt, 0-25 Ampere) Power Managers, to furnish 5V power at exceptionally low ripple (0.1 mV rms) to the system digital word generator.

Kepco Power Manager ATE 55-1M Quarter-Rack

Kepco Power Manager JQE 6-25M, Half-Rack

Kepco Digital Programming System SNR 488-8, Full-Rack

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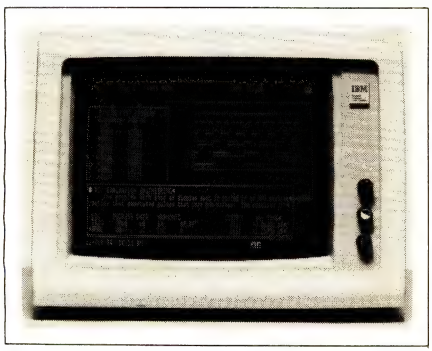
CIRCLE NO 200

SPEECH PROCESSOR

The Coretechs signal processor specifically performs speech processing for advanced speech recognition, speech compression, and resynthesis products. Packaged in an LSI CMOS, 68-contact leadless chip carrier, the Coretechs is capable of pitch-synchronous waveform analysis, is noise resistant, and yields strong acoustic cues for phonetic segmentation. The vendor claims that the processor provides speech that sounds natural and preserves the speaker's identity and inflection. The chip's encoding parameters include pitch track, segment duration, and the encoded waveform. The compression algorithms encode steady-state segments by specifying a variable number of repetitions. Transitional segments are encoded with more waveform detail and fewer repetitions. $30.

Scott Instruments Corp, 1111 Willow Springs Dr, Denton, TX 76205. Phone (817) 387-9514.

Circle No 531

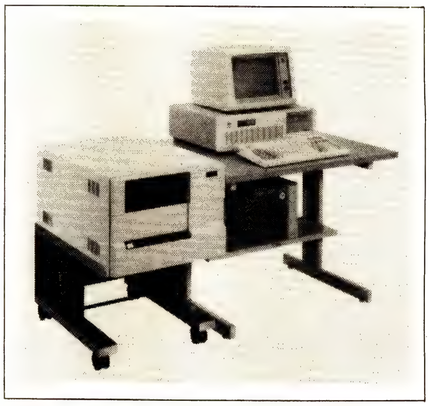


PC LOGIC ANALYST

The MicroAnalyst logic-analysis workstation consists of an i286-based IBM PC/AT, the manufacturer's Series 2000 logic analyzer, and a Lotus Symphony-based software package. The workstation integrates a state and timing analyzer with software for graphing, database sorting, documentation, terminal emulation, and spreadsheet operation. The combination of these five software functions allows you to perform logic-analyzer data analysis instead of merely acquiring raw data. You can use the database capability to filter the acquired data to your defined criteria. The graphics feature lets you define the manner in which the data relationships are displayed. The integrated communications facility lets you transfer your results to other computers. Options include a time-stamp module and an expanded line of disassemblers for 8-, 16-, and 32-bit microprocessors. $17,900.

Northwest Instrument Systems Inc, 15201 NW Greenbriar Parkway, Suite 140, Beaverton, OR 97006. Phone (503) 645-5151.

Circle No 532

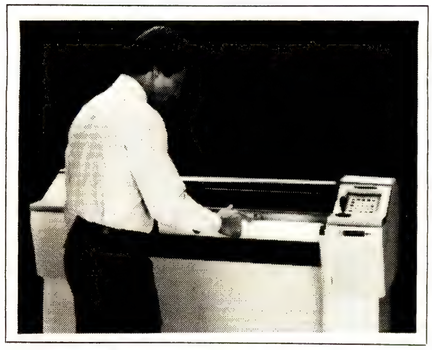


IBM PC 9-TRACK TAPE

In less than one hour, you can install a TDX-45 9-track-tape subsystem for use with your IBM PC/AT. This autothreading, dual-density 45-ips tape drive comes with a cabinet, cabling, an expansion board, and software. The software includes three drivers and three utility programs. The utility programs provide software for backup, verification, and restoration of the hard disk. Backup takes less than 10 min for the 20M-byte IBM PC/AT disk drive. You employ DOS commands to initiate disk copying; for more complicated data-processing tasks, you can control the tape drive directly from within any application program supported by DOS 2.0 or more recent versions. $6600.

Telebyte Technology Inc, 148 New York Ave, Halesite, NY 11743. Phone (516) 423-3232.

Circle No 533



DUAL-MODE PLOTTER

Model 1044 offers plotting capability to sizes as wide as ANSI size E or ISO size AO. The plotter operates in both cut-sheet and continuous-roll modes and allows you to produce single plots and batch jobs in production environments. Its 8-pen turret with automatic pen capping also provides automatic pen exchange over the plotting surface. This feature eliminates the delay in throughput caused by side-to-side returns for pen exchanges. The pen-turret design allows you to mix as many as eight colors and pen types, including liquid ball-point, nylon-tip, Ceramicron, and liquid-ink pens. The unit reads a bar code to determine pen type and automatically adjusts to the appropriate height, force, and velocity for each individual pen. You can program and store as many as four sets of setup parameters in the unit's nonvolatile RAM, including communications mode, baud rate, pen velocity/acceleration, scaling, rotation, and log-on messages via the unit's 40-character display. Built-in self-diagnostics run five tests every time the plotter is turned on. The 1044 provides a resolution of 0.001 in. and a plot speed of 14 ips with an acceleration of 1g. $11,995.

CalComp, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (714) 821-2142.

Circle No 534

LASER PRINTER

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Telephone: (305) 823-5440

Security Plastics In

CIRCLE NO 129

ing in a clustered work environment. The vendor claims that this laser printer is as much as 10 times faster than daisy-wheel printers and quiet enough to preclude the need for a sound enclosure. The LaserRight's cluster controller allows simultaneous and transparent access to the printer by more than one computer. The unit comes with 128k bytes of buffer memory (expandable to 512k bytes) for interleaving individual print jobs. It also features automatic self-testing and 59k bytes of raster graphics memory. The LaserRight prints 8 pgs/min on regular bond paper, which can be loaded through the unit's slide-in tray or manually fed one sheet at a time. You can print with multiple character fonts on the same page. $4495.

Extended Systems, Box 4937, Boise, ID 83711. Phone (208) 322-7163. TLX 590892.

Circle No 535

VIDEO GRAPHICS

The Video Production System allows you to overlay and integrate graphics generated by the manufacturer's computer with any standard external video-output signal. The module houses a genlocking circuit that gives video-production specialists a method for combining computer graphics with video sources for viewing on a single display. The genlocking circuit uses two proprietary VLSI graphics coprocessors and an Intel 80186 μP, and it uses a fast analog switch to select a signal source. Each pixel on the video screen is selectable for use by a key-bit selector inside the display processor. You can choose 640×400-pixel, 2-color interlaced resolution or 320×200-pixel, 16-color noninterlaced resolution. The system software includes a 512-color paint package; 11 fonts that you can customize with colors, angles, and drop shadows; a real-time animation program; a design-creation package; a synthesized monaural or stereo audio output; and a business-presentation package. $3799.

Mindset Corp, 617 N Mary, Sunnyvale, CA 94086. Phone (408) 737-8555.

Circle No 536

TERMINAL SERVER

The Ethernet-based CS/1 terminal server implements the TCP/IP (Transmission Control Protocol and Internet Protocol), which have been standardized by the Department of

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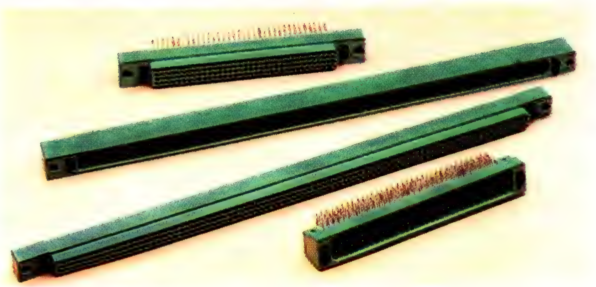

conventional pin and socket contacts, which minimizes the risk of connector or PC board damage during mating or unmating.

B³ contacts are made of multiple strands of high tensile strength wire that are bundled together to form a brush-like contact. Intermeshing two of these multi-strand wire bundles forms a gas tight connection with superior electrical characteristics including redundant current paths, minimal constrictive resistance and uniform current densities. B³ contacts maintain their electrical stability over 20,000 mating and unmating cycles.

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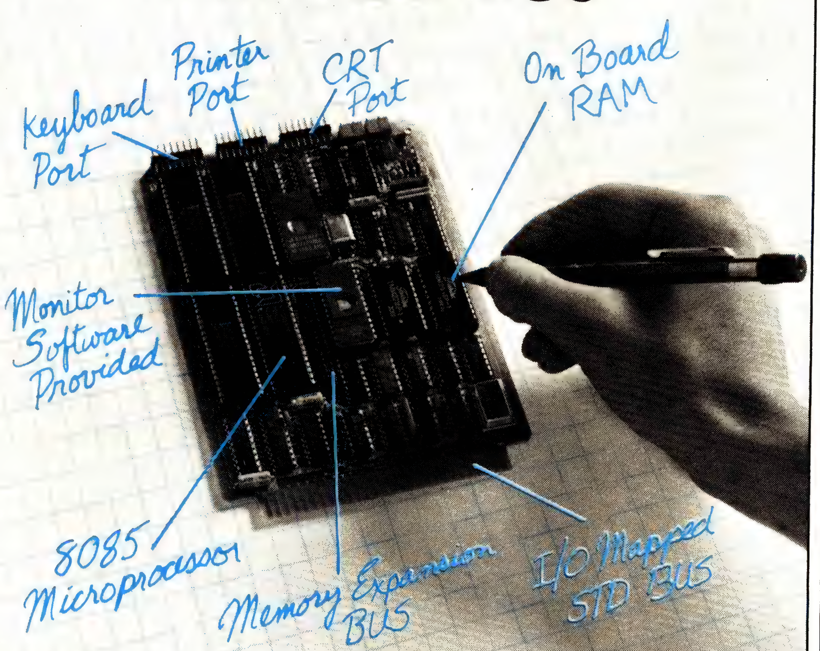
CIRCLE NO 156

Defense and are an integral part of the Unix 4.2 BSD operating system. With TCP/IP software, the CS/1 server functions as a terminal server or host server, allowing as many as 32 asynchronous devices to access host computers that support TCP/IP and are attached to an Ethernet LAN. The TCP/IP are higher level protocols (OSI model layers 3 through 5) that provide network and transport services above the physical and data link protocols defined by the Ethernet specification. The system uses a standard Telnet protocol to support virtual circuits among terminals and host computers. Also implemented on the CS/1 unit are the DoD Universal Datagram Protocol (UDP) and the Ethernet Address Resolution Protocol (ARP). The system's interface- and network-management services include usage statistics and Ethernet and server performance statistics. From $9900. Delivery, 60 days ARO.

Bridge Communications Inc, 1345 Shorebird Way, Mountain View, CA 94043. Phone (415) 969-4400. TLX 176544.

Circle No 537

SMART CRT CONTROLLER ON STD BUS



Cubit's new I/O Processor controls a CRT, printer and keyboard.

Using an 8085 microprocessor with its own memory, the board frees your system CPU to race ahead of slower peripherals. Terminal-like commands permit easy communication between this smart controller and the host-processor.

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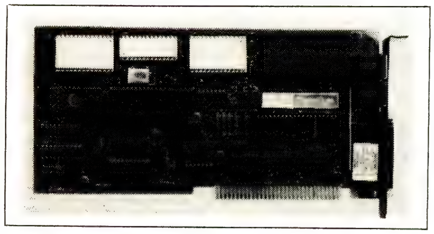

MODEM BOARD

The MOD-MB is an intelligent modem for the IBM PC and compatible computers. The board plugs into any of the computer's expansion slots and connects to your telephone line with the cable provided. It's Bell 212A and 103 compatible and features autodial and autoanswer capabilities and 14 other serial commands. You can program the modem's autodialer to dial either voice or data calls. If the number is busy, the unit can redial the same number or an alternate number. The board automatically selects DTMF or rotary pulse dialing. An auxiliary RS-232C port is a standard feature that can be used whether the modem is in operation or not. The MOD-MB comes with software, telephone cable, and a manual. $345.

MetraByte Corp, 254 Tosca Dr, Stoughton, MA 02072. Phone (617) 344-1990.

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HARD-DISK DRIVE

The Superior Interior provides 20M bytes of internally mounted hard-

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disk storage for your IBM PC. This half-height drive mounts in the second drive position of your PC and handles floppy and hard disks. The unit has a soft-start motor with a filtering system to reduce electronic noise. The data-transfer rate is 5M bps, and average access time is 3 msec. The unit comes with a controller card, configuration software, and documentation. $2195.

Percom Data Corp, 11220 Pagemill Rd, Dallas, TX 75243. Phone (214) 340-5800.

Circle No 539

MULTITASKING μC

The MC-186 dual-processor system provides your 8-bit stand-alone CP/M-based computer with multiuser and multitasking capabilities while protecting your existing hardware and software investments. The MC-186 operates under Multiuser Concurrent DOS (MC-DOS), which is based on Digital Research's Concurrent DOS with expansion and security enhancements. With this system, you can run as many as four programs concurrently on as many as eight workstations. Optional network-controller boards link the MC-186 with other systems and workstations in an ARCnet-compatible local-area network operating under Digital Research's DR Net. The unit has 80186 and Z80H CPUs for 8- and 16-bit multitasking. A standard configuration of the MC-186 includes a 23M-byte Winchester disk drive, 10 serial ports, one parallel port, a dual-density DMA floppy-disk-drive controller, one 1.2M-byte floppy-disk drive, the MC-DOS operating system, and applications software. $12,500.

Gifford Computer Systems, 2446 Verna Ct, San Leandro, CA 94577. Phone (415) 895-0798. TLX 704521.

Circle No 540

MODEM DIAGNOSTICS

The MDTS (Modem Diagnostic Test System) gives any modem the ability to provide automatic digital and variable-frequency alarms, modem

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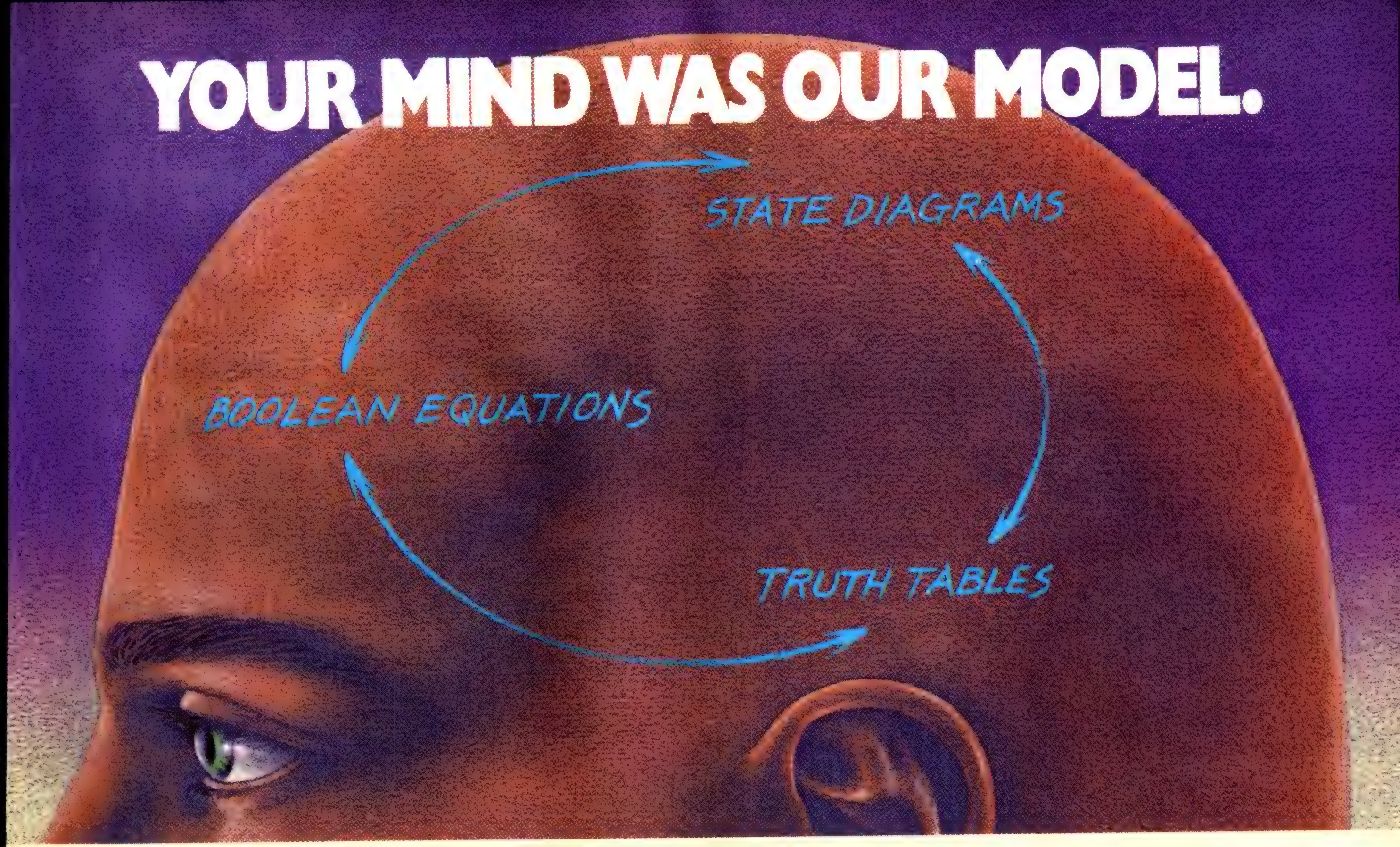
YOUR MIND WAS OUR MODEL.



ABEL™ lets you design programmable logic in the ways you think.

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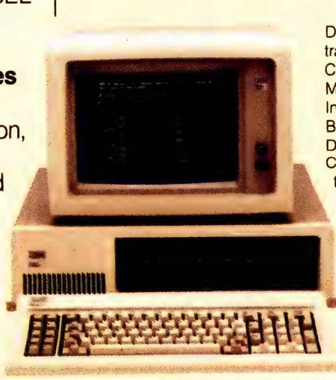
Order ABEL and start designing logic the way you think. Allow 4 weeks for delivery.



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Data I/O Corporation, 10525 Willows Road N.E., P.O. Box 97046, Redmond, WA 98073-9746. For immediate action, contact us directly, **CALL TOLL FREE:** 1-800-426-1045. In Washington, Alaska and Hawaii, call 206-881-6444. Europe: Vondelstraat 50-52, 1054 GE, Amsterdam, The Netherlands, Tel: (20) 186855. Germany GmbH: Bahnhofstrasse 3, D-6453 Seligenstadt, West Germany, Tel: (6182) 3088. Japan: Ginza Orient Building 6-F, 8-9-13, Ginza Chuo-ku, Tokyo 104, Japan, Tel: (03) 574-0211.

DATA I/O

CIRCLE NO 160

and terminal status checking, and remote testing. An automatic disconnect feature controls a streaming modem or terminal. This IBM PC-controlled network-management system masks your existing data network, giving you central-console control over WRB/1 modem wrap-around boxes, which perform interruptive tests on the network. The MDTS maintains a system database that contains information on circuits and drops in the communication system, and it monitors the operation of the network modems and maintains a record of alarm conditions. You can selectively enable or disable each monitor function, set high and low limits for alarm processing, and check the current state of each monitored point. A total of 14 signals are included in the monitoring function. MDTS tests include digital and analog loop backs, bit-error-rate tests, polling tests, analog level measurements, and self-tests. From $3990.

Digilog Network Control Div, 1370 Welsh Rd, Montgomeryville, PA 18936. Phone (215) 628-4530.

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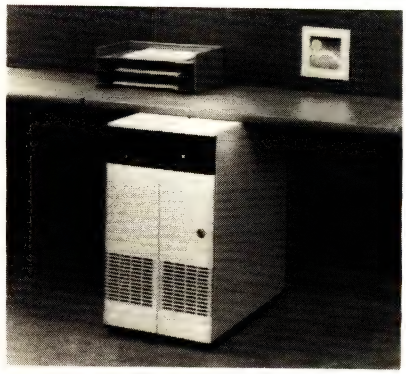

SUPERMINICOMPUTER

Using an enhanced version of AT&T's Unix V operating system (Centix) and sporting an integrated relational database system, the XE 550 provides mainframe power in a superminicomputer. Based on the 68010 and the Intel 186 μPs, the XE 550 distributes the workload over multiple functional processors, each of which has its own memory and can support applications, files, or communications. To maximize system performance, the CPU assigns each task to the processor most suited to that particular task. The 32-bit application processors run programs under Centix. There is also a file processor, a storage processor, a terminal processor, and a cluster processor. The system supports as many as 16 terminals; it has a Centronics-compatible parallel printer port and three RS-232C ports for datacomm services. The entry-level system configuration includes 2.5M bytes of memory and a 75M-byte hard disk. From $43,300.

Burroughs Corp, 6071 Second Ave, Detroit, MI 48232. Phone (313) 972-7000.

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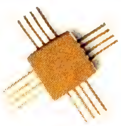

Shift registers, binary counters, and now, logic elements! Harris Microwave Semiconductor can now supply production quantities of SSI logic elements with 3.5 GHz clock speeds.

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For your information our name is Harris.

More information on Harris Microwave Semiconductor on page 394

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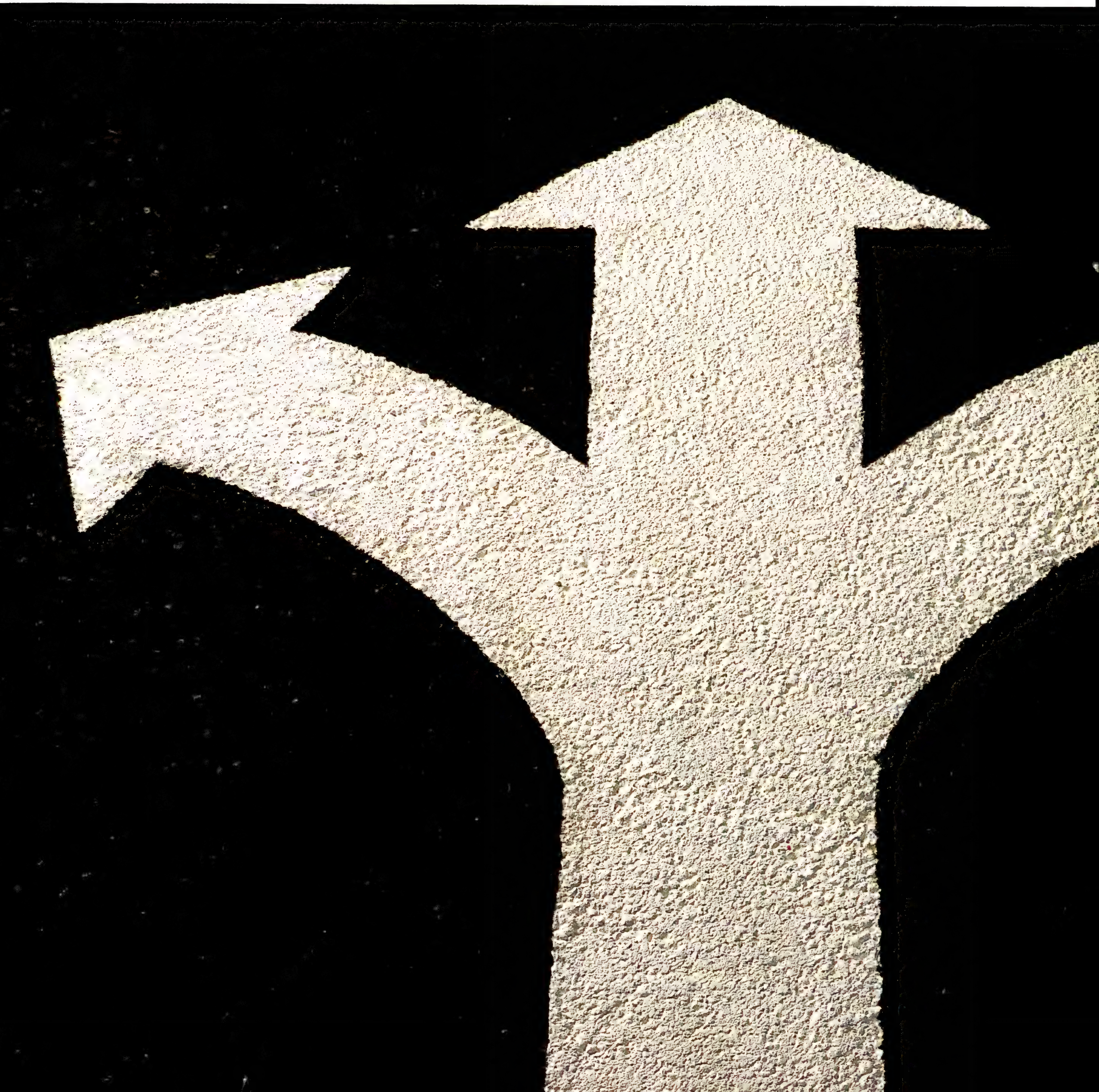

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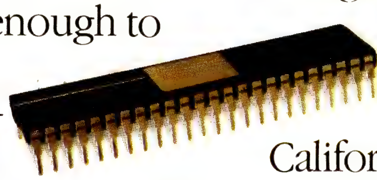
Whether it's a 10Mbps Ethernet LAN system for linking high-performance graphics workstations to minicomputers. Or a 2 Mbps LAN that links personal computers in a department.

Networking needs are as diverse as city streets and eight-lane highways. So it's a turn for the better that office LAN standards are emerging: IEEE 802.3/Ethernet, Cheapernet and IBM* PC Network.

And even though all three networks are different, they have one thing in common:

Intel's 82586 LAN Coprocessor, the only programmable LAN chip.

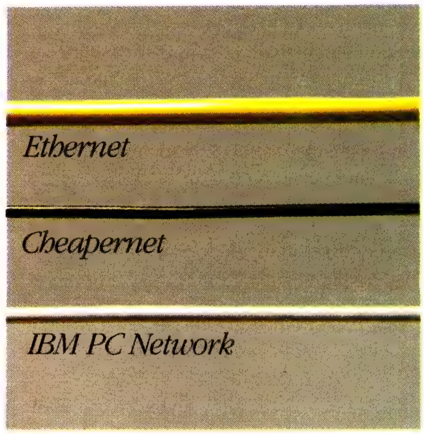
Because it's programmable, you have the flexibility to implement any of these office networks. With the 82586, you won't have to relearn a new chip every time the market takes a turn. You choose the office network and the 82586 is flexible enough to support it.



In addition to its unique programmable features, the 82586 eases your LAN design effort.

Its high level command interface performs datalink functions which means there's no low level software to write.

The 82586's diagnostic features such as loopback and self test,



make it easy to debug your system during development.

And the 82586 is designed to work with Intel's highly integrated microprocessors like the 8-bit 80188 and the 16-bit 80186. So you can keep your chip count down, which saves time and eases your design effort.

Find out more about the 82586 and how Intel can support your LAN design efforts. For our free brochure, call toll free: (800) 538-1876. In California, (800) 672-1833. Or write Intel Corporation, Lit. Dept. W-41, 3065 Bowers Ave., Santa Clara, CA 95051.

Because whichever network you need, there's only one way to turn:

Intel.

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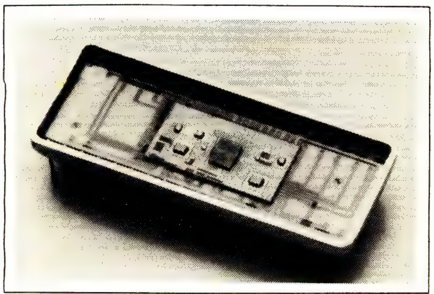
CIRCLE NO 163

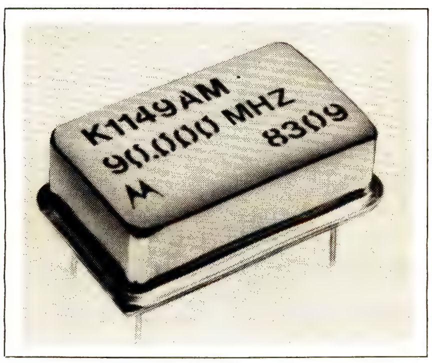


MULTIPLYING DAC

Featuring angular and radius accuracies of 1 arc min and 0.03%, respectively, the HDSC2026 is a 4-quadrant multiplying DAC with μP compatibility. It accepts a 16-bit digital input (CMOS/TTL) and multiplies it by an analog voltage to generate the trigonometric functions V_{IN} $\sin\theta$ and V_{IN} $\cos\theta$. The analog voltage can be an ac or dc reference with an amplitude of ±10V pk. The analog input is buffered through an operational amplifier to minimize loading of the input signal. Housed in a standard DIP, the converter requires only ±15V power supplies. From $245. Delivery, stock to 6 wks.

Natel Engineering Co Inc, 4550 Runway St, Simi Valley, CA 93063. Phone (805) 581-3950. TWX 910-494-1959.

Circle No 543

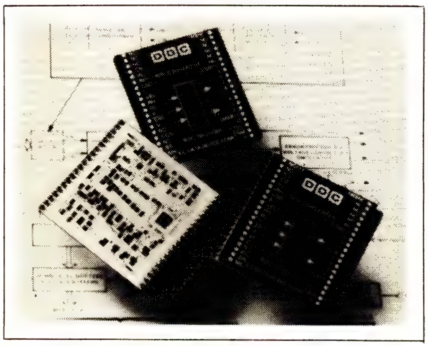


CRYSTAL OSCILLATOR

The ECL-compatible K1149AM crystal clock oscillator drives high-speed logic devices like the MECL 10K and 10KH logic families. The oscillator features a frequency range from 60 to 90 MHz with a stability of ±100 ppm. Rise and fall times are rated at 1.0 nsec typ, 2.0 nsec max. Typical I_{EE} supply current is 30 mA from a supply voltage of −5V dc ±5%. The K1149AM can withstand wave soldering operations without damage; insulated standoffs permit proper defluxing. It can also be plugged into a standard DIP socket, taking up only 0.820×0.520 in. on a circuit board. Its seated height of 0.270 in. lets you use standard logic boards without losing spacing. $85 (10). Delivery, 8 wks (prototypes).

Motorola Inc, Components Div, 2553 N Edgington St, Franklin Park, IL 60131. Phone (312) 451-1000. TLX 4990104.

Circle No 544



R/D CONVERTERS

RDC-19190 Series resolver-to-digital converters provide a velocity output with 1% linearity, which eliminates the need for bulky, costly electromechanical tachometers in control systems. Converters are available in 10-, 12-, 14-, and 16-bit resolution with accuracies of ±21, ±8.5, ±2.6, and ±1.3 min, respectively. Input frequency ranges for the various models are 360 Hz to 22 kHz, 600 Hz to 22 kHz, 1 to 3.5 kHz, and 360 Hz to 3.5 kHz. Resolver or direct inputs at 11.8V and 2.0V line-to-line are available. All units operate with a reference-voltage range of 4 to 50V. Maximum tracking rates range from 400 to 6.3 rps for 10- to 16-bit converters, respectively. From $133. Delivery, 4 to 8 wks.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 545

MEMBRANE SWITCH

This transparent membrane switch can be used for either linear or matrix switching or both. It uses a deposition of indium tin oxide and is available with a wide range of resistivity and light transmission. It is designed to be placed directly over CRT, LED, plasma, or backlit panels. When the switch is utilized as an analog switch, in conjunction with external circuitry, you can obtain almost infinite resolution and control depending on where you touch the membrane switch along its x and y axes. The switch is sealed against moisture and has been tested for over one million actuations. It can be manufactured to meet various military specs for ground support and airborne applications. The switch operates over −30 to +75°C typ and can operate in altitudes as high as 15,000 ft; optional vented units can operate in even higher altitudes. $55 to $500. Delivery, 10 to 12 wks.

CAM Graphics Co Inc, 145 Toledo St, Farmingdale, NY 11735. Phone (516) 694-1315.

Circle No 546

LED DISPLAY

The PD-2816, an intelligent, programmable alphanumeric display, is an end-stackable, 8-character, 18-segment device that offers built-in interface circuitry. It's compatible with an 8- or 16-bit μP. A control register is accessible through the data bus instead of external pins and is used to activate the device's software-controlled functions. Functions include a 3-level brightness control, blanking and highlight capabilities, intercharacter blink-

Continued on pg 342

Custom and Semicustom Solutions

Solutions that come from a VAX computer system and various CAE workstations.

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CIRCLE NO 164

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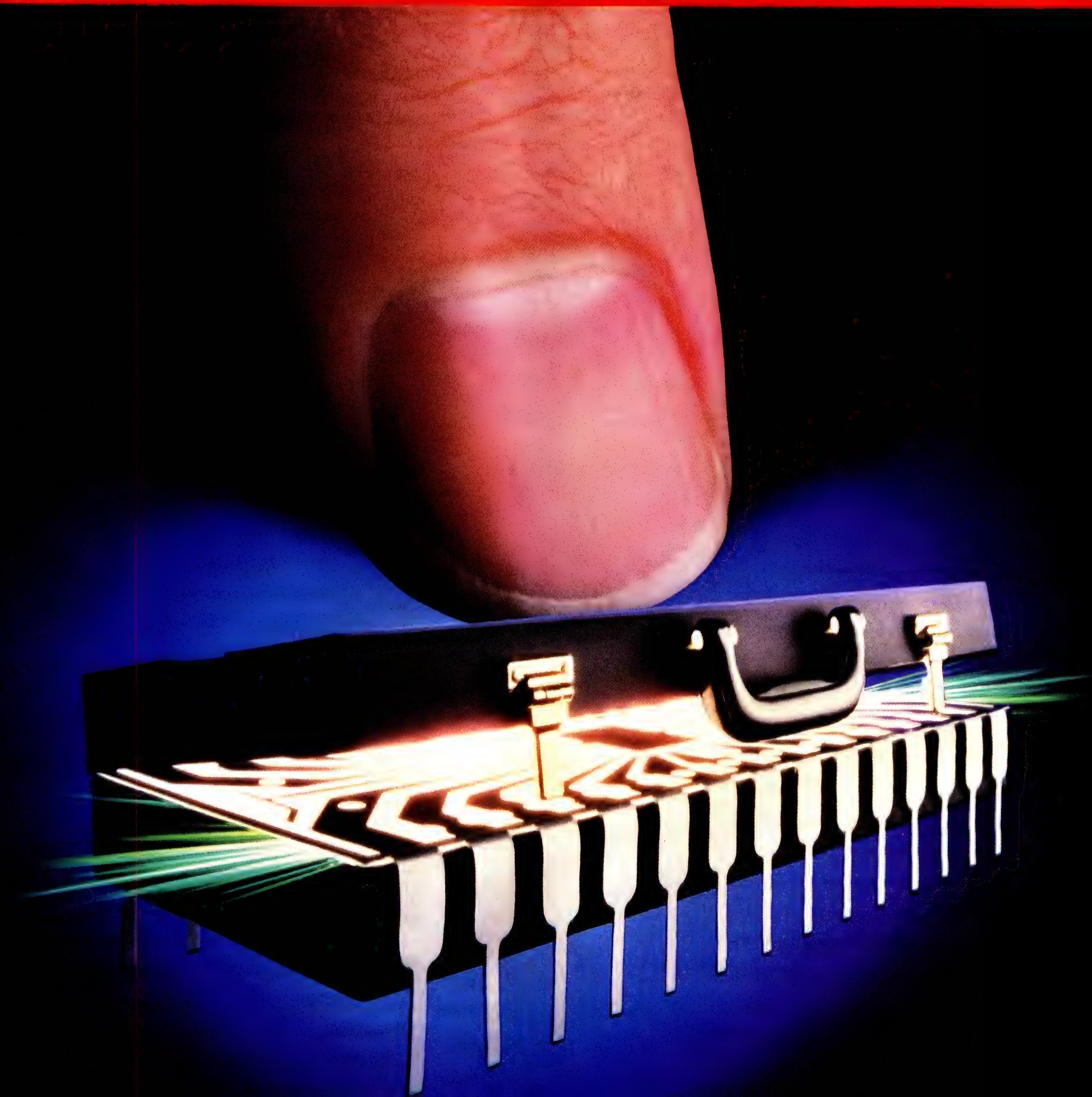
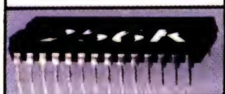
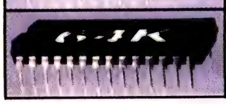
We pack CMOS ROMs so densely something gets squeezed:



...the price.

	Part Number	Organization	Access Time (ns)	Operating Current (mA)	Standby Current (μA)	JEDEC Package	100K Price
	CDM53256*	32Kx8	250	12	50	28 pin Type B	$4.20
	CDM53128	16Kx8	250	10	50	28 pin Type B	$2.50
	CDM5364	8Kx8	250	12	50	24 pin	$1.95
	CDM5365	8Kx8	250	12	50	28 pin Type B	$1.95

*Available first quarter 1985. Patterns accepted 12/84.

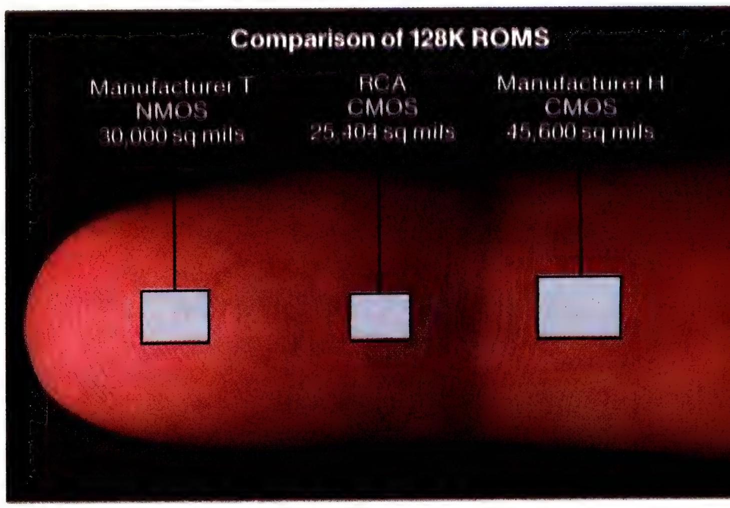
Now, CMOS ROMs at NMOS prices. RCA has broken the price barrier. For the first time, you can buy CMOS ROMs from RCA for the same price as NMOS ROMs.

Our new space-efficient chip cuts manufacturing cost. Using a new and smaller space-efficient silicon chip, RCA has made CMOS ROMs the same size as most NMOS ROMs—even smaller than many. We shrank geometries down to 3μ and arranged memory cells in a NAND-stack configuration that uses the small space more efficiently. Our costs go down, so your price goes down.

Faster than NMOS, too. At a maximum access time of 250 ns, RCA ROMs are even faster than many NMOS types. Cheaper and faster? Well, you'd expect the breakthrough in CMOS ROMs to come from the inventors of CMOS.

Pin-for-pin compatibility. RCA ROMs feature the same pinouts as competitive NMOS and CMOS ROMs or PROMs. They are input and output compatible with CMOS or TTL logic. So now it's easy to give your existing design the advantages of CMOS technology...lower power consumption, wider temperature range, etc.

Pack your pattern to your RCA sales office today. Squeeze your ROMs, before your competition squeezes you. To put CMOS advantages in your design, call your local RCA sales office for a price quote today. For technical brochures and ordering information **call toll-free 800-526-2177.**



If you would like an RCA salesperson to call on you with detailed information on price, delivery and technical considerations, please send this coupon to: RCA Solid State, Box 2900, Somerville, NJ 08876.

End product application: ______________________

What size ROM required? ______________________

Name: ______________________

Title: ______________ Phone: ______________

Company: ______________________

Address: ______________________

Call: Hamburg, 49-4106-6130; London, 44-03-2785511; Paris, 33-3-946-5656; Hong Kong, 8-52-3-723-6339; Sao Paulo, 55-11-210-4033.

Changing to serve you better.

RCA

CIRCLE NO 165

ing, character underline, and a lamp test that will turn on all segments at half brightness without disturbing the internal character memory. The display is controlled by a built-in CMOS IC that contains control and display read/write memory, an ASCII-character generator (ROM), multiplexing circuitry, segment and character drivers, and bus-control circuitry. Data access is asynchronous and can be random. Each display character is directly addressable and includes a Highlight Attribute control bit. The display requires a 5V supply, is TTL compatible, and draws a maximum of 250 mA when all eight characters are on. $32.95 (1000).

Siemens Components Inc, Optoelectronics Div, 19000 Homestead Rd, Cupertino, CA 95014. Phone (408) 257-7910.

Circle No 547

3220 Series

ATTENUATORS

These latching devices are available with attenuation ranges of 0 to 127 dB in 1-dB steps, 0 to 120 dB in 10-dB steps, and 0 to 31 dB in 1-dB steps. All units have a nominal impedance of 50Ω and operate from dc to 2.0 GHz with high linearity. Input and output ports use precision miniature female connectors that mate with SMA male connectors. The programmable latching attenuators are available in 5- or 8-cell units. Repeatability is ±0.001 dB per cell. Switch life is rated at >10 operations per cell, and switching time is 1.5 msec max. With no continuous power drain through the relay coils, a typical 8-cell latching unit runs cooler than a nonlatching device because power dissipation can be up to 3W less for latching units than for nonlatching units, which results in improved stability and contact repeatability. The units are rugged and compact and meet many of the environmental requirements of MIL-A-3933. $850 (8-cell); $625 (5-cell). Delivery, 60 to 120 days.

Weinschel Engineering, *One* Weinschel Lane, Gaithersburg, MD 20877. Phone (800) 638-2048; in MD, (301) 948-3434.

Circle No 548

FILTER

The R5635 modem filter contains two channels of bandpass filters in a 16-pin DIP and is fabricated using an industry-standard double-poly NMOS process. The bandpass filters are centered at 00 Hz (lowband) and 2400 Hz (highband). On-chip MUX switches and a TTL-compatible input pin switch the filters between the transmit and receive modes. Included on the chip is a select pin for switching the 550-Hz guard-tone notch filter, a TTL-compatible input pin for self-test mode, and lowpass clock filters in the transmit and receive paths. The modem filters are self-contained and require only positive and negative supplies and an external TTL (or CMOS) 153.6-kHz input clock to operate. $15 (OEM qty).

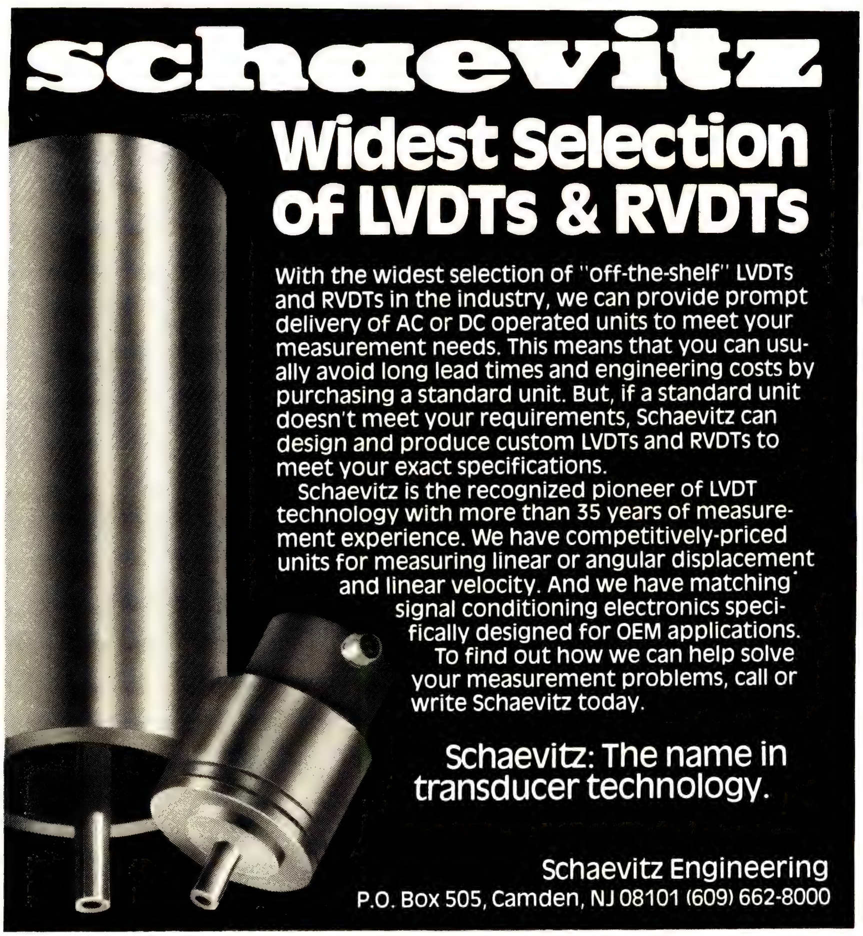
EG&G Reticon, 345 Potrero Ave, Sunnyvale, CA 94086. Phone (408) 738-4266. TWX 910-339-9343.

Circle No 549

VIDEO AMPLIFIER

The VA-120, a 120-MHz video amplifier, provides a 40V p-p output signal with a 2.9-nsec rise and fall

Continued on pg 346



CIRCLE NO 166

Introducing Unitest: Powerful Menu-Driven Software that Simplifies Your Instrument Control Programming Using HP 9000 Series 200 Computers.

Programming HP IEEE-488 (HP-IB) instruments just got a lot easier thanks to our powerful software development package: Unitest. Unitest eliminates the need to understand HP instrument programming protocols. The result: fewer man-hours needed to develop and debug a measurement intensive program.

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Priced at $99 (which is fully deductible from your order when placed within ninety days), the demo package comes complete with Unitest manual and demo software disks. Act today and discover the joy of having the right tools for the job. Unitest.

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CIRCLE NO 168

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The Innovator in Clad

And what makes TMI so unique?
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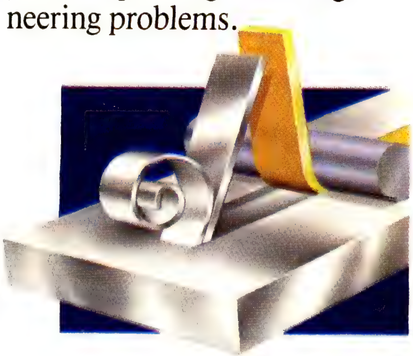
Pioneers Of Specialty Materials Systems

TMI shares your commitment. We are at the leading edge of clad metals technology for electrical and electronic applications. And our innovations will provide you with reliable, cost-effective solutions to your tough design and engineering problems.



We're The Experts In Clad Metals

Our superior metallurgical engineering staff puts us in a unique position to improve your cost-performance. We'll work closely with you to dramatically reduce product costs and improve quality. The benefits of this person-to-person association are many.

TMI Is A Cost-Effective Alternative

TMI can help you do your job more effectively. We will consult, quote, produce, and ship—based on your needs.

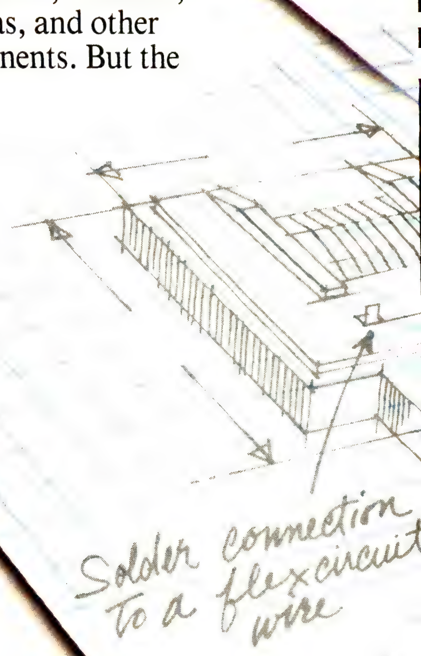
TMI's advanced technologies allow us to precisely control the location and dimensions of the precious metal areas. Therefore, our processes help eliminate precious metal waste and save money. We have available special alloys, such as TMI 305 (diffused gold/palladium silver), as alternatives to the standard 24 Kt. gold. Numerous other contact materials are also available to meet your demands on material performance.

And TMI's cladding technologies help reduce labor costs because there are fewer manufacturing steps from stamping to assembly. Yet the quality of the end product is superior.

Increase Your Flexibility

By using TMI's advanced clad metals technology, you are able to design components with optimum efficiency and economy. Your flexibility as a designer allows you to use our technologies in many diverse electrical and electronic applications.

These include: telecommunications, automotive, semiconductors, connectors, switches, cameras, and other components. But the



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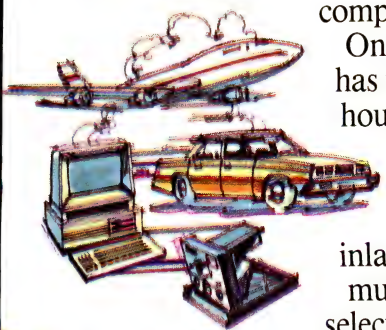
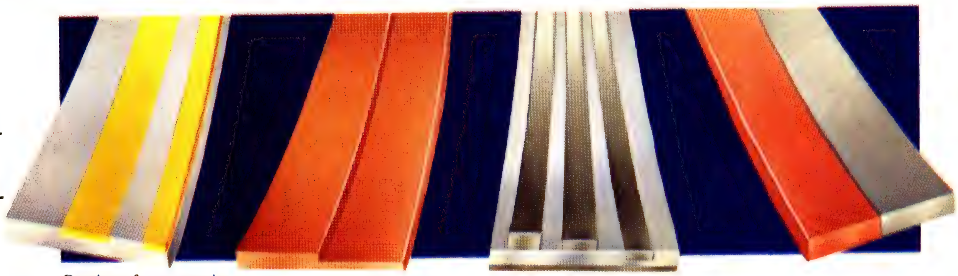
We offer more cladding technologies than any other company. Only TMI has the in-house capabilities for producing inlay clad, multi-gauge, selective solder coating, EB welding, and zone annealing. A wide variety





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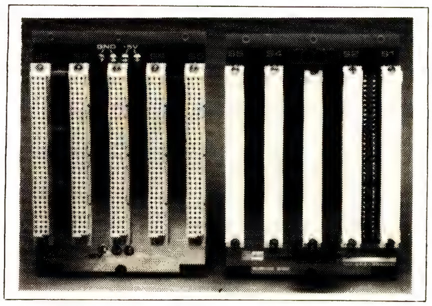
CIRCLE NO 169

time at 0.7V p-p input signals. The amplifier directly drives the CRT of a high-resolution video monitor and has scan rates around 64 KHz. The amplifier contains dc gain-control circuitry and provides a fully dc-restored video output. It features 10% max overshoot and a settling time of <2 nsec. Frequency response is 50 Hz to 120 MHz, and the amplifier operates over 0 to 50°C. Four versions are specifically designed for monochrome, in-line, delta-delta, and Trinitron picture tubes. The module measures 6×3.5×1.2 in. and requires no additional heat sinking for output devices.

Extron Electronics, 10041 Montecito Plaza, Garden Grove, CA 92640. Phone (714) 530-6265.

Circle No 550



VME BACKPLANE

The 234-39122C 5-slot backplane is compatible with Motorola's I/O interface specification. Each unit comes tested and assembled, with connectors, removable termination, and power connectors. The 4-layer device incorporates five pressfit DIN connectors and two polarized power connectors. Each connector position is fitted at the rear with a removable DIN-connector shroud to allow female DIN flat-cable connectors to mate. For larger I/O applications, the termination may be removed; multiple 5-slot backplanes can be linked via a 64-conductor ribbon cable. $193.

BICC-Vero Electronics Inc, 171 Bridge Rd, Hauppauge, NY 11788. Phone (516) 234-0400.

Circle No 551

SENSOR SYSTEM

The Series SX-23 miniature, self-contained photoelectric system operates on 12 to 24V dc input. Fiber-optic cables in 1- to 3-ft lengths couple directly to the miniature amplifier. These cables are available either in a duplex version (for through-beam operation) or in a simplex version (for reflex operation). The system features a 3-msec response time, a solid-state transistor output, the ability to detect objects as small as 0.004 in., immunity to ambient light, and a metal amplifier package with a built-in sensitivity adjustment. $209. Delivery, stock to 8 wks.

Control Engineering Inc, 1686 Riverdale St, West Springfield, MA 01089. Phone (413) 781-1330.

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Rugged reliability

in high voltage, DC power supplies . . . the Glassman PG series

Air insulated, lightweight and compact, the PG series is the forefront of high voltage power supply technology. Its off-the-line switching design provides high efficiency and high reliability. The PG series is tightly regulated — better than ±0.005% line and load . . . standard models range from 0-5KV @ 100 mA to 0-300KV @ 2mA, positive, negative, or reversible polarity.

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CIRCLE NO 170

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To request for Sales engineer call/samples Circle 241

ITT Schadow Micro Key Switches

Ultraminiature size and low applied cost make ITT Schadow KSA switches a superior choice where front panel space is at a premium.

If you're interested in saving up to 50 per cent on front panel space, you should ask for free samples of ITT Schadow's KSA switches. Not merely because they're small, but also because they can save you money across the board.

Auto insertable: KSA switches can be automatically inserted with your existing IC DIP insertion machines. This means higher productivity and lower installation costs than other types of switches. In addition to this time and labor savings, machine insertable KSA switches have highly competitive unit prices.

Sealed construction: The unique sealed design prevents contamination during flow soldering and automated cleaning processes. Switches are compatible with industry standard water wash, solvent immersion, ultrasonic bath, and vapor phase operations.

Compact size: Center-to-center spacing of 7.62x10.16mm is possible through their efficient package design. Features include built-in contact straps which simplify X-Y Coding and minimize the need for double-sided PCBs. Custom keycaps, PCB positioning studs, snap-in terminal pins and options such as integral ground terminals for electrostatic discharge (ESD) protection are also available.

For details on ITT Schadow's money-saving KSA Micro Key Switches – or for information on ITT Schadow's custom switchmaking and world-wide sourcing – mail the coupon below or contact your local authorized ITT Schadow switch center.

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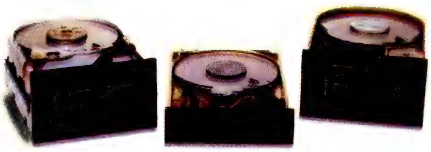
Schadow ITT

WHEN IT COMES TO WINCHESTERS, WE RUN CIRCLES AROUND THE COMPETITION.



Tandon's made so many improvements in Winchesters that the rest of the drive industry is dizzy just trying to keep up.

We build a wide range of drives. Open-loop and high performance closed-loop models. In both full and half-height versions ranging from 12.8 to 36.2MB unformatted capacities.

All are available in high quantities now, because Tandon's been ramping up capacities at a pace like never before. And we've kept up the pace of improving Winchester performance as well, so the most advanced technology is ready when you need it.

As far as our current line is concerned, the low-cost TM500 line has become the most reliable full-height 12.8 and 19.1MB drives you can get. The new TM252 half-height 12.8MB surpasses the industry's most critical specifications. And our TM703 has been increased to 36.2MB to make it the ideal high capacity drive for desktop business systems.

Another part of our success revolves around our highly automated plated media plant in Northern California. Its buttoned-down efficiency and technological sophistication guarantee higher quality and higher volume production than ever.

What's more, our proprietary plated media is used in all our Winchesters, no matter what the capacity. It's more durable, more reliable. And it has six times more storage capacity than oxide media. At less than half the cost.

In fact, it's so good, other drive manufacturers are buying their plated media from us.

So all around, Tandon Winchesters have more capacity in less space at less cost.

And that's a pretty good circle to run around in.

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THE DRIVING FORCE BEHIND THE SMALL COMPUTER INDUSTRY.

Tandon Corporation, 20320 Prairie, Chatsworth, CA 91311. (818) 993-6644, TWX: 910-494-1721, Telex: 194794. Regional Sales Offices: Boston (603) 888-8612 • New York (201) 851-2322 • Atlanta (404) 934-0620 • Chicago (312) 530-7401 • Dallas (214) 423-6260 • Irvine (714) 669-9622 • Santa Clara (408) 727-4545 • Kelsterback/Frankfurt, West Germany 6107-2091, Telex: 411547 • Reading/London, England (0734) 664-676, Telex: 848411. Distributors: Hall-Mark, Kierulff, Schweber.

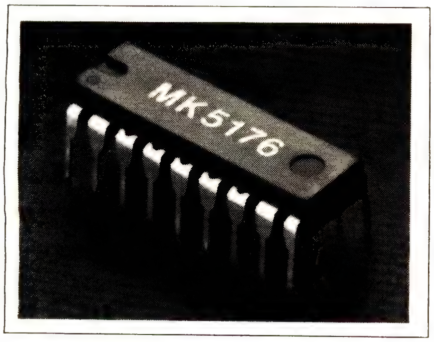
CIRCLE NO 171

SWITCHER ICs

The ULN-8161M and -8168M ICs, for control of switched-mode power supplies, come in 8-pin plastic miniature DIPs. The ULN-8161M controller, for use in low-cost power supplies, is also suitable for motor controllers and dc/dc converters. It includes an error amplifier, a sawtooth generator, current limiting, and double-pulse protection. The ULN-8168M is pin-compatible with the -8161M and features a ±2% tolerance on the temperature-compensated reference, while the -8161M features a ±5% tolerance. ULN-8161M, $1.12; ULN-8168M, $1.22 (100).

Sprague Electric Co, Integrated Circuit Operations, 115 Northeast Cutoff, Worcester, MA 01606. Phone (413) 664-4411.

Circle No 553

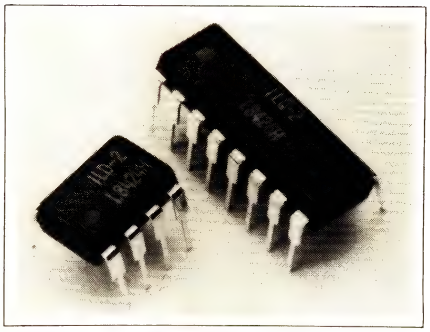


REPERTORY DIALER

The MK5176 repertory dialer features continuous mute timing, which minimizes transceiver noise that occurs during dialing. The dialer offers automatic dialing of 10 16-digit numbers and last-number redial capability. In normal pulse mode, the part accepts keyboard inputs and provides the pulse logic levels required for loop-disconnect signaling. The dialer operates over −30 to +60°C from 10.5V dc max. It dissipates 500 mW max at 25°C. In 18-pin plastic package, $5.10 (1000). Available 1st qtr 1985.

Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006. Phone (214) 466-6000.

Circle No 554



OPTOCOUPLERS

These multichannel couplers replace the industry-standard 4N35 single couplers. The ILD-2 dual-channel optocoupler provides two isolated channels in an 8-pin miniature DIP; the ILQ-2 quad-channel coupler offers four isolated channels in a 16-pin DIP. The devices employ a GaAs infrared emitter and a silicon npn phototransistor. They feature 7400 Series TTL compatibility, 7500V isolation, 0.5-pF coupling capacitance, and UL approval. The vendor claims that the couplers transmit signal information with virtually no crosstalk. ILD-2, $1.35; ILQ-2, $2.85 (1000). Delivery, 8 to 12 wks ARO.

Siemens Components Inc, Optoelectronics Div, 19000 Homestead Rd, Cupertino, CA 95014. Phone (201) 321-4842.

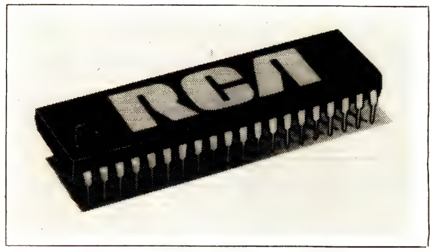
Circle No 555

DECODER/DRIVERS

These nonmultiplexed 4-digit, 7-segment decoder/drivers contain the circuitry needed to drive standard LCDs. The CD22104 and the -22105 decode binary inputs into hexadecimal outputs, while the -22104A and -22105A decode binary inputs into decimal outputs. An internal ROM decodes the four data inputs into the 7-segment outputs that drive the LCDs. CD22105 and -22105A permit simple interfacing with a μP. These models employ a 2-bit select-code latch controlled by two chip-select inputs. In the CD22104 and -22104A, four digit-select inputs go directly to latches that control each digit. A backplane I/O pin lets you synchronize devices when cascading decoder/drivers to drive additional digits. All four models use 5V typ, operate over −20 to +70°C, and come in 40-pin plastic DIPs. $5.95 (100). Delivery, 8 wks ARO.

RCA Solid State Div, Rte 202, Somerville, NJ 08876. Phone (800) 526-2177.

INQUIRE DIRECT



8-BIT CMOS μP

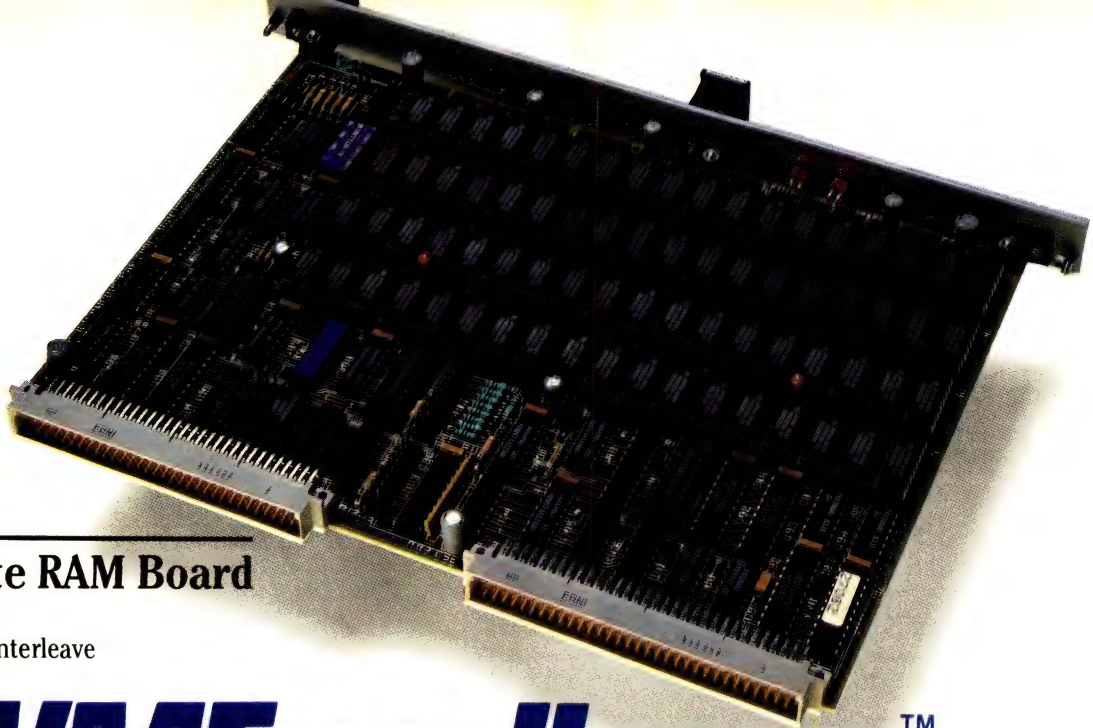
The CDP6805E3 8-bit μP addresses 64k bytes of external memory. The μP, which is an enhanced version of the CDP6805E2, is a fully static CMOS device that contains a CPU, 112 bytes of on-chip RAM, I/O, and an internal 8-bit timer with a software-programmable 7-bit prescaler. Typical operating power is 35 mW when the device is operating from a 5V supply. The μP consumes 5 mW in wait mode and 25 μW in stop mode. Two hardware interrupts (timer and external) and one software interrupt can be used. Master and power-on resets are provided. The instruction set consists of 61 basic commands of five types: register/memory, read/modify/write, branch, bit manipulation, and control. The μP operates from supply voltages between 3 and 6V dc and comes in a 40-pin plastic DIP specified for the 0 to 70°C temperature range. $9.18 (1000).

RCA Solid State Div, Rte 202, Somerville, NJ 08876. Phone (800) 526-2177.

INQUIRE DIRECT

POWER MOSFETs

The MTP3055A power MOSFET, a member of the TMOS III family, is



IV-1611

2 Megabyte RAM Board

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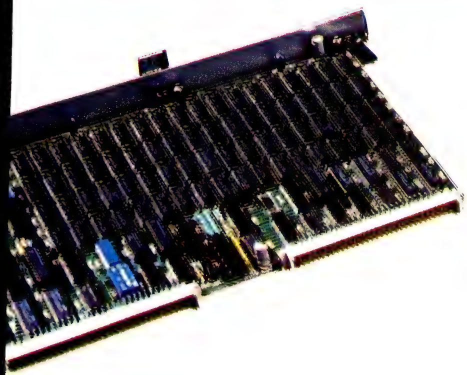

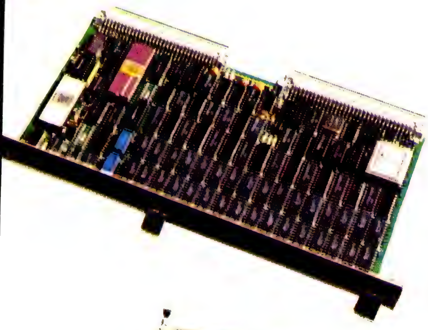

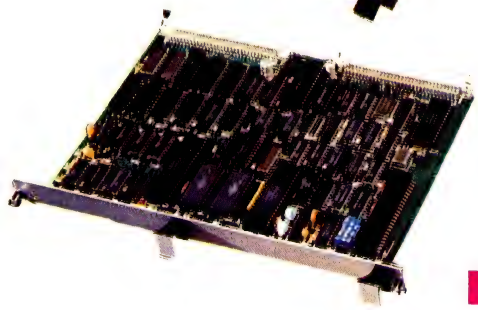

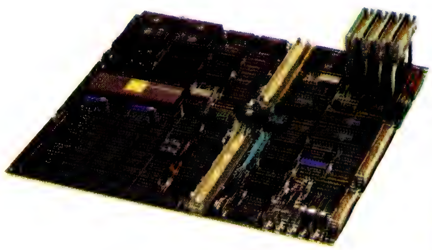

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CIRCLE NO 126

rated at 60V, 12A and features an $R_{DS(ON)}$ of 0.15Ω. It can replace the industry-standard 2N3055 bipolar npn transistor in many applications. The MTP14N05A is rated at 50V, 14A and has a 0.10Ω $R_{DS(ON)}$; the MTP16N05A is rated at 50V, 16A and offers a 0.08Ω $R_{DS(ON)}$. Cell density of the TMOS III A Series products is 1,000,000 cells/in^2. The devices come in TO-220 packages. MTP3055A, $0.60; MTP14N05A, $1.31; MTP16N05A, $1.46 (100). Delivery, 6 to 8 wks ARO.

Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036. Phone (602) 244-4911.

Circle No 556

ARRAYS

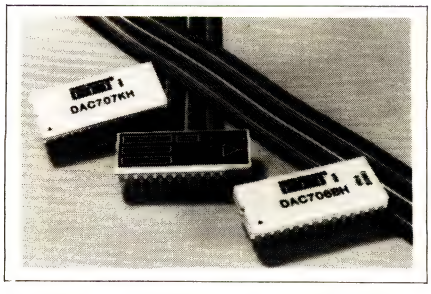
This family of programmable arrays has a 15-nsec max access time over 0 to 85°C and a 20-nsec max access time over −55 to +125°C. The devices dissipate 600 mW typ. In most applications, a single 20-pin array can replace three to six advanced Schottky SSI/MSI parts; in some cases, the vendor claims, this array can replace as many as 10 parts. For the commercial temperature range, $11.50 (plastic), $13.50 (ceramic); for the military temperature range, $18.50 (ceramic) (100).

National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 721-5000. TWX 910-339-9240.

Circle No 557

D/A CONVERTERS

For servomotor applications, the DAC710KH and DAC711KH provide high-resolution monotonic output transitions (±2048 counts around bipolar zero over 0 to 70°C). Differential linearity error (DLE) (±2048 counts around biploar zero) is +0.006, −0.003% of FSR at 25°C max. At 0 to 70°C max, DLE is



+0.009, −0.003% of FSR. Maximum gain drift is ±50 ppm/°C. Settling time (to ±0.003% of FSR) is 4 μsec and 350 nsec for the -711KH and -710KH, respectively. The -710KH provides a ±1-mA current output; the -711KH offers a ±10V output. Both models accept complementary binary-coded digital input and are compatible with TTL, LS TTL, and 54/74HC devices over the specified temperature ranges. Each model has a precision buried zener reference in its monolithic chip; the -711KH adds a low-noise, fast-settling op amp. In hermetic, 24-pin ceramic dual DIPs, from $29 (100).

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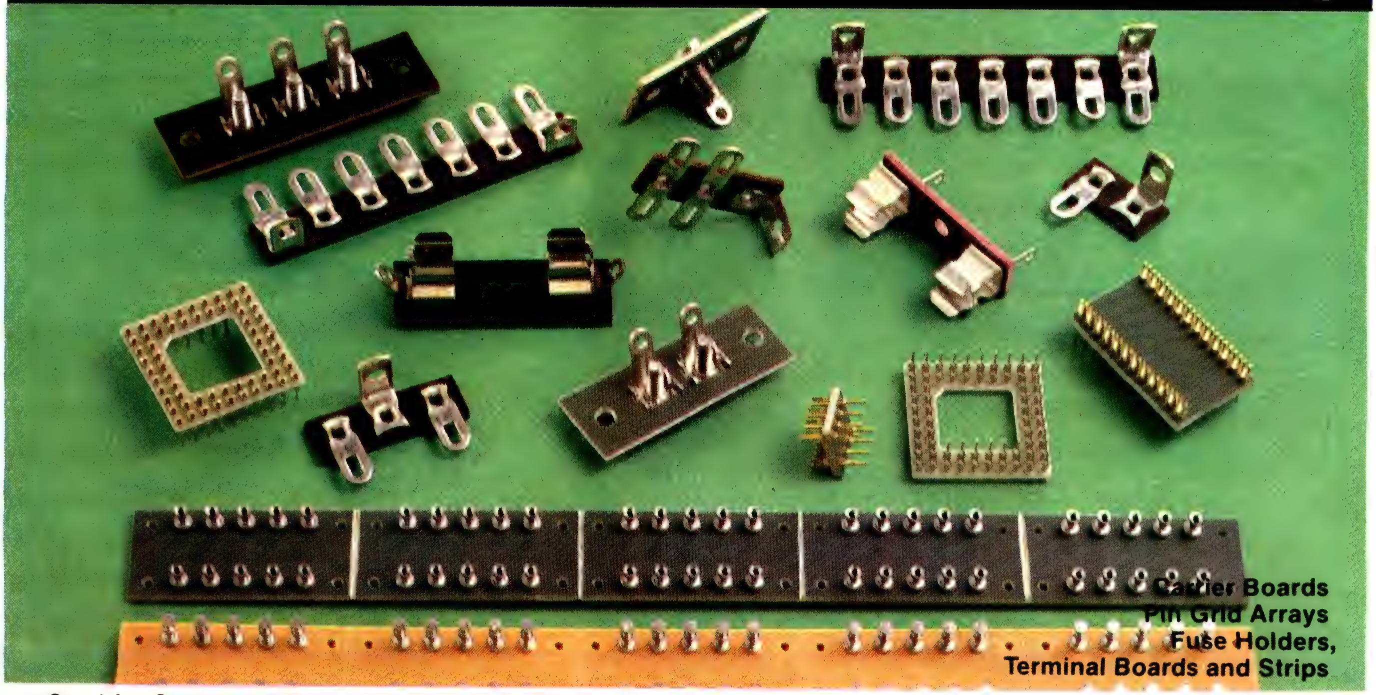

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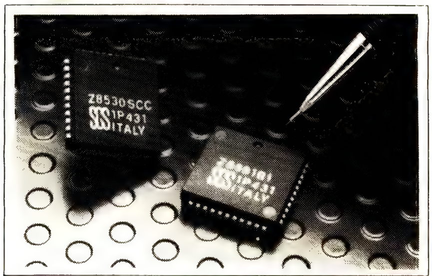

SMD μPs

Quad-in-line J-type plastic chip-carrier packaging is available for the company's Z8, Z80, Z8000, and Z8500 Series μPs. These surface-mounted μPs and peripherals are offered in commercial, industrial, and military temperature ranges. They come in plastic or ceramic packages and in a ±10% power-supply range. Pricing for a typical Z80 CPU (4-MHz version) is approximately $2.50 (10,000).

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 559

LOGIC DEVICES

The HPL-16LC8 is a CMOS-programmable logic circuit that is functionally equivalent to and pin-compatible with the industry-standard bipolar 16L8 but consumes 95% less power. You can use an existing 16L8 or 16P8 master device or JEDEC-formatted paper tape to program the circuit. Test circuitry permits complete functional, ac, and dc testing of the device prior to programming. The device also features programmable output polarity, which permits the polarity of each output to be changed individually from active-low configuration to active-high by programming. The part features a standby current of 150 μA max (guaranteed over the device's temperature range). Operating current is less than 5 mA/MHz. Average operating power is less than 50 mW; the standby power requirement is 250 μW. The device is available in commercial, industrial, and military temperature ranges and comes in a 20-pin ceramic DIP. Maximum propagation delay is 125 nsec over the full voltage and temperature ranges. In 100 qty, $12.99 (0 to 70°C); $14.43 (−40 to +85°C); $28.86 (−55 to +125°C); $36.07 (−55 to +125°C with DASH-8 processing).

Harris Semiconductor, Box 883, Melbourne, FL 32919. Phone (305) 727-9100.

Circle No 560

DYNAMIC RAMs

These dynamic RAMs are organized in 64k 4-bit words for parallel transmission of data. The HM50464P

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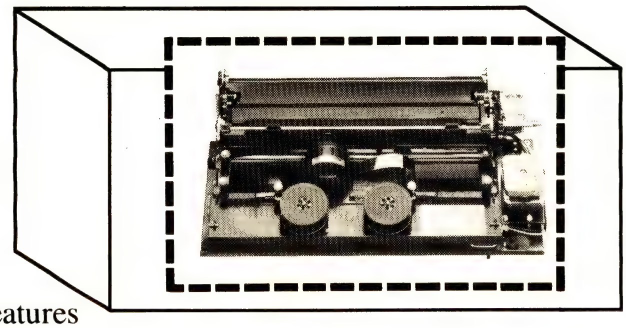

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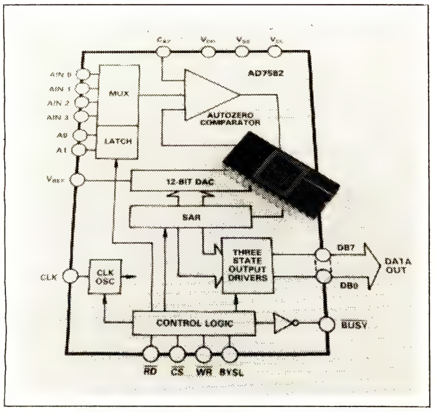
Datron Instruments Ltd. Hurricane Way, Norwich Airport, Norwich NR6 6JB England (0603) 404824 Telex 975173

CIRCLE NO 176

transfers data in page mode; the HM50465P uses nibble mode. Both models are available with 120-, 150-, and 200-nsec access times. In nibble mode, the fastest version of the HM50465P can read or write 16 bits (four parallel bits in four sequential locations) in 400 nsec (40M bps). Both models consume 350 mW while active and 23 mW in standby mode, and both come in 18-pin plastic DIPs. \$75 (sample qty). Available 1st qtr 1985.

Hitachi America Ltd, 2210 O'Toole Ave, San Jose, CA 95131. Phone (408) 942-1500.

Circle No 561



A/D CONVERTER

The AD7582 4-channel, successive-approximation A/D converter features a maximum conversion time of 100 μsec. The 12-bit CMOS converter requires a 5V external voltage reference and several passive components. An autozeroed comparator provides low zero and gain errors. The device accepts analog signals of 0 to 5V. You can use either an internal or an external clock. The converter operates from ±5 and +15V power supplies and consumes 150 mW max. Maximum differential nonlinearity for all grades is ±¾ LSB; maximum full-scale error is ±¼ LSB; and maximum offset error is ±¼ LSB. The converter comes in a 28-pin DIP. KN version (plastic, specified over 0 to 70°C), \$32.50; BD version (ceramic, specified over −25 to +85°C), \$37.50; TD version (ceramic, specified over −55 to +125°C), \$92.37 (100).

Analog Devices Inc, Box 280, Norwood, MA 02062. Phone (617) 935-5565.

Circle No 562

DYNAMIC RAMs

These three configurations of 256k-bit dynamic RAMs feature access times of 150 and 200 nsec. The devices are implemented in NMOS technology with double-poly interconnects. The μPD41256 is a 256k×1-bit page-mode device, the -41257 is a 256k×1-bit nibble-mode part, and the -41254 is a 64k×4-bit part. The dynamic RAMs feature nonredundant parts. μPD41256, \$27.50; μPD41257, \$30; μPD41254, \$33 (100).

NEC Electronics Inc, Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

Circle No 563

D/A CONVERTER

This silicon-gate, 8-bit CMOS D/A converter for graphics terminals provide composite sync, composite blank, and 10%-bright signals (the last is for displaying white characters on white backgrounds). It drives 75 or 37.5Ω loads while operating at a minimum conversion rate of 25M samples/sec. The device has a linearity of one bit, requires one 5V supply, and is TTL/CMOS compatible. The device has the same specs as the TML1840 except that the composite video signals are not adjustable, and signal inversion is not supplied. The converter comes in a 20-pin plastic DIP. TML1842A, \$20.12; TML1842B, \$18.11 (100).

Telmos Inc, 740 Kifer Rd, Sunnyvale, CA 94086. Phone (408) 732-4882. TWX 910-339-9623.

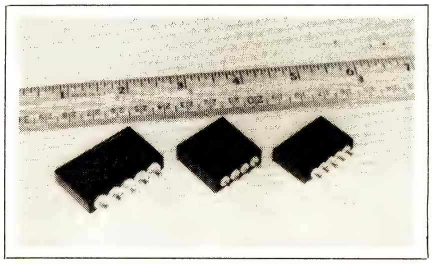
Circle No 564

GATE ARRAYS

According to the vendor, these HCMOS arrays have the speed and output current drive of bipolar TTL arrays. LL8000 Series 2-μm, 2-layer metal HCMOS arrays have 10-mA buffers that are reconfigurable to 20 mA per output. Gate counts range from 880 to 3200 (2-input NAND). The arrays' delay times are identical to those of the LL7000 series. They are supported by more than 200 LL7000 macrocells and more than 400 LL7000 macrofunctions. A typical 3000-gate array in a 68-pin plastic chip carrier specified for commercial use costs \$55 (2000).

LSI Logic Corp, 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 263-9494.

Circle No 596



RECTIFIERS

SL6300, SL1500, and SL30300 Series bridge rectifiers are available with peak inverse voltage ratings of 1000V in the general-purpose (5-μsec) versions and 600V in the fast-recovery (150-nsec) versions. The last two are also available in a 150V, 30-nsec version. The SL1500 rectifier is a single-phase, 15A version with a thermal impedance of 2°C/W. The case is 0.31 in. high. The 0.25-in.-high SL6300 is a 3-phase, 6A version with a thermal impedance of 2°C/W. The SL30300 is a 3-phase, 30A model and is 0.31 in. high; its thermal impedance is 1.25°C/W. The bridges are constructed using internal glass hermetic diodes and are available with JAN, JANTX, or JANTXV diodes. Screening to MIL-STD-19500 is available. A 200V, general-purpose version of the SL1500 is \$20; the SL6300, \$31; and the SL30300, \$44 (100). Delivery, 6 to 8 wks ARO.

Sensitron Semiconductor Div, RSM Electron Power Inc, 221 W Industry Court, Deer Park, NY 11729. Phone (516) 586-7600. TLX 967737.

Circle No 597

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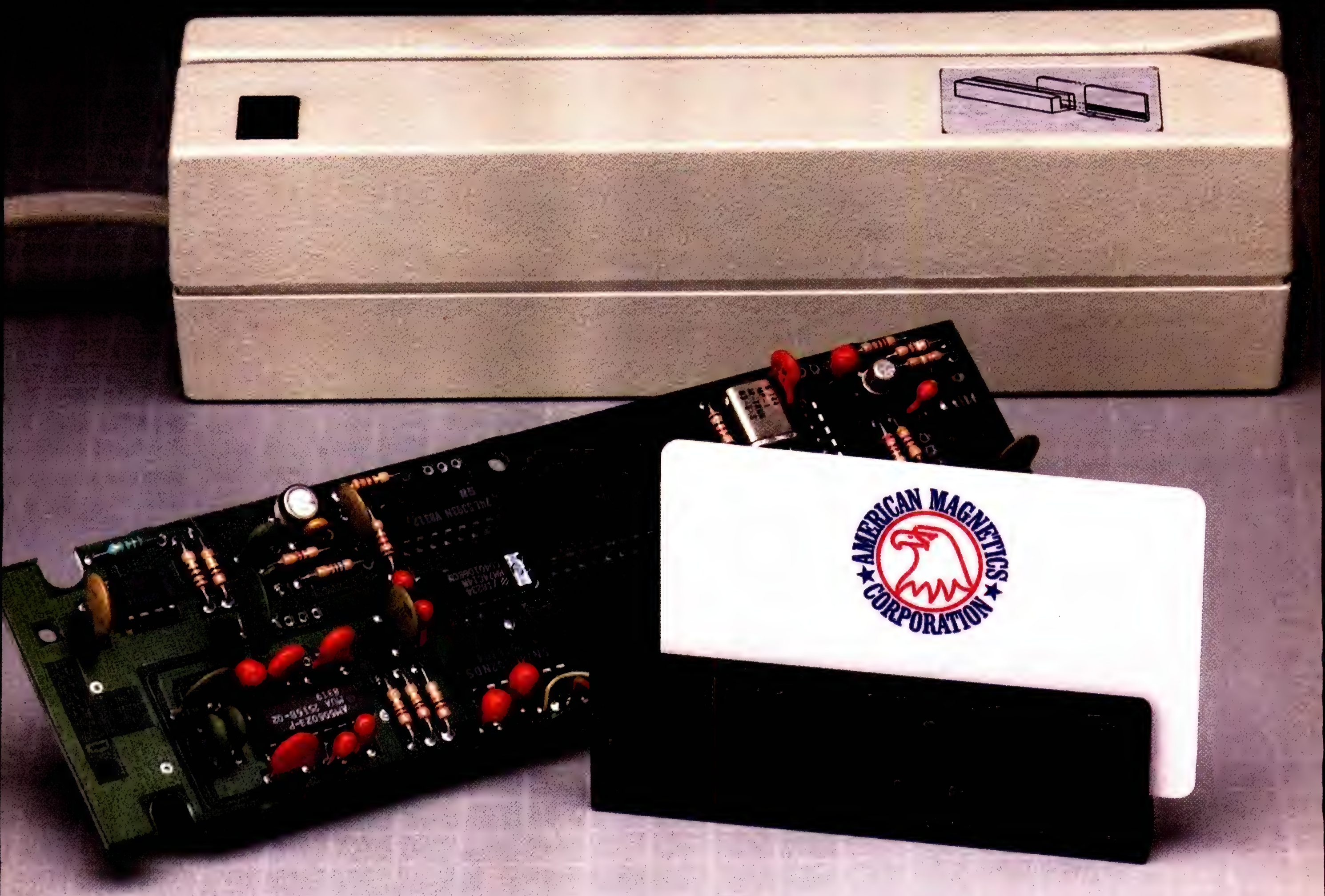

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DATA INTERFACE

The GM/SEL32 interface provides the required logic terminations and compatible driver-receiver circuitry to interface the firm's analog and digital conversion subsystems with the Gould/SEL HSD controller. A 16- or 32-bit format is available. In the 32-bit format, a data-packing feature allows data to be packed into 32-bit words (at rates of 500 kHz or 1 MHz) and then transferred to the computer at a ÷2 rate. Options for the GM/SEL32 include simultaneous sample/hold control, programmable conversion rates, high-speed random channel sequencing, programmed start and stop modes, analog signal conditioning, antialiasing filters, digital I/O, and D/A conversion. As another option, the device can multiplex discrete digital inputs or outputs. Software support is available for Concept 32 computers (Model 27, 67, or 87) running with MPX 2.1 or 3.X operating systems. $3775. Delivery, 120 days ARO.

Preston Scientific, 805 E Cerritos Ave, Anaheim, CA 92805. Phone (714) 776-6400. TLX 655321.

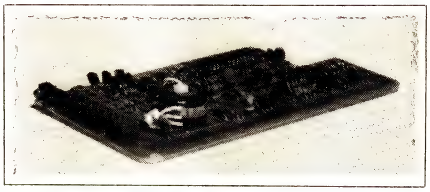
Circle No 565

TAPE DRIVE

You can use Model T201 6250 streaming magnetic-tape drives on all Stratus/32 continuous processing systems. It is also compatible with IBM 6250 tape drives. At 6250 or 1600 bpi, the T201 operates at 75 in./sec in the streaming mode or 25 in./sec in the start/stop mode. The drive reads and writes standard ½-in. (12.7mm) reel-mounted magnetic tape; data can be unformatted or ANSI- or IBM-formatted. $25,000.

Stratus Computer Inc, 55 Fairbanks Blvd, Marlboro, MA 01752. Phone (617) 460-2000. TLX 294112.

Circle No 566



MODEM BOARD

This asynchronous 120k-bps half-duplex short-haul modem board is designed for industrial-control-equipment manufacturers. The 2-wire board uses an advanced on-off key technology to provide you with high-transparency, automatic line turnaround, and the ability to receive while transmitting for use with CD/CSMA protocols (such as Ethernet). Transformer coupling eliminates dc continuity requirements and removes restrictions for transceiving data on inexpensive 22 AWG phone station wire in noisy, high common-mode-voltage areas. Error rates as low as one in a billion are possible by using RS62A/U-type cable over distances of 7000 ft. Built-in networking provisions support star, multidrop, or daisy-chain configurations, either separately or in combinations. The standard OEM board is 5.5×6.5 in., requires ±12V dc and +5V dc, and accepts TTL-level bit serial I/O. $350 (100). Delivery, 6 wks ARO.

Controlonics Corp, Nonwire Div, 4 Kidder Rd, Chelmsford, MA 01824. Phone (617) 256-1918.

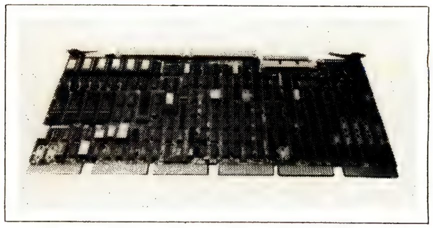
Circle No 567

MASS STORAGE

The Quick Cassette is a small, high-speed, mass-storage system that replaces audio cassette systems. The manufacturer's Microwafer storage cartridges are used in the drive, which plugs into the existing cassette port of any Commodore 64 or Vic 20 computer. Because the Quick Cassette can read data 15 times faster than an audio cassette, you can load 64k bytes in approximately 30 sec. Comparatively, it takes 23 min with an audio cassette and 2 min with a Commodore disk. The storage system has a slow-speed read mode that emulates an audio cassette for the Commodore 64; this enables you to boot the system from a Microwafer. You can copy programs from either a Commodore C2N audio cassette or another Quick Cassette drive by means of a connector. The Quick Cassette operating system controls the drive. Its functions include format, load, save, verify, directory, and clean, and it also has a file management utility. <$85.

Entrepo Inc, 1294 Lawrence Station Rd, Sunnyvale, CA 94086. Phone (408) 734-3133.

Circle No 568



CACHE COUPLER

The Tape Dimension IV Cache-coupler is the first cache-buffer coupler to emulate the DEC TS11 tape subsystem, according to the manufacturer. A 64k-byte cache buffer stores multiple records and ensures that streaming tape devices operate at maximum efficiencies on DEC-PDP-11 families; it also provides total immunity to "data late" conditions of heavily populated buses while maintaining the tape at streaming speeds. The coupler provides the interface for an industry-compatible, formatted streaming tape drive at 1600, 3200, or 6250 bpi at speeds to 125 ips. It also supports start/stop tape drives at densities to 6250 bpi and tape speeds of 200 ips. The TD-IV fits directly into any

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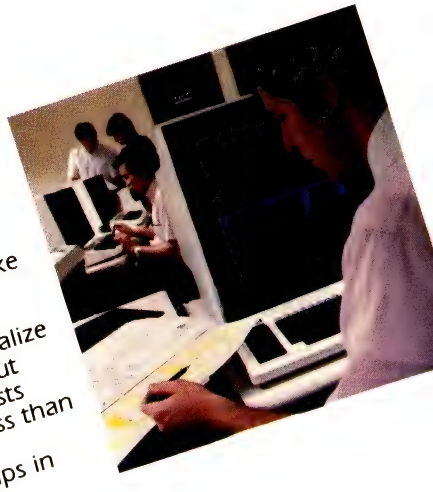

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Western Peripherals, 14511 New Myford Rd, Tustin, CA 92680. Phone (714) 730-6250.

Circle No 569

½-HEIGHT WINCHESTER

The 724 half-height 5¼-in. Winchester disk drive is a 26M-byte unit boasting a closed-loop servo system. With this drive you benefit from such data-protection features as high damping, 4-point shock mounts, a dynamic spindle brake, and an actuator that automatically retracts the read/write heads when the drive is powered down. The formatted capacity of the 724 is 20M bytes. The closed-loop servo-positioning system doubles the drive's track density from 360 tpi to 720 tpi. The stepper-motor/band-actuator system positions the read/write head; the drive measures 1.63×5.8×8 in. <$500 (OEM qty). Deliveries to begin this qtr.

Shugart Corp, 475 Oakmead Parkway, Sunnyvale, CA 94086. Phone (408) 737-4355.

Circle No 570

ONE-BOARD SYSTEM

A single-board computer, the DPX86/ME contains both the Intel 286 and 186 µP with each running dedicated environments. The system possesses a shared memory capability that allows I/O processing (including Ethernet, RS-232C asynchronous communications, and either a Centronics or an SCSI disk interface) to occur simultaneously with an applications environment controlled by the independently running 286. You can configure 1M bytes of RAM and 400k bytes of ROM. In addition, you can access a maximum of 16M bytes of RAM by using the Intel iLBX memory extension interface. An option for data encryption is available via the 287 numeric coprocesser. The DPX86/ME supports Xenix, RMX286, and PC-DOS. Networking software includes a real-time executive and TCP/IP Arpanet protocols. DPX86/ME, from $4000 (100); encryption option, $140; 287 coprocessor, $245.

Little Machines Inc, 4141 Jutland Dr, San Diego, CA 92117. Phone (619) 483-3606.

Circle No 571

TOEI
Toei Electronics Co., Ltd.

HIGH PERFORMANCE, VERSATILITY, VIVID COLOR, CRISP IMAGE

TOEI COLOR DISPLAYS FTC/CDM – SERIES.

TOEI, experienced Display Monitor specialists, offer a wide selection of Color CRT Displays. You can choose from our versatile standard models or OEM versions to meet your exacting requirements.

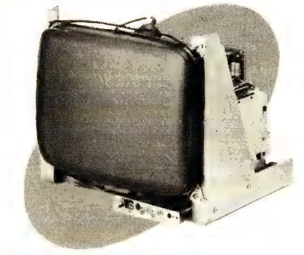
FTC Series •Housed in lightweight, impact-resistant Cabinet. •Hi-Contrast (Black Face), Hi-Brightness CRT displays a crisp, sharp image. •Limitless colors can be displayed through Analog Input.

FTC-12" Series

Item / Versions	RGB Version	NTSC Version	NTSC & RGB Version	IBM PC Compatible only	
12" (CRT Pitch)	FTC-1208-R (0.28mm Dot trio) FTC-1203-R (0.38mm Dot trio) FTC-1201-R (0.47mm Stripe)	FTC-1201-N (0.47mm Stripe) FTC-1200-N (0.63mm Stripe)	FTC-1201-NR (0.47mm Stripe)	FTC-1208-HF (0.28mm Stripe) FTC-1203-HF (0.38mm Stripe)	FTC-1208-W (0.28mm Dot trio)
		PAL Version	PAL & RGB Version		
		FTC-1201-P (0.47mm Stripe) FTC-1200-P (0.63mm Stripe)	FTC-1201-PR (0.47mm Stripe)		
14" (CRT Pitch)	FTC-1455-R (0.31mm Dot trio) FTC-1435-R (0.39mm Dot trio) FTC-1423-R (0.42mm Stripe) FTC-1410-R (0.52mm Stripe)	NTSC Version	NTSC & RGB Version	FTC-1455-HF (0.31mm Dot trio) FTC-1435-HF (0.39mm Dot trio)	FTC-1455-W (0.31mm Dot trio)
		FTC-1410-N (0.52mm Stripe) FTC-1416-N (0.64mm Stripe)	FTC-1410-NR (0.52mm Stripe)		
		PAL Version	PAL & RGB Version		
		FTC-1410-P (0.52mm Stripe) FTC-1416-P (0.64mm Stripe)	FTC-1410-NR (0.52mm Stripe)		
Input Signal Level	RGB Analog RGB plus Intensity RGB TTL	NTSC(PAL)	NTSC(PAL) RGB Analog RGB plus Intensity RGB TTL	RGB plus Intensity / RGB TTL	
Applications, Others	IBM PC · PC jr. Apple IIc, IIe *	IBM PC · PC jr., Apple IIc · IIe, Commodore C-64		H.F. 25kHz	Scanning Doubler

* With RGB card. FTC-1203-R, FTC-1203-HF : Non-Glare

CDM-14" Series



CDM Series (Unit for OEM)

Model	CRT Size	CRT Pitch
CDM-1208-PC	12"	0.28mm Dot trio
CDM-1203-PC	12"	0.38mm Dot trio
CDM-1201-PC	12"	0.47mm Stripe
CDM-1455-PC	14"	0.31mm Dot trio
CDM-1435-PC	14"	0.39mm Dot trio
CDM-1423-PC	14"	0.42mm Stripe
CDM-1410-PC	14"	0.52mm Stripe

- OEM versions include Color 6"-26" in addition to the above, Monochrome 3"-26", CRT Pitch 0.64mm - 0.21mm, Horizontal frequency less than 64kHz, Non-glare to meet your requirements.
- Green/Orange CRT Displays are also available. (Included IBM PC Compatible.) CRT size: 9" or 12".
- We are looking for reliable and established distributor worldwide.

IBM PC is a Trademark of IBM Corp. Apple IIc, IIe are Trademarks of Apple Computer Inc. Commodore C-64 is a Trademark of Commodore Business Machine Inc.

TOEI ELECTRONICS (MFG) CO.,LTD.
Kanda Cent Bldg., 2-4, Yushima 1-chome Bunkyo-ku, 113 Tokyo JAPAN
Tel. (03) 257-1131 Telex. 0222-2555 TOEICO J FAX (03) 258-3560

CIRCLE NO 180

CONDUCTIVE SYSTEMS

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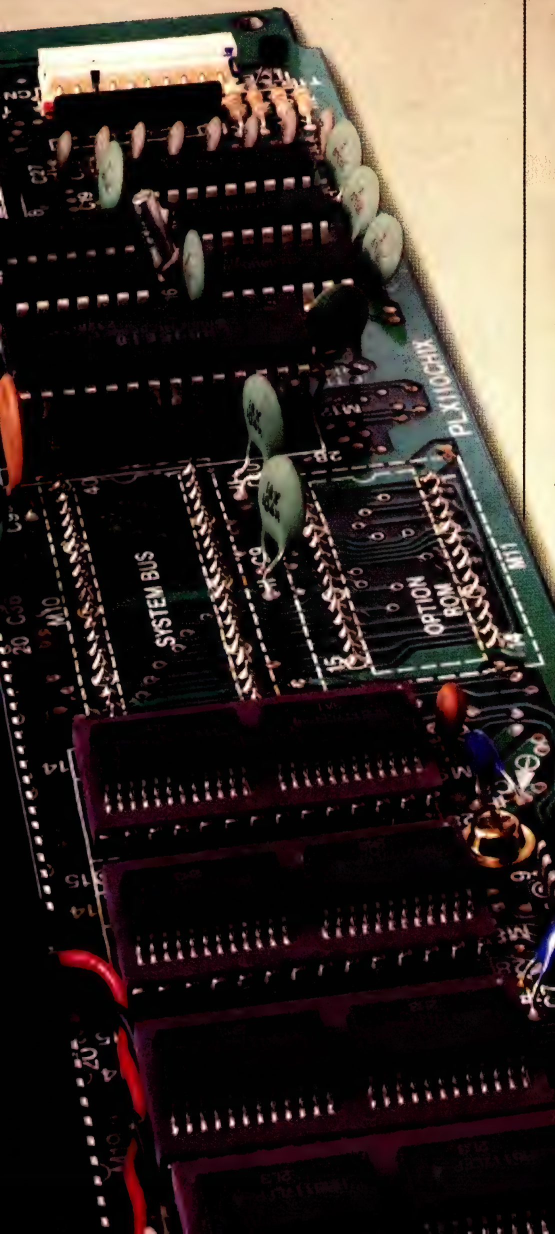
The cost of staying in business in the electronics industry can be high. Tough competition and tougher regulations can quickly cut into your profit margin. We have better answers, such as Eccocoat® CC-33W, a new one-component, waterborne coating that can save you up to 37% on application costs, as well as provide EMI/RFI shielding over the complete FCC mandated range.



How to get your profit up front.

We've got solutions that allow you to resolve EMI/RFI emission problems in the design phase. This includes our Conductive Applications Laboratory, which can help you specify materials, and figure out your costs, before you go into production.

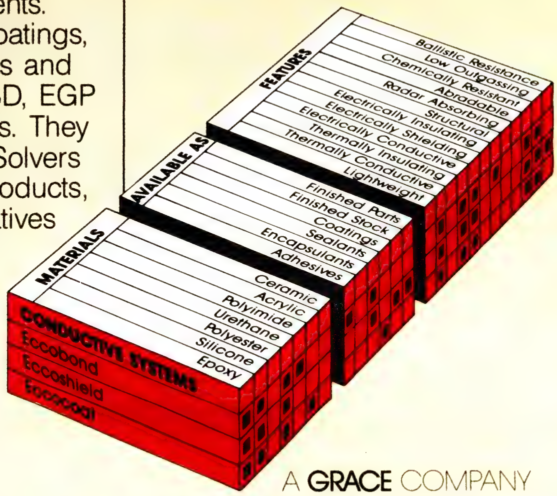
How to cover all your options.

We offer you more in the way of materials, not only in economy of use and cost, but to cover all your shielding requirements. These include sprays, coatings, tapes, gaskets, adhesives and sealants for EMI/RFI, ESD, EGP and environmental seals. They include our Problem Solvers series of shielding products, cost-effective alternatives for production and field repair. We can even customize an EMI/RFI field repair kit for your specific electronics product.

How to name your own price.

With our Value in Use program, you have the option to match the cost/performance features of shielding materials to select the product that best meets all of your needs, including your budget.

If you want to stay in the chips, and make them pay off for you, discover even more ways we can help by sending for "A Selective Guide to Conductives Technology," an up-to-date handbook on contemporary materials science. Emerson & Cuming, Marketing Services Department, Canton, MA 02021. Telephone: 617/828-3300, or call, toll-free, 1-800-TECHWAY (832-4929).

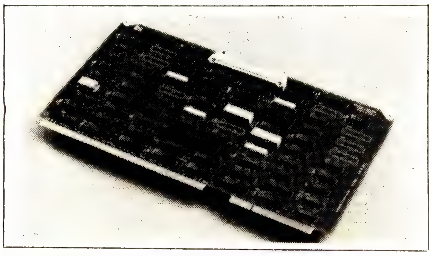


A GRACE COMPANY

EMERSON & CUMING

Where there's a way.

CIRCLE NO 181

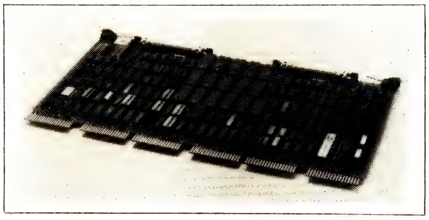


TAPE CONTROLLER

Model MTO2 of the Titleist SCSI tape controller series supports QIC-36 standard ¼-in. streaming cartridge tape drives using the QIC-24 media format. Working with one of the company's independent host adaptors, the MTO2 interfaces through the SCSI to IBM PCs and compatibles, the IEEE 796 Multibus, and the DEC Q Bus and Unibus. The QIC-24 format provides 9-track sequential, serpentine recording at 8000 bpi (GCR) at speeds of 90 ips. A read-after-write verification occurs automatically when data is recorded. The tape controller supports SCSI arbitration for as many as eight hosts or peripherals. Contained on a single 5¾×8-in. pc board, the MTO2 resides inside the QIC-36 tape transport. It requires +5V dc at 1.5A. $435. Delivery, 60 days ARO.

Emulex Corp, Box 6725, Costa Mesa, CA 92626. Phone (800) 854-7112; in CA, (714) 662-5600.

Circle No 572



MULTIPLEXER

The Optimux/16DMF+ asynchronous communications controller is designed for all PDP-11 and VAX computers. It possesses the standard capabilities of DEC DMF32 and DH11 subsystems as well as allowing you to connect 16 peripherals from a single backplane slot. The multiplexer offers bidirectional data flow control and multiword DMA transfers between the CPU and the controller. When the multiword transfer capability is enabled, the Optimux will pass 4-word data bursts to the CPU; when it is disabled, it performs single-word DMA operations. According to the company, it also provides twice the maximum data transfer rate of other systems. You can choose rates from 50 to 34,800 bps (software selectable). The controller supports serial printers with speeds of 900 lines/min, and you can switch-select two of the 16 channels as printer ports. The Optimux is contained on a hex pc board. You receive both DMF32 and DH/11/DM11 firmware with each board; the desired emulation can be easily selected. Power requirements are +5V at 7A, +15V at 0.035A, and −15V at 0.15A. Operat-

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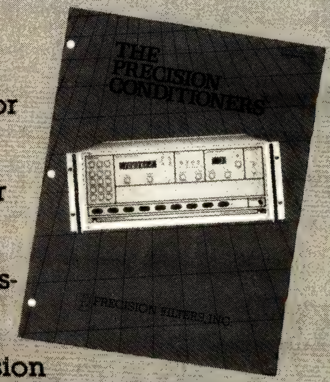
80 dB/octave attenuation. Time delay filters superior to Bessel. 1° phase match or better. Standard computer interfaces. Serial, parallel and GPIB.

We set these industry standards, and we keep extending the choice of Precision systems for HP, LP, TD, BP, BR and anti-alias filters. 2 channels to 64. Choice of cut-off frequencies, resolution, amplification and other features to match your needs precisely.

Read about them all in our summary catalog, **The Precision Conditioners.** Call 607-277-3550 or write.

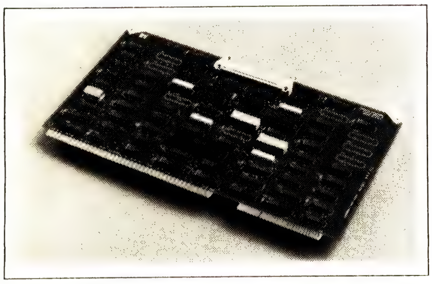


PRECISION FILTERS, INC.
240 Cherry Street, Ithaca, New York 14850

ing temperature ranges from 10 to 40°C. $3000. Delivery, 30 days ARO.

Distributed Logic Corp, Box 6270, Anaheim, CA 92806. Phone (714) 937-5700.

Circle No 573



HOST ADAPTER

Contained on a single pc board, the MB01 Multibus host adapter integrates SCSI-based disk- and tape-storage devices with IEEE-796 Multibus computers. The product provides an 8-bit data-path link and supports seven SCSI devices. Any combination of single-ended interface host systems, intelligent controllers, or intelligent peripherals is permitted. You can configure the MB01 for either serial- or parallel-bus arbitration, and it will respond to both vectored and nonvectored interrupts. The host adapter requires +5V, ±5% at 1.1A max and supports 8-, 16-, or 24-bit I/O addressing. $695. Delivery, 30 days ARO.

Emulex Corp, Box 6725, Costa Mesa, CA 92626. Phone (800) 854-7112; in CA, (714) 662-5600.

Circle No 574

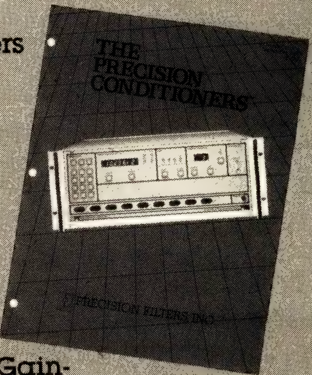
MULTIPLEXERS

These two asynchronous multiplexers connect serial lines to Unibus-based VAX and PDP-11 computers and provide half- or full-duplex communications. The DHU11 interfaces as many as 16 lines between any PDP-11 or VAX system with an integral Unibus operating under Version 4.0 of the VAX/VMS operating system. The DMZ32 supports as many as 24 lines for the Unibus-based VAX systems. Both controllers feature DMA and FIFO operations. The DHU11 utilizes RS-232C and RS-432A interfaces. You can program its 256-character FIFO buffer for split speeds and full modem control. Each channel contains a 64-byte FIFO buffer for output data. The DMZ32 consists of an interface module and a distribution panel (including power supply, TDM, and 24 EIA-RS232 connectors). Modem control logic is optional. You can place the panel as far away as 5000 ft from the Unibus connection. DHU11, from $3120; DMZ32, from $3215.

Digital Equipment Corp, Maynard, MA 01754. Call local sales office.

Circle No 575

BEGONE, OTHER PESKY PROBLEMS



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Instrumentation and filter amplifiers. Gain-ranging amplifiers and preamps. Multimode conditioners for strain, charge and voltage. Switching matrices. Frequency-band translators for super BP applications, as well as providing analog zoom for spectrum analysis, modal analysis and beam forming.

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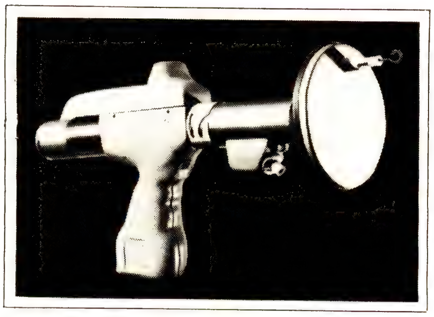


ESD SIMULATORS

Model H-10 initial-spike adapter, in conjunction with the company's Series 2000 ESD simulators, lets you simulate the electrostatic discharge from a handheld metal object such as a tool, key, bracelet, or ring. Model H-10 generates a 2- to 3-nsec, 15 to 30A peak-current spike. This pulse is characteristic of electrostatic discharges from personnel, which cause malfunctions in computers, ATE, and medical electronic systems. The previous lack of simulation capability for the 2- to 3-nsec spike at the start of an ESD tester's output wave has been a major cause of noncorrespondence between ESD test simulations and actual on-site ESD-related equipment malfunctions. Initial spike adapter, $395 (stock); Series 2000 ESD simulators, from $4500.

KeyTek Instrument Corp, 12 Cambridge St, Burlington, MA 01803. Phone (617) 272-5170.

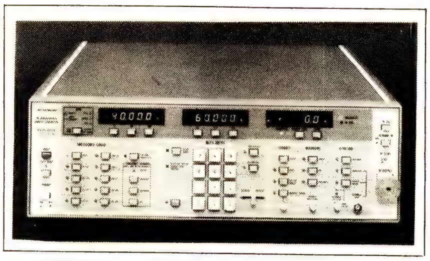
Circle No 576

DC/DC CONVERTERS

The 625 Series low-profile, 6W dc/dc converters offers power densities to 8W/in.^{3} The series is packaged in a 1×2×0.375-in. metal case that provides 6-sided shielding that virtually eliminates radiated EMI/RFI. Each of the three models has an input voltage of 5V dc; outputs are ±12V dc at ±250 mA, ±15V dc at ±200 mA, or ±18V dc at ±165 mA. Outputs are isolated from the inputs and can be referenced to ground to produce 24V dc, 30V dc, or 36V dc. Other features include 500V dc input/output isolation and short-term, short-circuit protection. An internal π input filter minimizes reflected ripple current on input lines. $69. Delivery, stock to 8 wks.

Power General, Box 189, Canton, MA 02021. Phone (617) 828-6216. TWX 710-348-0200.

Circle No 577



SWEEP GENERATOR

This programmable sweep generator covers the 40- to 60-GHz range with an output power of at least 1 mW. Model 6672A has five sweep modes, five preset carrier-wave frequencies, three markers, and full IEEE-488 programmability. It has a frequency accuracy of ±30 MHz and spurious signals of <−60 dBc. Residual FM over a 30-Hz to 15-MHz bandwidth is <50 kHz peak. The output signal is supplied through a standard WR-19 waveguide, and it requires an external directional detector or a power meter to level the output power. The instrument provides a 10-dB power-control range with a resolution of 0.1 dB. $23,000. Delivery, 16 wks.

Wiltron Co, Box 7290, Mountain View, CA 94042. Phone (415) 969-6500. TWX 910-379-6578.

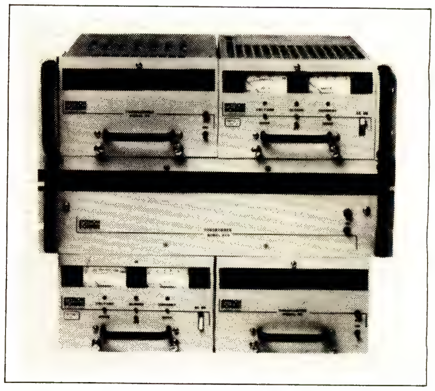
Circle No 578

MILITARY SWITCHER

This modular 4-output switching power supply provides 5V dc at 200A, −5V dc at 1A, and ±15V dc at 1.5A from a 115V ac single-phase 47- to 440-Hz input. Model M7963 meets MIL-E-16400 and MIL-E-5400 standards for applications in government defense programs and in industrial environments. Input range is 98 to 130V ac and includes ac overvoltage and undervoltage protection. Operating temperature spans 0 to 71°C with no derating; noise, ripple, and spikes are <100 mV p-p. Other features include 30-msec holdup, remote sensing on all outputs, isolated outputs, and internal cooling. The 29-lb M7963 measures 5×17×8 in. including tubeaxial fan. $6700.

CEAG Electric Corp, 1324 Motor Parkway, Hauppauge, NY 11788. Phone (516) 582-4422.

Circle No 579



POWER SUPPLIES

System 1001 programmable power supplies suit ATE applications. The P-6 and P-12 power-supply programmers take instructions from your test-equipment controller, monitor the performance of the power supplies connected to them, and report problems. These IEEE-488 units can control as many as 12 independent, voltage-programmable dc power supplies, and they require only one bus address. The programmer controls the voltage, current, and voltage limit of each supply and can determine the value of the load-determined independent variable. A μC-based programmer replaces previously available power-supply programmers, and a built-in test-module adapter obviates peripheral hardware. A built-in test routine verifies that all system components are operational. During operation, a self test constantly monitors the status of each supply. Power requirements spec at 103.5 to 129V or 207 to 258V, 47 to 420 Hz,

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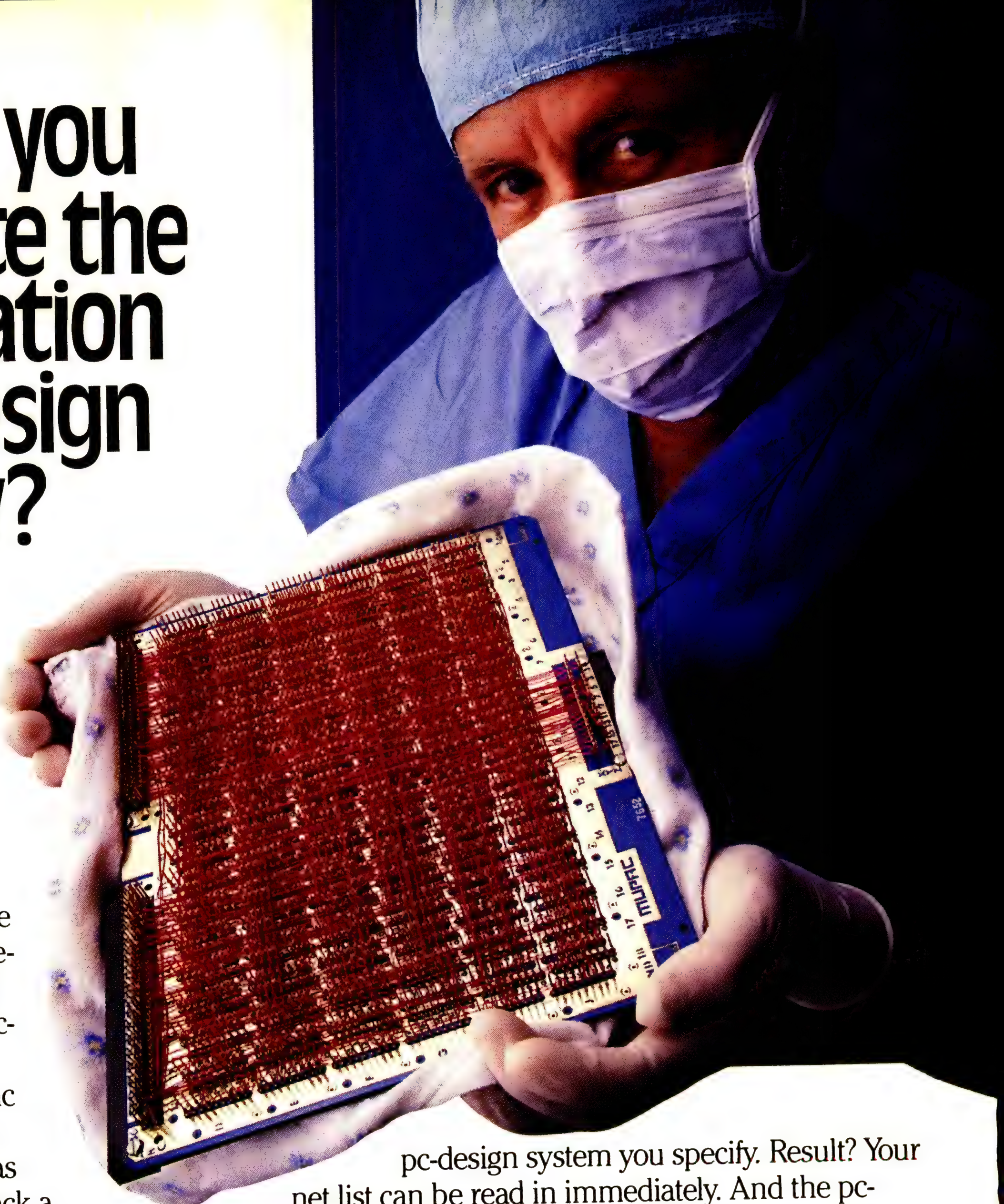

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All you have to do is come up with that new, beyond-the-state-of-the-art idea. The one destined to push back the horizons in electronic circuit design technology.

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Mid-Western Division—502 Morse Ave., Schaumburg, IL 60193/(312) 529-7690 Telex: 722474
European Division—In der Klinge 5 D-7100 Heilbronn, W. Germany (07131) 217 12 Telex: 841 728144
1-800-521-8008—Outside Massachusetts

CIRCLE NO 183

for both the P-6 and P-12; the P-6 specs 0.5A max and the P-12, 0.75A max. P-6 programmers, $2050; P-12 programmers, $2150.

Systron Donner, 2727 Systron Dr, Concord, CA 94518. Phone (415) 671-6637. TWX 910-481-9479.

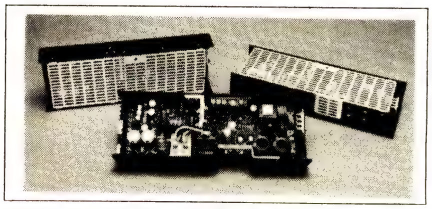
Circle No 580

LOW-COST SUPPLIES

This linear power-supply series, based on a split-bobbin transformer design, meets major international safety and emission standards. The E-Series consists of more than 30 models in the industry-standard open-frame package. They range from 6 to more than 140W, with as many as three outputs on the standard units. From $19.20 (100).

CurrenTechnology Corp, 135 Prestige Park Circle, East Hartford, CT 06108. Phone (203) 289-6831. TWX: 710-425-6063.

Circle No 581



MAG AMP SWITCHERS

The Mass 300 magnetic amplifier switchers are available in the six multioutput models that use proprietary magnetic-amplifier regulators. This type of regulation provides high instantaneous peak for inductive loads like disk drives without degrading other output's regulation. The main 5V output provides to 35A. All outputs are regulated. From $259 (OEM). Delivery, stock to 8 wks.

Elpac Power Systems, 3131 S Standard Ave, Santa Ana, CA 92705. Phone (714) 979-4440.

Circle No 582

65W SWITCHER

This switching power supply takes advantage of new control-circuitry technology and standardized design components. Model SX65 features a flyback design, appropriate for CRT monitors, Winchester or floppy-disk drives, printers, personal computers, and other low-power communications devices. Output ratings are 5V at 6A, 12V at 2.5A, −12V at 0.7A, and −5V at 0.7A. This switcher also offers pc-board mounting, quick-disconnect connectors, overvoltage protection, and automatic current-recovery protection. It meets VDE 730 and 871, IEC 380, UL 478, CSA C22.2 No 154, and FCC 20780 Subpart J Class A. Customization is available. $52 (OEM qty).

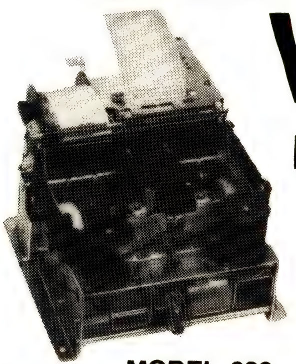
Summit Electronics Inc, 750 S Sherman, Richardson, TX 75081. Phone (214) 231-1456.

Circle No 583

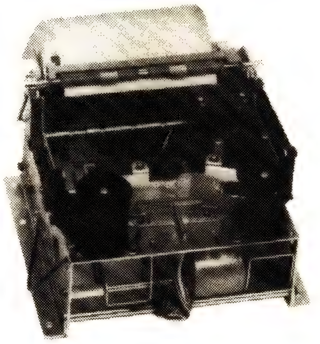
WESTREX

DOT MATRIX PRINTERS

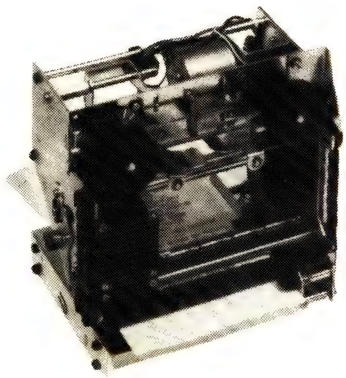
800 SERIES



MODEL 820
SPLIT PLATEN PRINTER
- Two independently controlled print stations
- Up to 46 character print line
- Receipt tear off
- Journal rewind
- Up to 5 lines per second receipt printing



MODEL 850
JOURNAL PRINTER
- 51 columns at 12 cpi.
- Rewind
- Tear-off available
- Adjustable paper width
- Paper low sensor and more



MODEL 840
SLIP/DOCUMENT PRINTER
- 40 columns at 12 cpi.
- Adjustable slip stop
- Top and bottom form sensors
- Side or front form insertion
- Optional programmable paper feed

WESTREX 800 Series of 150 character per second, alphanumeric bi-directional printers include split platen, flat bed slip/document and 51 column journal printers in a variety of standard models to suit many OEM applications. All utilize the same simple, reliable drive system, head position sensors, ribbon transport mechanism and other quality tested components for maximum cost effectiveness.

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WESTREX OEM PRODUCTS

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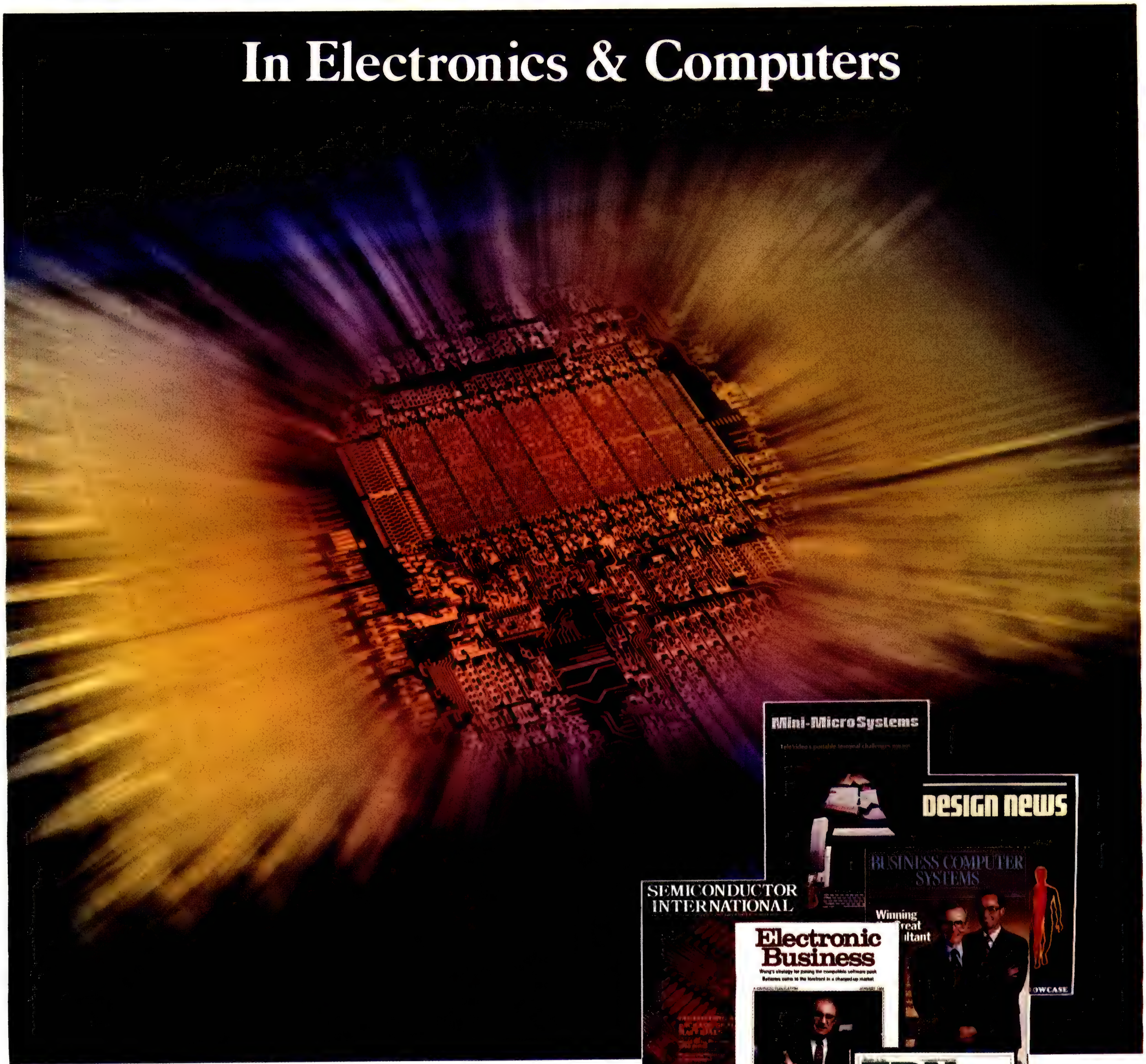
IN SWEDEN — WESTREX OEM PRODUCTS, Box 3503, S-17203 Sundbyberg, Sweden 46/8 + 981100 TELEX: 12139

CIRCLE NO 237

Cahners Means Business



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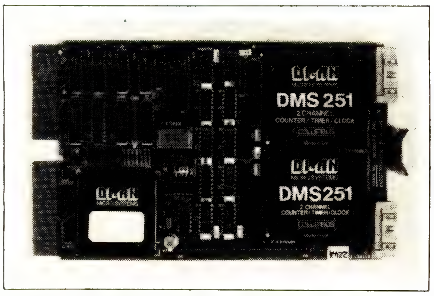


COUNTER/TIMER CARD

Compatible with LSI-11/2, 11/23, 11/73, and SBC-11/21 processors, the DMS511 interface card accepts two DMS251 plug-in timing modules, allowing you to add four counter/timer/clock channels to DEC Q-bus systems. Each module contains two independent 16-bit counters, which you can preload under software control, to provide up/down counting, pulse counting, frequency or time-interval measurement, and clock output functions at speeds as high as 1 MHz. You can cascade the two counters for 32-bit operation. External up/down control and gating inputs are provided, together with open-collector drivers which activate when the associated counter reaches a predefined count. Module command/status and data registers appear as four contiguous memory locations, which have a jumper-link selectable base address. Supporting the 4-level interrupt structure of the LSI-11/23, you can also software program the board's vector address. For 8-channel operation, the DMS512 expansion board accepts two further counter/timer modules. DMS511, £155; DMS512, £95; DMS251 modules, £130.

Di-An Micro Systems Ltd, Mersey House, Battersea Rd, Heaton Mersey, Stockport, Cheshire SK4 3EA, UK. Phone 061 442 9786. TLX 669592.

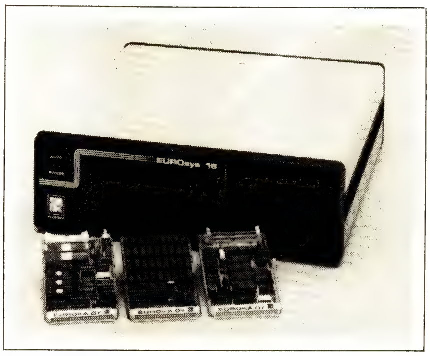
Circle No 584

TRACKERBALL

Targeted at low-cost CAD/CAM applications, the RB2/CAD cursor-control trackerball features a freely rotating 2¼-in. ball and three user-definable pushbutton functions. For the X and Y axis, the unit outputs TTL-level pulse trains, which are quadrature encoded to indicate the degree and direction of ball rotation. Resolution is 200±5% pulses/revolution in either axis. The tracking force on the surface of the ball measures approximately 30g. An optional RS-232C interface can be incorporated into the trackerball housing. Operating over 5 to 45°C, the unit draws 75 mA from a 5V supply. A lower cost version, the RB2/PC-1, is targeted at the consumer-computer market and is supplied complete with software drivers for the BBC microcomputer. RB2/CAD, £78; RB2/PC-1, £59.50.

Marconi Electronic Devices Ltd, Power Div, Carholme Rd, Lincoln LN1 1SG, UK. Phone (0522) 29992. TLX 56163. In US, 160 Smith St, Farmingdale, NY 11735. Phone (516) 293-8686.

Circle No 585



DEVELOPMENT SYSTEM

EUROsys 16 runs the OS-9/68000 operating system to provide multiuser program-development capabilities. It incorporates a 68008 processor, 256k bytes of RAM, a 20M-byte Winchester drive, and a 500k-byte floppy-disk drive. Interfaces include four RS-232C ports, 28-line parallel I/O, SASI, and a QIC-02 to tape streamers. For target system expansion, the 19-in. frame has 13 free slots, which can accommodate single-Eurocard EURO-6/16 or compatible modules. Approximately Fin markka 48,000.

Euroka Oy, Hameentie 155 C 52a, 00560 Helsinki 56, Finland. Phone (90) 799522. TLX 125490.

Circle No 586

TERMINAL

First in a planned series of terminals, the j100 features 32k bytes of internal RAM, 16k or 32k bytes of ROM, and a separate 8k×16-bit display memory, which does not encroach on its Z80 processor's address space. Using a 16×16-pixel character cell, the terminal displays 30 lines of 80 characters, but you can reconfigure the number of TV lines used to make up the character height and thereby vary the number of character lines displayed. Character attributes include hide, low intensity, inverse video, underline, and blink. The standard character generator provides 128 characters, but an optional 256-character version is available. Interfaces include RS-232C, RS-422A plus auxiliary and printer RS-232C ports. The terminal supports synchronous or asynchronous, bit- or byte-oriented protocols. Baud rates are programmable in the 50- to 19,200-baud range. Approximately £600 (500).

Lynwood Scientific Developments Ltd, Park House, The High St, Alton, Hants GU34 1EN, UK. Phone (0420) 87024. TLX 858811.

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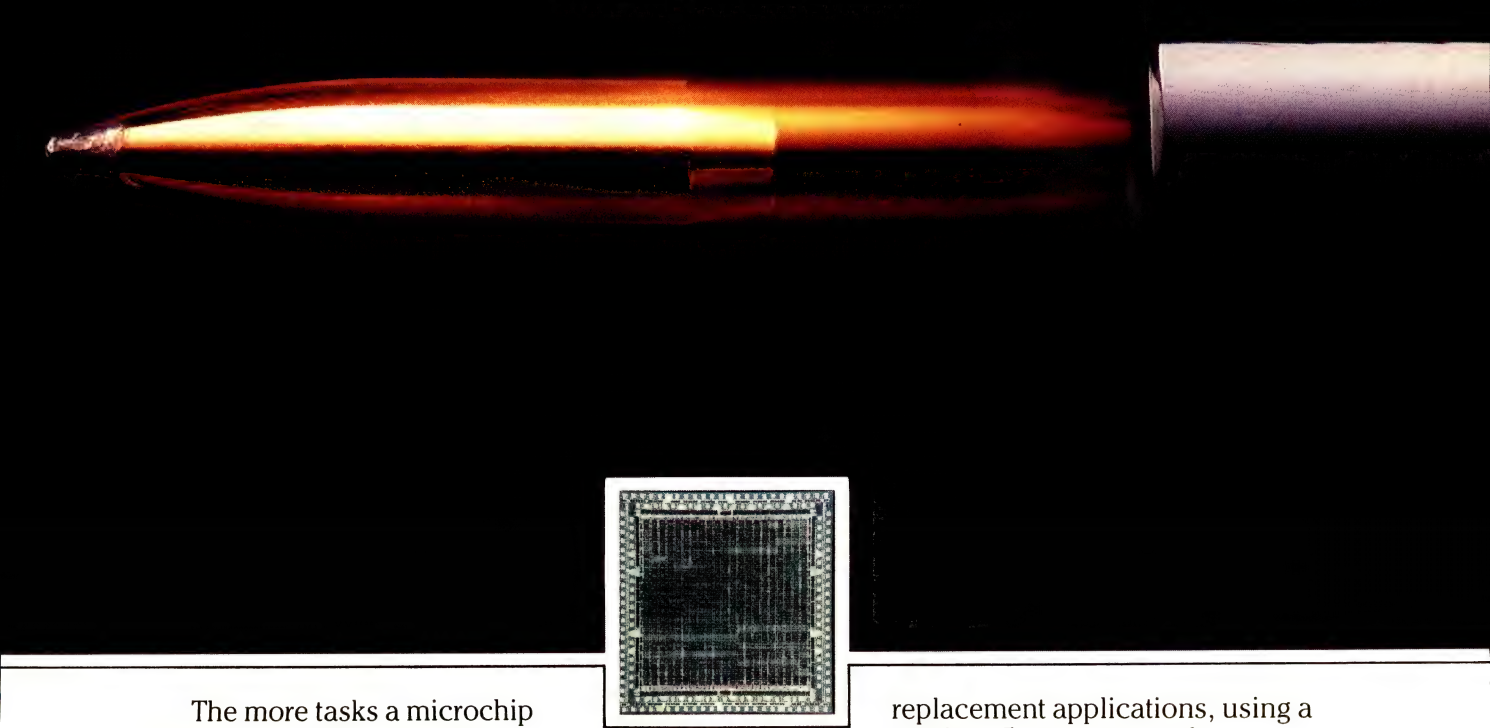

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The Honeywell Digital Product Center, 1150 East Cheyenne Mountain Blvd., Colorado Springs, Colorado 80906. 1-800-328-5111, extension #3402. (In Minnesota, call 1-612-870-2142, extension #3402.)

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NETWORK ANALYSIS

NETAZNS is a linear network-analysis program that runs under CP/M or CP/M-86. The program handles both passive and active network elements and can do transmission-line analysis. You input each element in the network by assigning a node number and a component type. The allowed component types are resistor, capacitor, inductor, transmission line, shortened stub, open stub, op amp, beta generator, and transconductance generator. The program's output is a frequency sweep of the network. You can specify the output voltage for any node. An option allows you to print out a plot of the magnitude and phase of the node voltage vs frequency. You can modify any circuit element and rerun the analysis with the original frequencies. The program requires 15k bytes of RAM. $30.

Kask Labs, 1207 E Secretariat Dr, Tempe, Az 85284. Phone (602) 831-1420.

Circle No 588

SOLIDS MODELING

The Polycad/10 solids-modeling system runs on the IBM PC and uses optimizing algorithms that, according to the manufacturer, allow the system to outperform high-end CAD systems and VAXs. The software allows you to create 3-D, shaded-surface, full-color (4096 from a palette of 16.8 million) models using the IBM PC or PC-compatible systems and a 512×512-pixel display and frame buffer. Three hundred menu commands allow you to rotate, scale, duplicate, and combine models. The program also allows you to alter a light source's direction, smooth jagged lines using antialiasing, and choose between orthogonal and perspective projections. The software allows you to record animated sequences automatically, rather than force you to supervise the process frame by frame. By adding contact-closure relays to the system's mother board, cameras and video recorders are placed under video control. $11,900.

Cubicomp Corp, 3165 Adeline St, Berkeley, CA 94703. Phone (415) 540-5733.

Circle No 589

μP DEVELOPMENT

Uniware is a μP development tool kit that runs under Unix. The kit contains a macro preprocessor, a linking loader, an archiver, and several formatters. The macro preprocessor features file inclusion with search paths and nesting, macros with nested definitions and calls, positional or named formal parameters, textual variables (similar to the Unix shell variables) with arbitrary-length names and recursive invocations, substring extraction from any textual variable, and two types of For loops. The cross assemblers support most major μPs and feature fully relocatable object code, macros, conditional assembly, optional assembly listing, symbol tables of unlimited size, and symbol names of arbitrary length. The link editor features arbitrary-length external symbol names, mixed object code, archive library files, and a C-like link-specification language that allows you to define your load map once it's in a central file, define and use symbols in arithmetic expressions, and create links among overlays. $3000 with VAX 780 host. $2000 with VAX 750 host. $800 to $1200 for each cross assembler.

Nuvatec Inc, Uniware Div, 3110 Woodcreek Dr, Downers Grove, IL 60515. Phone (312) 971-8500.

Circle No 590

ON-CHIP INTERPRETER

The MCS BASIC-52 package is a version of the Intel 8052 microcontroller that houses a BASIC interpreter in 8k bytes of on-board ROM. The package includes 8-digit floating-point arithmetic, an EPROM and EEPROM programmer, and a user-accessible function library. You can store as many as 225 programs in the EPROM/EEPROM. For faster execution, you can also store assembly code in the on-chip memory. The manufacturer claims that the BASIC interpreter is 2.5 to 10 times faster than Tiny BASIC. The system can automatically execute a program upon reset or turn it on without human intervention. You can control the built-in hardware clock via software. $45 (1000).

Intel Corp, 5000 W Williams Field Rd, Chandler, AZ 85224. Phone (602) 961-2756.

Circle No 591

INVERSE FFT TUTOR

The IFFT is a tutorial program for the inverse fast Fourier transform that runs on any Apple computer with 48k bytes of user memory. The program is broken into two parts. The first part deals with the theory of the fast Fourier transform, the discrete Fourier transform, and frequency-domain filtering. Examples are provided throughout. The software also contains a subroutine which shows the distortion of serial transmissions (NRZ, for example) by a telephone line. You specify the length of the line and the baud rate, and the program graphically displays the distorted bit pattern. The software also displays the eye patterns that are often used to evaluate such transmission lines. The second part of the program shows you how to run the program for evaluating Fourier transforms. You can specify the sampling rate, as many as 128 points and as many as 64 harmonics. You can also manually specify the filter or use a pole/zero description. You can use real and imaginary coefficients. $29.95.

Dynacomp Inc, 1427 Monroe Ave, Rochester, NY 14618. Phone (716) 442-8960.

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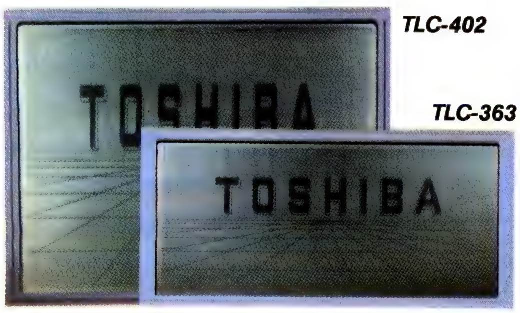

Specifications

		TLC-402	TLC-363
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W×H×D)		274.8×240.6×15.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		–20 – 70°C	–20 – 70°C
Operating Temperature		0 – 50°C	0 – 50°C
Supply Voltage	V_{DD}	7 V	7 V
	V_{DD}-V_{EE}	18 V	18 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5 ±0.25 V	5 ±0.25 V
	V_{EE}	–13 V Max.	–13 V Max.
Input Voltage	High	4.0 V Min.	4.0 V Min.
	Low	0.5 V Max.	0.5 V Max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		5	5
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

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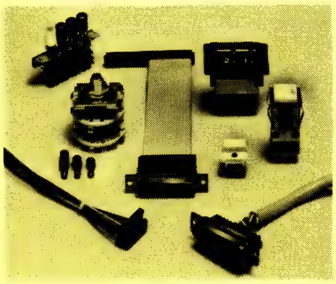

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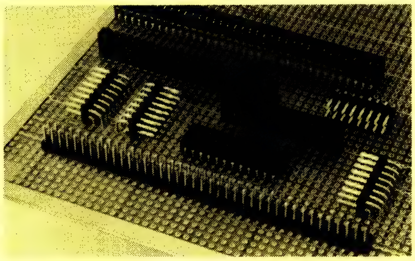

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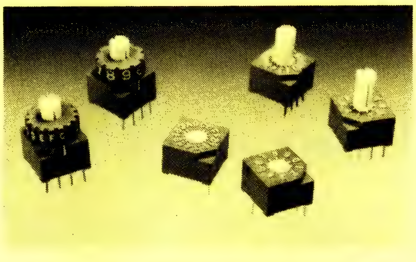

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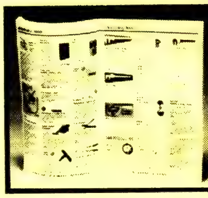

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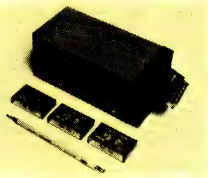

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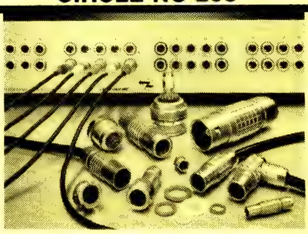

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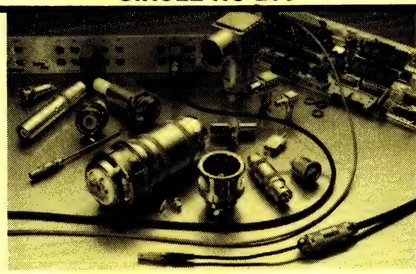

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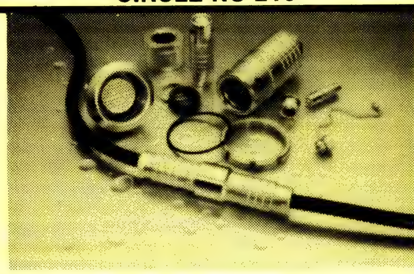

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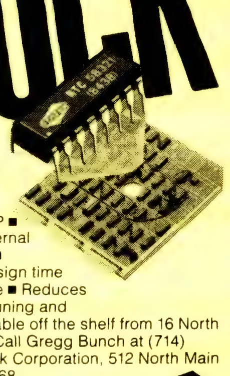

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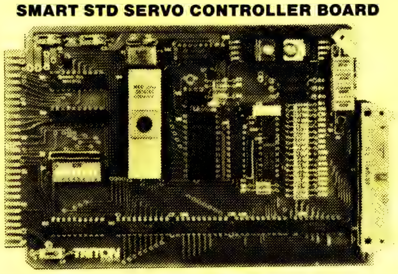

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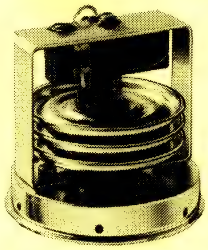

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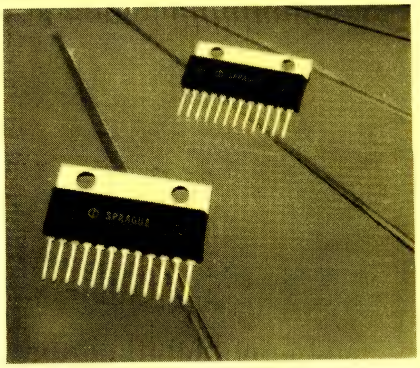

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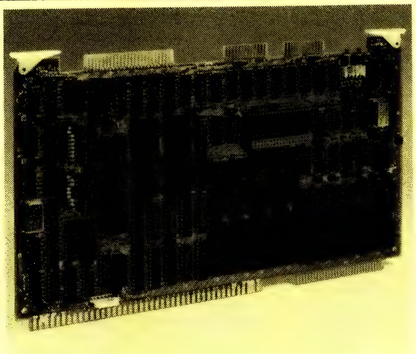

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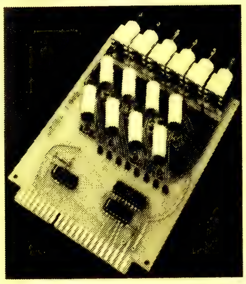

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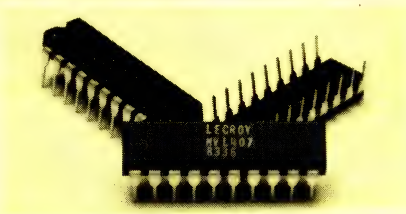

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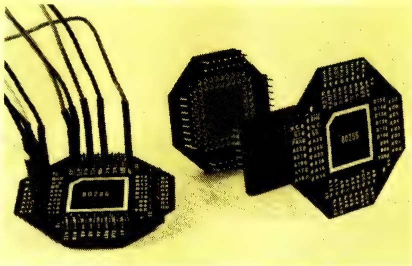

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The BUG CATCHER II™ offers the first reliable method for debugging software and hardware for your iAPX186/286, 68000/68010 and new 68020 PGA packages. The fully labeled overlay plate complete with the mnemonics for your processor, eliminates counting pins. BUG CATCHER™ is also available for popular circuits packaged in 40, 48, or 64 pin dual-in-line pkgs. **EMULATION TECHNOLOGY, INC.,** 422 Ives Terrace, Sunnyvale, CA 94087 (415) 960-0652

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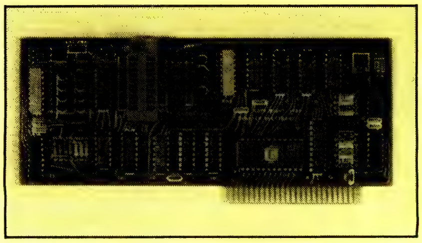

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PALP-701 is an Apple II computer plug-in card. It is designed to read, program, verify and verify-protect* the 20-Pin series PALs. A screen editor is built in for the PAL logic pattern editing. $225.00 each. Add $3.00 for shipping and handling. Manual only, $5.00 each.

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*An external 19 Volt power supply is required for verify-protect.
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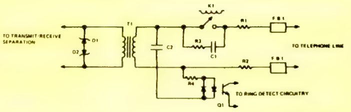

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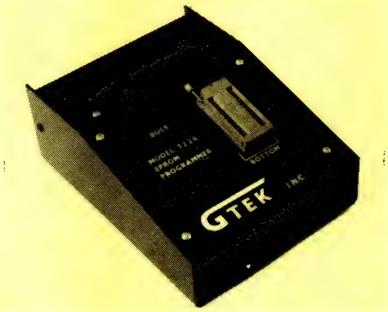

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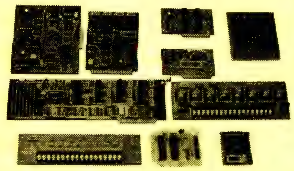

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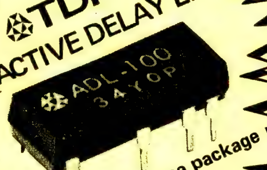

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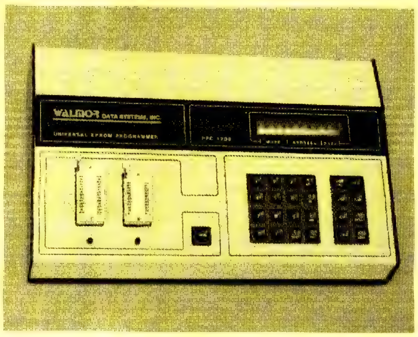

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Microwave products described

This 6-pg, illustrated brochure describes the company's components, instruments, and subsystems that operate at millimeter and submillimeter wavelengths. Products covered include multipliers, swept multiplied sources, mixer/detectors, FET amplifiers, Gaussian optic components, Cassegrain antennas, scalar feedhorns, tunable submillimeter spectrometers, radiometer backends, and noise-figure meters. Accounts of typical specifications and applications complete the treatment.

Millitech Corp, Box 109, South Deerfield, MA 01373.

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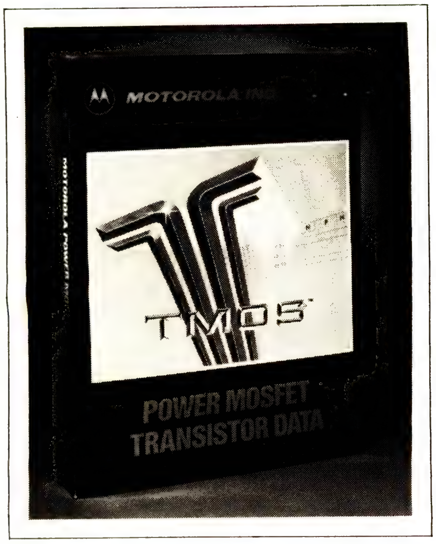

Manual for power MOSFETs

This data manual (DL 135) is intended to give users of power MOSFETs basic description and application information on the firm's TMOS products, which are available in 11 package configurations. Included are theory applications, selector guides, data sheets, and a cross-reference index for more than 300 standard devices. Chips for hybrid circuits on all the products in the book are also presented. A glossary of terms, symbols, and definitions common to power MOSFETs, as well as a section on small-signal TMOS devices, are included. $2.25 (25).

Motorola Semiconductor Products Inc, Box 20924, Phoenix, AZ 85036.

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Guide to fiber-optic products

This data sheet describes specifications for the manufacturer's fiber-optic emitters, receivers, and detectors; photoemitters; photodetectors; optocouplers; slotted optocouplers; and LEDs. There is also one page of dimensional drawings.

Aborn Electronics, Franciscan Business Park, 3675 Enochs St, Santa Clara, CA 95051.

Circle No 594

Reference card for electronic circuits

Micro Chart #10, entitled "Active Electronic Components," is a 2-sided, 2-color, 8½×11 plastic reference card that provides you with the basic information needed when designing or repairing circuits. Some devices that are referenced include transistors, thyristors, light emitters and receivers, voltage followers and regulators, diodes, A/D and D/A converters, op amps, multipliers, and optocouplers. Typical descriptions give part names, signal names, details of operation, and examples of key specification parameters. $6.95.

Micro Logic Corp, Box 174, Hackensack, NJ 07602.

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Primer for PCM and T-1 carrier devices

This publication is suited for design engineers using the manufacturer's T-1 carrier devices and pulse-code modulation (PCM) techniques. The primer describes the advantages of PCM and cites specific application examples to illustrate the T-1 devices' capabilities. The company's T-1 carrier system, comprising the T-1 8040 3-port memory, 8050 serial transmitter, and 8060 serial receiver, is discusssed.

Rockwell International Corp, Semiconductor Products Div, Box C, MS 501-300, Newport Beach, CA 92658.

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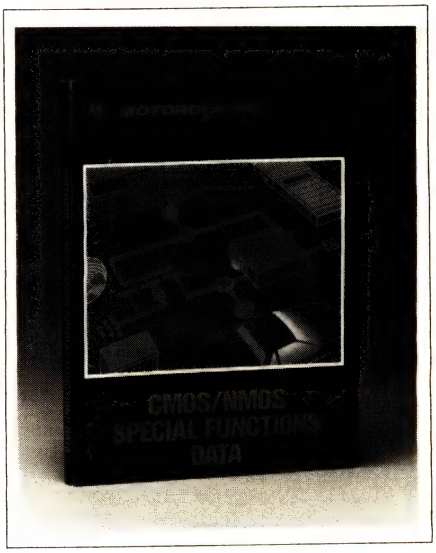

CMOS/NMOS data manual

A compilation of product specification and application information, this book (No DL130) covers more than 60 special-function VLSI ICs offered by the company. Data sheets provide complete specifications for the individual circuits. The catalog consists of 11 chapters, including separate chapters for different device families (ie, CMOS A/D and D/A converters, CMOS decoder/display drivers, CMOS op amp/comparators, CMOS/NMOS PLL/frequency synthesizers, and CMOS remote-control functions and smoke detectors). Such topics as pin connections (including diagrams), testing information, and electrical characteristics are covered. $1.20 (25).

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INQUIRE DIRECT

Rotate printouts 90°; reduce cutting and gluing

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If you're lucky enough, at least once in your life you'll encounter an inexpensive software program that's useful, easy to use, and adequately documented. Sideways is such a program. It commands your dot-matrix printer to print text files at a 90° angle to their normal orientation—to wit, *sideways*.

Printing something sideways is a useful function. Consider, for example, a 50-row spreadsheet that contains 30 columns of data, with each column 12 characters wide. If your spreadsheet and the word processor used to format the sheet's text are configured for 80 characters max, you'll obtain five sheets from the printer; you'll then have to trim, align, and glue those sheets to complete the spreadsheet.

With Sideways, your printer will print the foregoing spreadsheet in one pass, thereby eliminating the gluing. You simply configure the spreadheet's character-count parameter for a number of characters that's greater than that of the sheet's longest row. If the maximum allowed character count is less than the width of your spreadsheet, an option called glue lines lets Sideways ignore the spreadsheet's page sectioning. Simply set the glue lines option to the number of the bottommost row in the spreadsheet.

Fig 1 shows a spreadsheet printed under the command of Sideways. The sheet contains 17 columns and 69 rows; the longest row contains 288 characters. With the font style chosen (normal), Sideways permits the printer to print 53 lines before issuing a form feed and then printing the remaining 16 lines. The broken line ("glue line") does not represent printed characters; it's inserted in **Fig 1** for clarity.

The program is friendly—upon

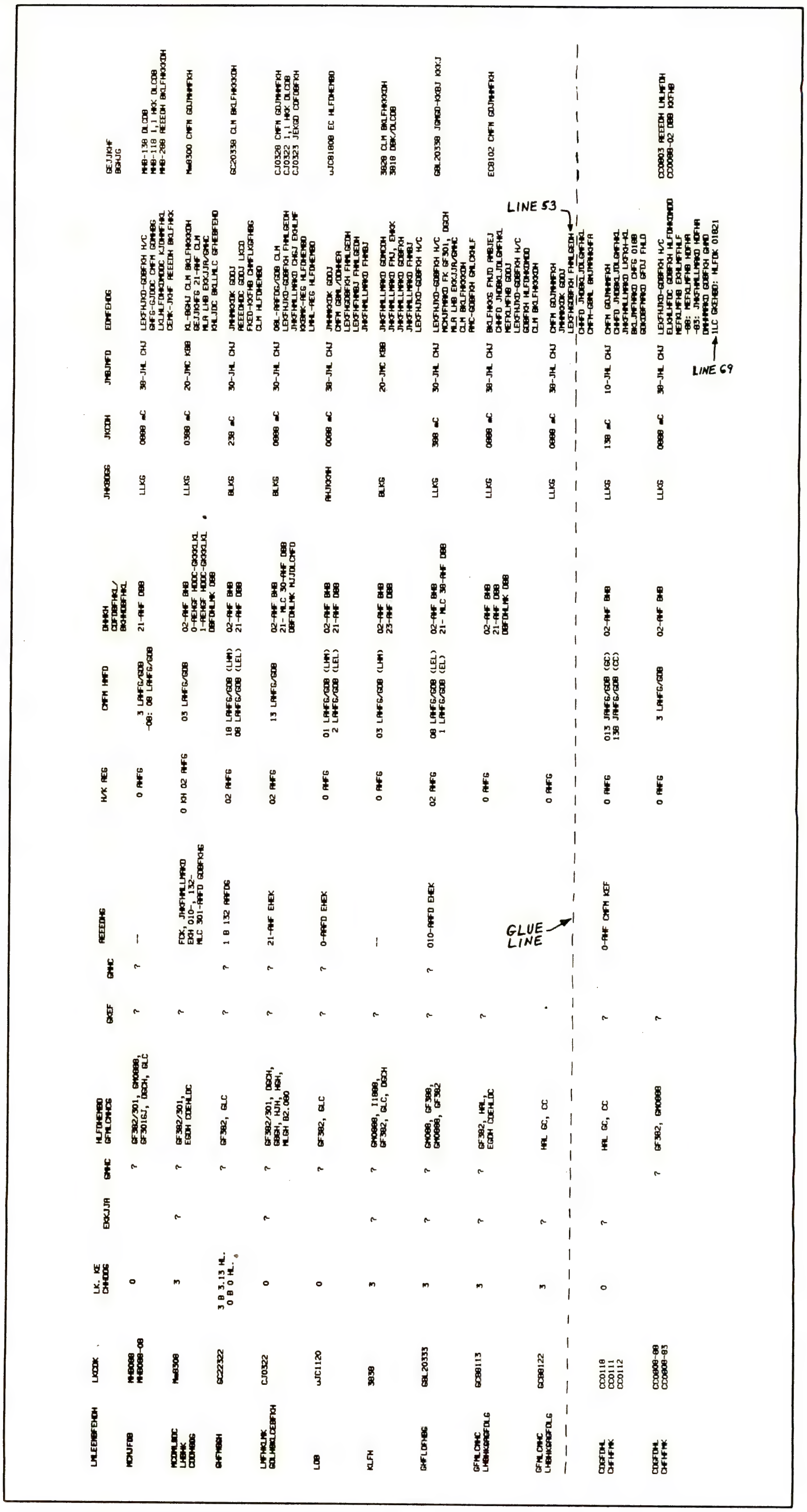

***Fig 1—Reduce cutting and gluing** with Sideways. It's easy to use with an IBM PC or Apple, and it commands most popular dot-matrix printers. The sheet shown here required one easy gluing operation; without the program, you'd need to cut, align, and glue four sheets.*

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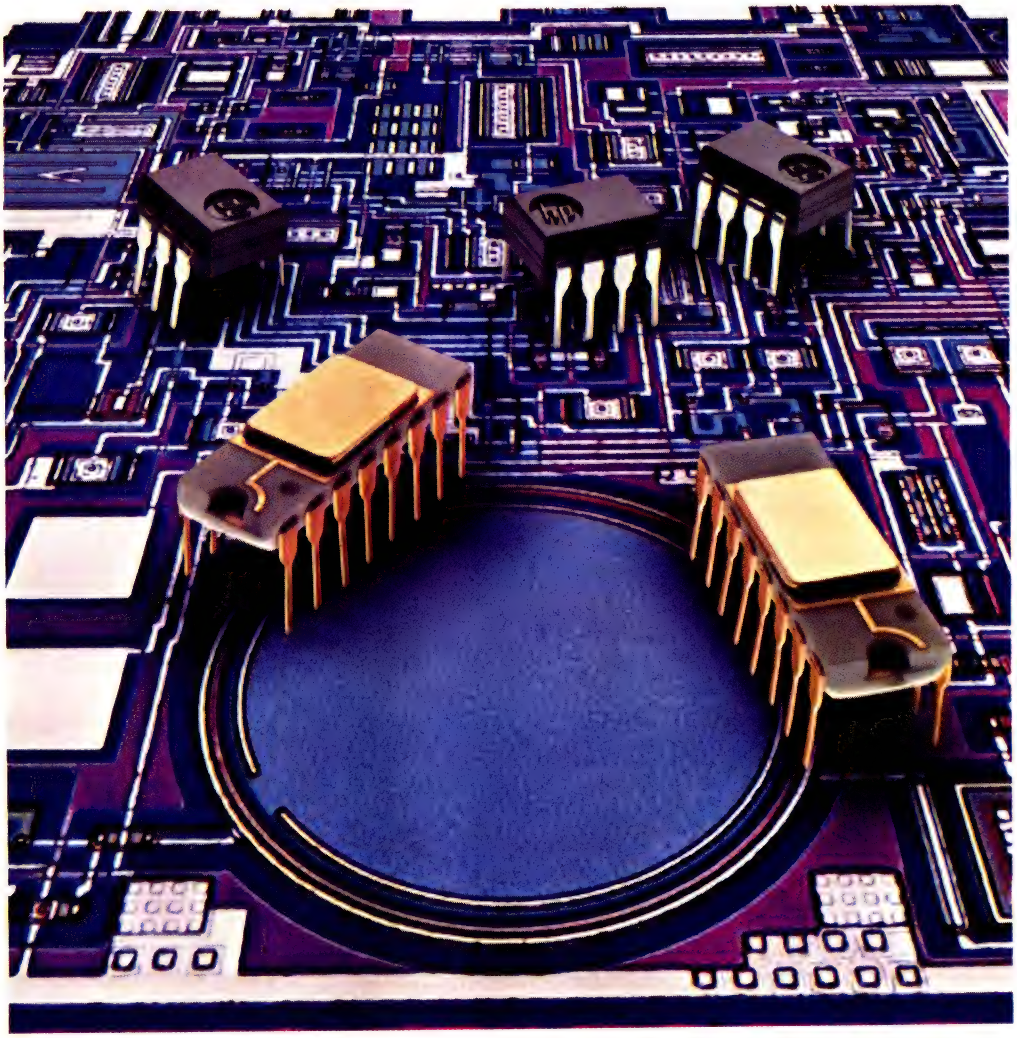

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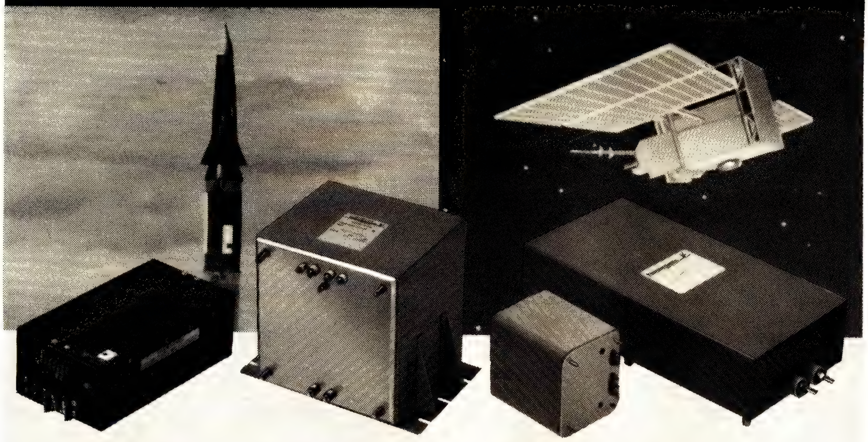

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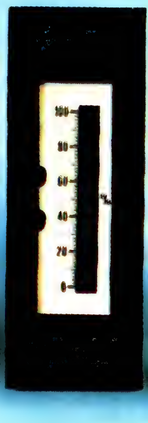

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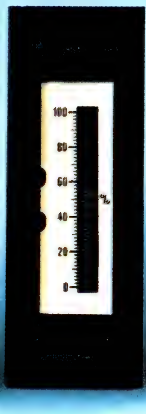

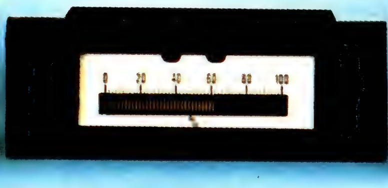

8025

CIRCLE NO 197

start-up, a menu allows you to set up paper size, character weight (the sheet in **Fig 1** uses the double-strike, boldface option), character font, left and top margins, and the glue-line parameter. Six character fonts are available, ranging from tiny to extra large. Based on the character font you choose, Sideways automatically adjusts the number of lines per page.

The program is available for the IBM PC and compatibles and the Apple II Series. The publisher plans to introduce versions for the Wang personal computer and the TI Professional. Sideways accommodates the following printers: IBM Graphics Printer, Epson MX-80/100 and FX-80/100, Okidata Microline 82A/83A/84/92/93, C Itoh Prowriter, and IDS printers including Prism 80/132, Micro Prism, and IDS 460/560. In addition, the publisher provides information for using a Star Micronics Gemini 10X, Printronix MVP 150B, and TI 850 or 855. For example, a Debug program makes the TI printers emulate an IBM Graphics Printer.—***Bill Travis***

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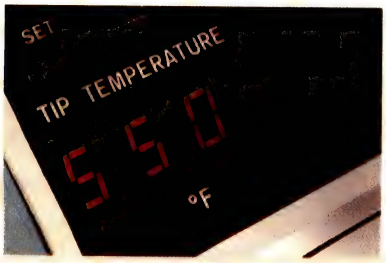

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CIRCLE NO 174

WRITTEN AND EDITED BY DEBORAH ASBRAND

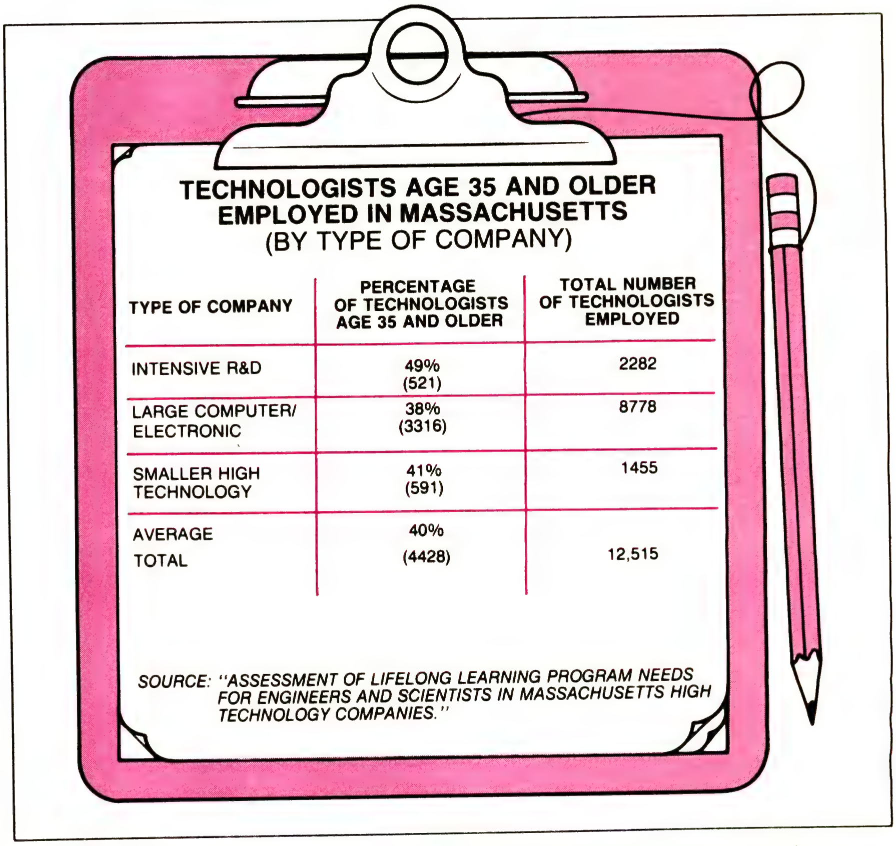
Studies explore continuing education for engineers 35 years and older

The high-technology industry has always been characterized by its youthful community. The success stories of young entrepreneurs who guided basement businesses into million-dollar corporations almost always costarred a young engineering staff that worked late into the night applying new technologies into highly marketable products.

But accompanying the industry's expansion and success is a problem that has grown to large proportions. As technology becomes increasingly sophisticated, many engineers are discovering the large gap that exists between what they learned in college and what continually evolving technologies are demanding.

Obsolescence among electrical engineers is a problem that has always existed but has only recently begun to receive widespread attention. However, even as far back as the 1960s, a report by the state of California warned that the changing face of technology would require a shift in the traditional structure of engineering education, with more emphasis on continuing education.

But as the percentage of engineers over the age of 40 continues to grow, the problem becomes more acute. Researchers at Northeastern University (Boston, MA) found that 40% of surveyed engineers and scientists in Massachusetts high-technology companies were reported to be 35 or older. Research and development companies employed the largest percentage of engineers and scientists in this age bracket with 49%. Large computer/electronic companies and smaller high-technology companies reported that 38% and 41% of their technical staffs were in the 35-and-older age group, respectively.



TECHNOLOGISTS AGE 35 AND OLDER EMPLOYED IN MASSACHUSETTS
(BY TYPE OF COMPANY)

TYPE OF COMPANY	PERCENTAGE OF TECHNOLOGISTS AGE 35 AND OLDER	TOTAL NUMBER OF TECHNOLOGISTS EMPLOYED
INTENSIVE R&D	49% (521)	2282
LARGE COMPUTER/ ELECTRONIC	38% (3316)	8778
SMALLER HIGH TECHNOLOGY	41% (591)	1455
AVERAGE	40%	
TOTAL	(4428)	12,515

SOURCE: "ASSESSMENT OF LIFELONG LEARNING PROGRAM NEEDS FOR ENGINEERS AND SCIENTISTS IN MASSACHUSETTS HIGH TECHNOLOGY COMPANIES."

The 14 companies surveyed employ nearly 13,000 engineers and scientists. All were members of the Massachusetts High Technology Council (MHTC), which sponsored the survey and chose the participating companies as representative of the MHTC's 160 member companies. "It's becoming more and more clear that in order to have any realistic chance of capitalizing on new ideas and successfully implementing them, engineers have to be far more up to date," says MHTC president Howard Foley. "The focus on lifelong education has become much more important than we realized."

Researcher Glenn Pierce, associate director of Northeastern University's Center for Applied Social Research, credits the MHTC for its willingness to examine the problems that might exist and for organizing a 2-day conference on the topic. He and Paula Leventman, assistant dean at Northeastern's College of Engineering, conducted the research. Although Leventman has studied engineering careers for 10 years, she was still surprised by the large percentage of technical employees age 35 and older at the companies surveyed. "You think of [engineering] as a young person's field. That was true 10 years ago, but those people are now 10 years older," says Leventman. "If they haven't kept up with the changes, they need some catching up."

In a study she did for Digital Equipment Corp (Maynard, MA) several years ago, Leventman found that engineering managers typically rate engineers as most productive

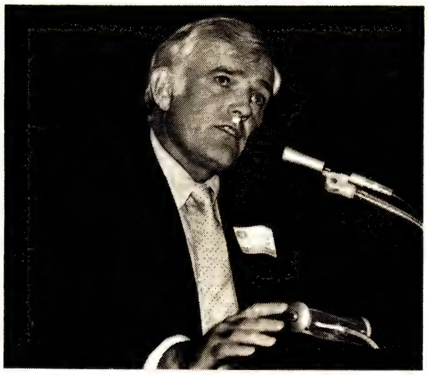
when they're in their early thirties, and that engineers rate themselves as most productive in their late thirties. Yet the most technically difficult tasks, Leventman's study found, were being given to engineers in their twenties.

A first step in examining the effects that obsolescence of engineers can have on a company is to survey the engineering staff—a task few companies have undertaken. Leventman and Pierce were surprised that most of the companies they studied didn't have a breakdown of engineers' continuing education activities by age. "We haven't realized how important education is," Pierce says, which is why educational data traditionally has not been kept on employees.

Neither Leventman nor Pierce knows of any companies that have taken the responsibility to track their employees' educational backgrounds. "There are no ongoing monitoring systems that are regularly measuring where each and every scientist is in terms of the programs they're taking or programs they should be taking, where they are in terms of their technical requirements, or where they may be going in terms of their technical requirements," says Pierce.

Innovative managerial policies for engineers, as well as continuing-education programs, have long been advocated by academic researchers. Technically oriented people in engineering-based staff positions, although well paid, were found to be the least satisfied with their jobs in a study of MIT alumni from the classes of 1951, 1955, and 1959. Many of the engineers surveyed at mid-career found themselves performing unfulfilling work that no longer challenged their technical talents, according to MIT management professor Lotte Bailyn, who conducted the study.

"We at companies need to do a lot more," says Delfine Thorndike, director of technical training at Digital Equipment Corp. Not everyone can take time away from their jobs to do the necessary reading and studying required to stay up to date. Thorndike says that in the past, some engineers whose skills weren't up to par drifted into managerial positions—a solution she hopes to avoid. "It's not what we want to do with our good engineers," she says.



Massachusetts High Technology Council president Howard Foley *says that a company's ability to act on new ideas and put them into action depends on a strong engineering staff.*

Northeastern University (Boston, MA) researcher Paula Leventman conducted a survey with colleague Glenn Pierce *for the Massachusetts High Technology Council that revealed 40% of the technologists in the companies studied are 35 and older.*

Preventive maintenance is the key to reducing obsolescence, most industry observers agree. Managers need to schedule time for their engineers to keep their technical skills sharp and intact, just as they schedule down time for machinery repair and maintainence. "Obsolescence is a problem that shouldn't exist," says Leventman.

Understanding the importance of continuing education is just the first step, says MIT engineering professor Louis Smullin, one of four authors of a 1982 study called *Lifelong Continuing Education.* The study, presented at a symposium marking the centennary of MIT's electrical engineering department, reported that a 4-year college education is no longer an adequate foundation for a lifetime career in engineering. In addition, simply replacing older engineers with new graduates won't sustain the industry's need for up-to-date engineers, the study reported. The industry is paying attention to such results as these—MIT has received thousands of requests for copies of the report.

Smullin believes that companies that are serious about continuing education need to devote financial and human resources to the effort. Pointing to the report done by the state of California in the 1960s, Smullin says continuing education and preventing obsolescence might be ideas whose time has finally come. "The same ideas keep resurfacing—maybe now is the time when something can be done."

Some companies have taken the first steps, allowing engineers to take as many as five weeks off each year for training. Although continuing education was once looked upon as part of a benefits package to attract and keep the best engineers, Thorndike says this condition has changed. Continuing education and obsolescence prevention are no longer a matter of competition, says Thorndike, but a matter of survival.

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Reference

Katz, R, "Trained as Engineers: Issues for the Management of Technical Personnel in Midcareer," *Career Issues in Human Resource Management*, Prentice-Hall Inc, Englewood Cliffs, NJ, 1982.

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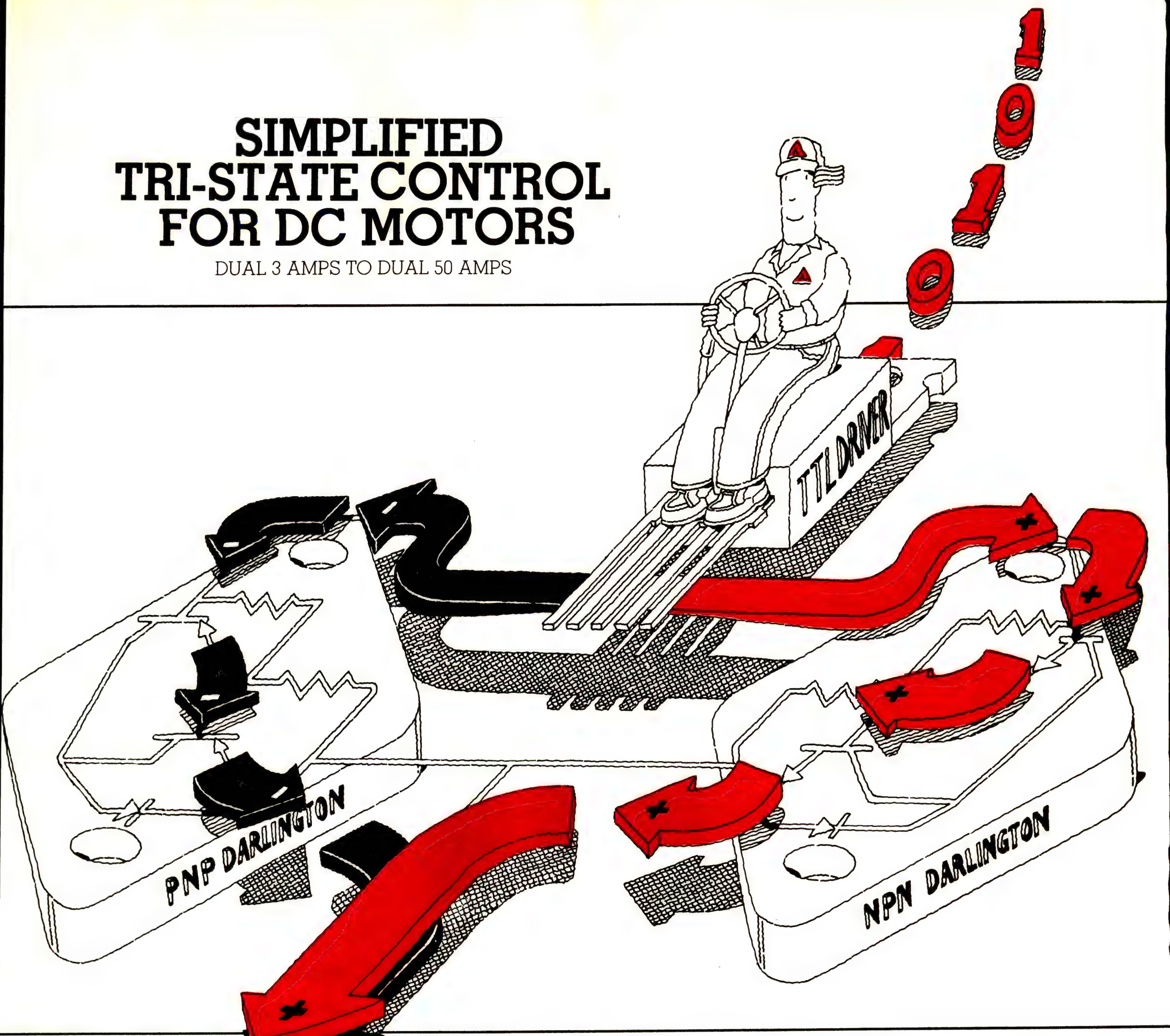

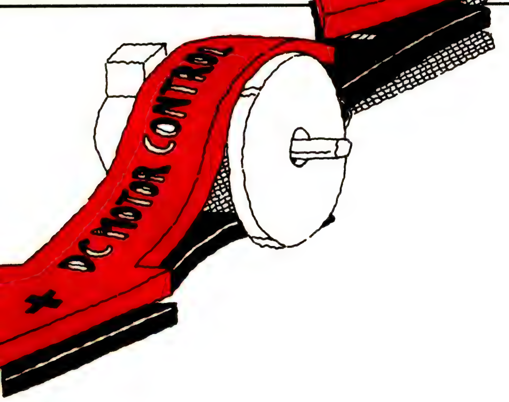

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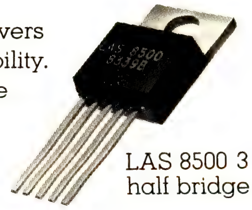

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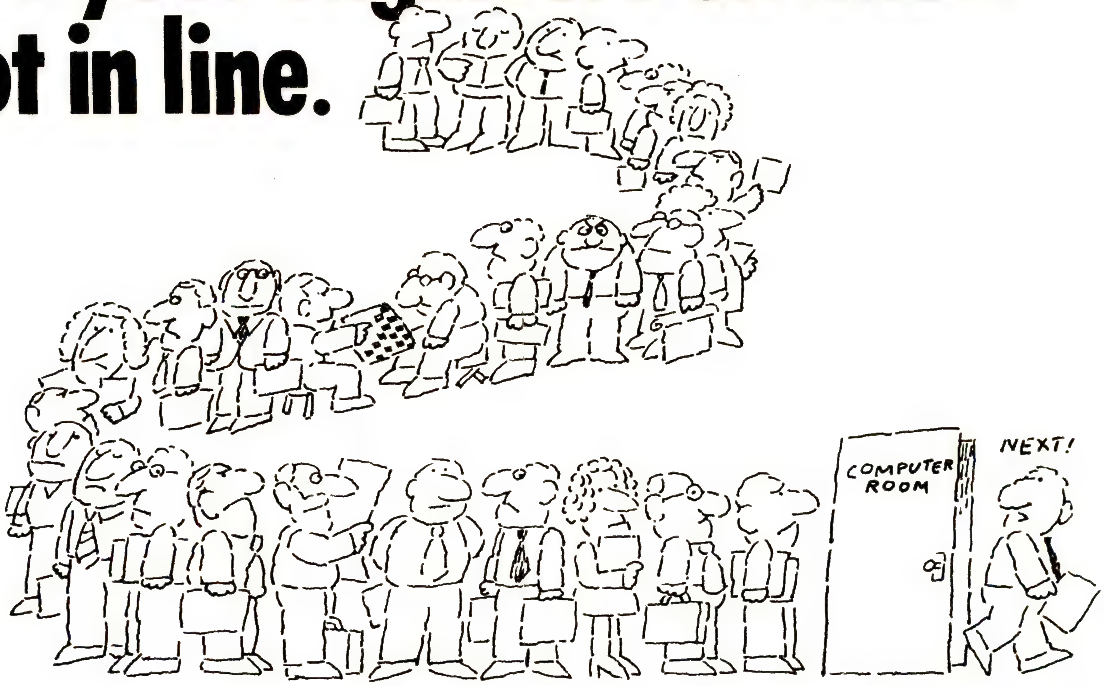

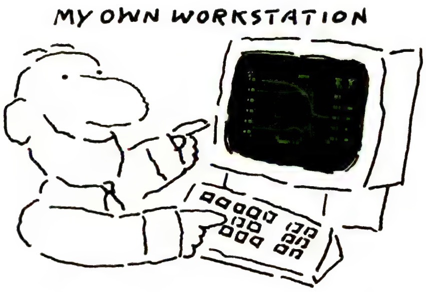

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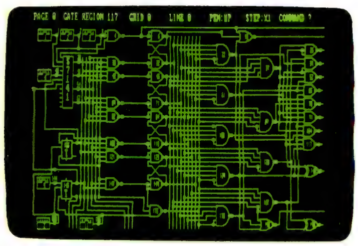

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A business without proprietary clout can still protect its software programs

H Newcomb Morse, JD,
Pepperdine University, Malibu, CA

A business with no proprietary stake over its computer programs can still find protection for the time and financial investment it has made in the programs and their importance to the company. The laws governing the use of computers are often unclear (see EDN, "A Question of Law," December 13, 1984, pg 383), but the basic laws of business still apply.

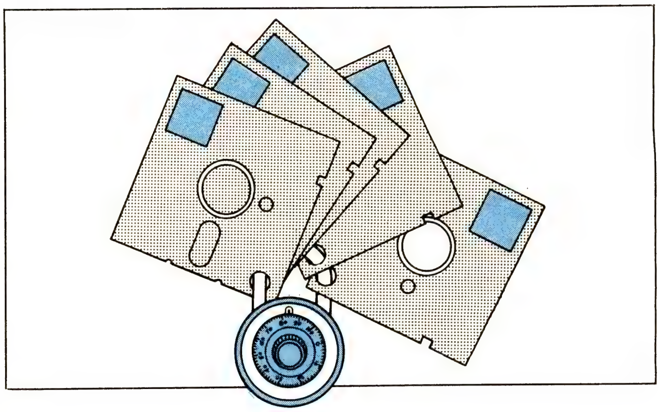
To protect the computer programs that were an integral part of its business, Computer Print Systems Inc brought suit against David A Lewis, Victor S Liss, and CPC Associates Inc for conversion of what Computer Print Systems claimed were its own computer programs, and for conspiring to usurp a corporate opportunity. The company, which filed the suit in the Court of Common Pleas, Bucks County, PA, also sought a preliminary injunction restraining the three defendants from using the computer programs.

Computer Print Systems is a data-processing service that develops computer programs for direct-mail advertising. David Lewis served as administrative manager and vice president of the company from May 1973 until January 1975, and thereafter as president until May 7, 1976.

From 1973 until 1976, Lewis was actively involved in the daily operations of Computer Print Systems. He exclusively managed the account of CPC Associates, one of the company's clients. Part of his job was to process CPC's monthly mailings using specialized computer programs.

CPC Associates had its own clients, which were a number of department and specialty stores in different areas of the country. CPC purchased subscription lists, which Computer Print Systems manipulated to identify subscribers who had recently moved to areas near its client stores. They constructed mailing lists and sent promotional literature from the stores to the people on the lists.

Victor Liss, CPC's president and a principal shareholder in the company, testified that it was important to CPC's clients that the mailings be generated as soon as possible after the potential customers' names were gathered. The stores' strategy was to identify new customers early and make contact with them before they established shopping habits—and, more important, before competing stores made contact with them.



To accommodate CPC's schedule, Computer Print Systems established a rigid timetable for CPC's monthly mailings. The company also developed programs to process the CPC account, testified Kurt Schneider, the sole shareholder of Computer Print Systems. Schneider testified that an "unduplicating" program, which prevented duplicate mailings to individuals who subscribed to more than one magazine, and a zip-code program, which identified persons who lived within a particular zip-code district, had been developed for the CPC account.

In January 1975, Lewis requested permission to make copies of the computer programs used for the CPC account and store them at CPC as a precaution against fire. Schneider refused, saying it was against company policy to give customers copies of programs developed for them by Computer Print Systems. This policy prevented the company's customers from taking the lists—and their business—to another computer processor.

Later that year, another company of which Schneider was sole shareholder encountered financial difficulties and ceased activity. Fearing a similar fate might befall Computer Print Systems—and disrupt CPC's monthly mailing operation—Liss informed Lewis that unless CPC could acquire backup copies of the computer programs used to process its work, he would take the account to another company. Without informing Schneider, Lewis procured backup copies of the programs, along with machine-code instructions, and turned them over to Liss. At that time, Liss did not know that it was contrary to Computer Print Systems' corporate policy for Lewis to supply the items. Liss obtained the items, but didn't use them, and maintained the CPC account with Computer Print Systems.

In January 1976, Lewis talked with Schneider about leaving his position at Computer Print Systems. He submitted his resignation to Schneider in March, but remained with the company until May 7. Liss had discovered in April that Lewis was going to leave Computer Print Systems. Somewhat concerned, he sought to induce Schneider to retain Lewis by threatening to take his account to a competing computer processor unless Lewis remained on the CPC account. Apparently, Liss was concerned that the CPC account would not receive the individual attention that it had received during Lewis' tenure with Computer Print Systems.

An independent agreement is reached

Unable to convince Schneider to retain Lewis, Liss contacted Lewis on April 20, unbeknownst to Schneider. The two men made an agreement that Lewis would process the CPC account as an independent consultant. Three days later, Lewis, who had purchased several blank computer tapes for this task, ran a test of the tapes at Computer Print Systems's facility to determine that they were in good condition. For a reason that was never explained, the log that recorded computer use at Computer Print Systems was torn and didn't reflect Lewis's use of the computer that day.

Schneider learned in early May that Lewis planned to take the CPC account with him when he left. In letters dated May 4 and May 14, 1976, Liss instructed Schneider to relinquish to Lewis the programs and material used to process the CPC account; Schneider didn't respond to the letters. On May 17, Lewis, Liss, and Schneider met to try to reach a settlement.

Debating ownership of the programs

During the meeting, Schneider refused to deliver the material in question. He informed Liss for the first time that the programs were the exclusive property of Computer Print Systems—not of CPC. Neither Lewis nor Liss revealed to Schneider that CPC had retained the program copies Lewis had made in June 1975. After the meeting, Lewis informed Liss that, in his assessment, the tapes and other material didn't belong to CPC. Liss told Lewis "not to worry about it."

The next day, Liss turned the 1975 backup tapes over to Lewis. Using the backup tapes and the facilities of an independent computer-processing company, Lewis developed new programs to process the CPC account in time for a direct mailing, which was to take place at the end of May.

Shortly thereafter, Schneider learned that the computer at Computer Print Systems' office had been used on April 23, and that this use wasn't reflected in the computer log. The unlogged computer use, and the knowledge that Lewis had in an extremely short time developed programs to process the CPC account, led Schneider to suspect that Lewis had appropriated copies of the CPC tapes in April. He further speculated that Lewis had made the copies and conspired to usurp the CPC account while he was still employed by Computer Print Systems.

Charges of conversion are filed

On June 8, Computer Print Systems brought suit against Lewis and Liss, charging them with conversion of the CPC tapes, conspiracy to have Lewis breach his fiduciary duty as an officer of Computer Print Systems, and usurping of Computer Print System's corporate opportunity. The lawsuit proceeded upon the premise that the defendants had conspired to divert the CPC account from Computer Print Systems since January, when Lewis first contemplated leaving Computer Print Systems, and that Lewis had converted copies of the CPC programs in April in furtherance of the conspiracy. Only after the lawsuit had been filed did Schneider discover the correct account of how CPC had obtained copies of the computer programs.

The Court of Common Pleas concluded that the evidence was insufficient to support the allegation that Liss and Lewis had usurped corporate opportunity. The Court also denied Computer Print Systems' request for a preliminary injunction restraining the defendants from using the computer programs, and found no support for the conspiracy charge.

The Court did, however, judge in favor of Computer Print Systems on its claim for conversion of the computer programs in the sum of $18,000, representing the value of the computer programs appropriated by the defendants. The defendants appealed, contending that they were not guilty of conversion because Computer Print Systems had no proprietary interest in the computer programs.

The Superior Court of Pennsylvania rejected the defendants' contention and affirmed the judgment of the Court of Common Pleas. The Superior Court declared that the ". . . appellee (Computer Print Systems) had a legally protected interest in the items taken since the programs represented a substantial investment of time and money by [appellee] and a device of importance to the continuing operation of [appellee's] business.'" **EDN**

Author's biography

H Newcomb Morse, JD, LL M, FAAFS, received the Juris Doctor degree from Tulane University and the Master of Laws degree from the University of Wisconsin. He is Professor of Law at Pepperdine University in Malibu, CA.

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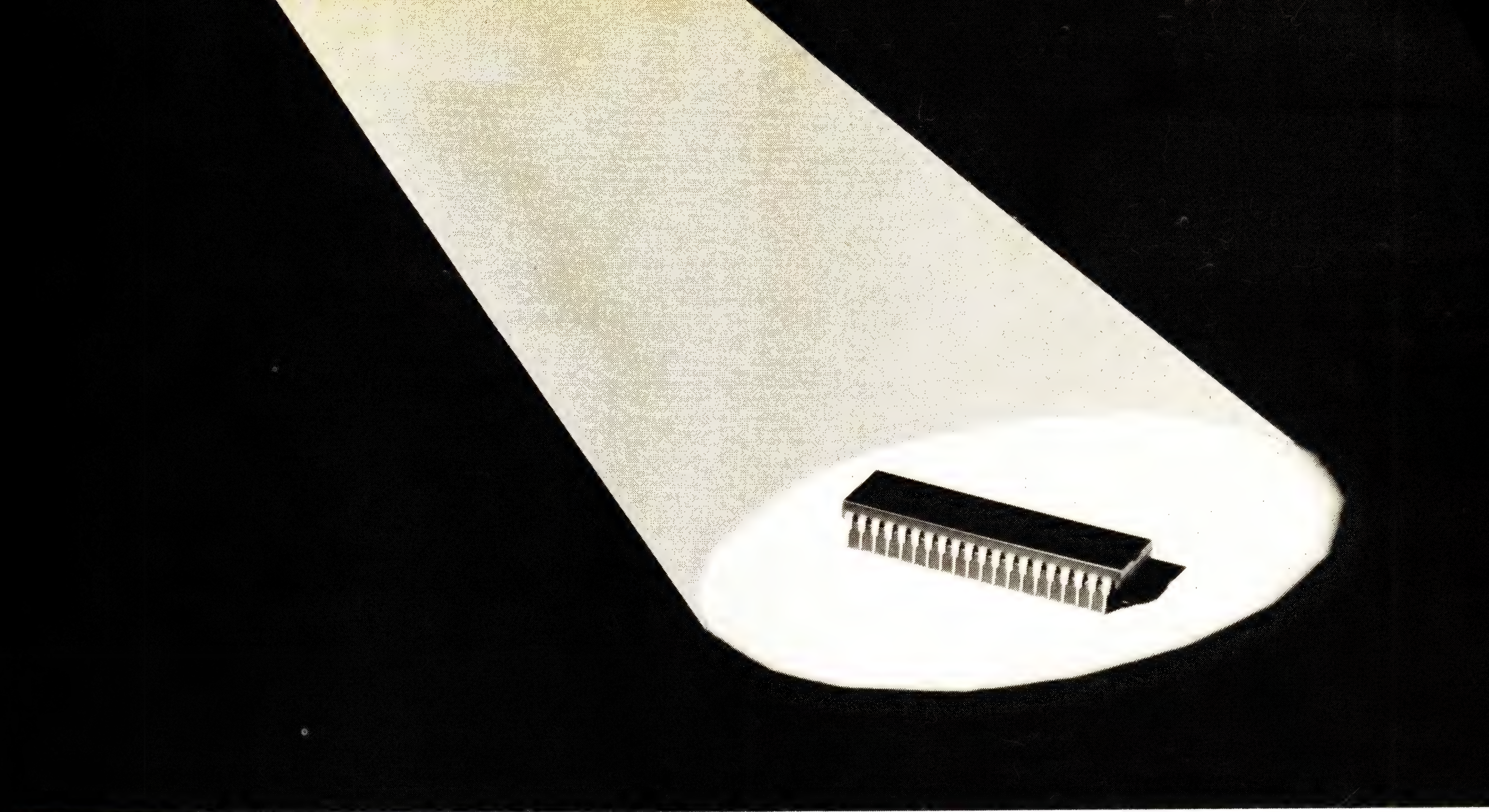

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Heavy emphasis is placed on design examples involving gate arrays. Newly developed products covered in the proceedings include the ACE series (advanced customized ECL) from Signetics, the R series of bipolar devices from Ferranti for systems with complexities to 10,000 gates, CMOS and CMOS/SOS gate arrays from RCA, ECL core arrays from Applied Micro Circuits Corp., and analog/digital gate arrays from Telmos. Also of interest are papers on linear arrays, logic simulation, software, and testing.

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1985 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	EDN Editorial Emphasis
Jan. 10	Dec. 11	Microprocessor Technology Technical Article Database Index Power Semiconductors Semicustom IC Design Electronic Materials
Jan. 24	Jan. 2	Display Components Military Electronics CAE Report Instrumentation Automated Design & Engineering for Electronics Show Preview
Feb. 7	Jan. 15	Computer Peripherals Memory Technology Power Supplies Software Converters
Feb. 21	Jan. 29	Semicustom IC Directory & Design Series Automated Design & Engineering for Electronics Show Product Preview (CAE/CAD) Electronic Materials Instrumentation Fiber Optics Technology
Mar. 7	Feb. 12	Instruments Microprocessor Technology Report & Directory Microcomputer Operating Systems Circuits
Mar. 21	Feb. 26	Communications Special Issue CAE Report Encryption Technology Instruments Graphics IC Technology
April 4	Mar. 12	Personal Computers Electro '85 Show Product Review Semicustom ICs April Fools Supplement Hybrid ICs
April 11	Mar. 19	Military Electronics - Product Showcase Power Supplies, Packaging, Hardware, Interconnect Devices, ICs & Semiconductors, Components, Test & Measurement Equiment, Computers & Peripherals
	ELECTRO '85 SHOW GUIDE	Available to advertisers running a full page in both Electro issues . . . a free page in the Electro Show Guide
April 18	Mar. 26	Electro '85 Show Issue Surface-mount Devices IC Technology CAE Report Computer Boards
May 2	April 9	Power Supplies Comdex '85 Show Preview Computer Technology Instruments Artificial Intelligence Technology
May 16	April 23	Analog Design Technology Special Issue Op Amps Semicustom IC's CAE Report
May 30	May 7	CAE Workstations Telecommunications ICs Computer Peripherals Components
June 13	May 21	Microcomputer Development Systems Fiber Optics Technology Power Semiconductors ICs
June 20	May 28	Microsystems Special Issue Microcomputer Board-Level Directory, Controllers, Interfaces, Memory
June 27	June 4	National Computer Conference '85 Show Issue Disk Drives Converters Semicustom ICs Microcomputer Operating Systems
July 11	June 18	Product Showcase — Volume I ICs & Semiconductors Hardware & Interconnect Devices Power Supplies Sources Software Literature on Computers, Peripherals, Components, Test & Measurement Instruments, Products from Europe

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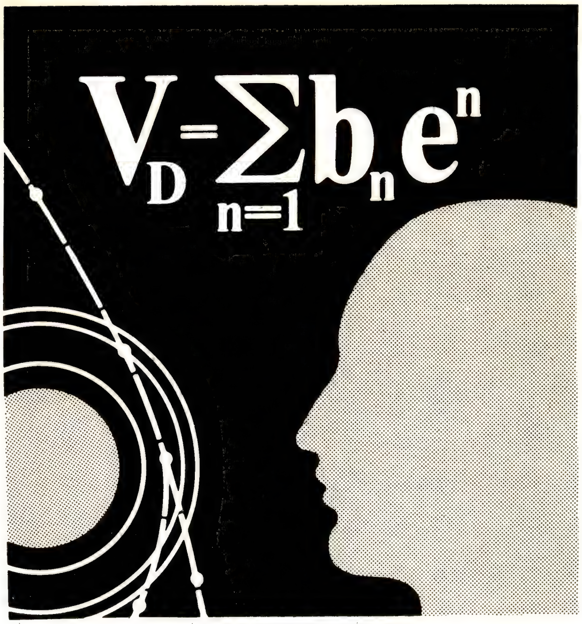

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Test Equipment Development Manager — Manager of development projects for manual and automatic test equipment for missile radar fuze development and production programs. Experience in test equipment system architecture, system level spec generation, radar signal processing and design of computer driven IEEE bus controlled systems. Contact Jerry Rule.

Microwave Electronic Engineers — Senior level engineers to lead the development of EHF technology for future SDLS compatible spacecraft. Must have the ability to translate the system requirements into module and component performance requirements. Responsibilities include assisting in SDLS system definition, generating EHF component requirements and designing, directing and reviewing EHF technology development activity. Prefer BSEE and 9 years experience. Project/task leader experience a plus. Contact Jerry Chadwick.

Signal Processing Design Engineers
Our Aerospace Advance Communications Section has several design assignments: Digital signal processing units for PSK/QAM modulation recognizer, IF analog signal processing modules for recognition system from DC to 400 mhz and state-of-the-art spread spectrum and PCM receivers. Prefer BSEE/MSEE with 5 years related experience. Contact Paulette Dorris.

Supplier Quality Assurance Engineers
Responsibilities include source surveys, supplier liaison and internal coordination of project personnel. Knowledge of both electrical and mechanical parts, statistical sampling, production processes and MIL-Q-9858. Prefer BSEE with 3 years related experience. Contact Gary Yost.

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Please send your resume with salary history/requirements to: **Mr. Tony Rodriguez, Employment Manager, Dept. EDN 1/84, ITT Federal Electric Corporation, P.O. Box 5728, Vandenberg Air Force Base, CA 93437.**

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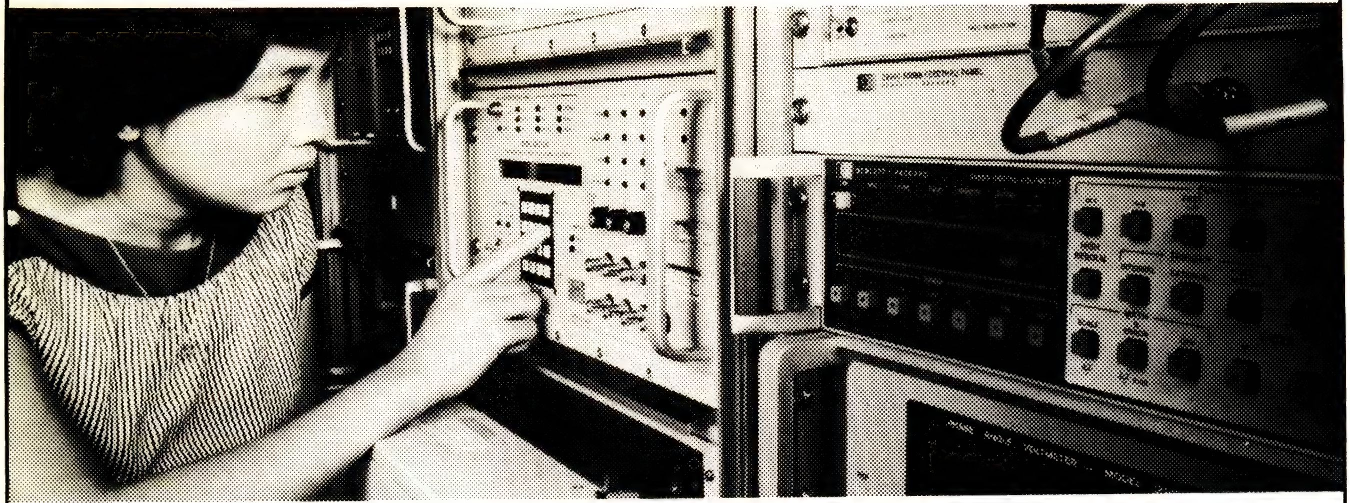

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ATE Specifications Engineer
Develop specifications for ATE hardware and software in accordance with MIL-STD's 490 & 483. Requires knowledge of ATLAS and experience with ATE or test program sets. MIL-STD 490/483 background preferred. BSEE required.

Firmware Development Engineer
Develop firmware for microprocessor-controlled test equipment. Requires 3+ years experience in firmware or real-time program applications. BSEE or BSCS required.

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Design and develop Automatic Test Systems using the MATE philosophy . Requires background in Assembly and High Order Languages (JOVIAL J73). Experience with UNIX operating systems, VAX 11/780 and MIL-STD-1750A computers desirable.

Microprocessor Programming Engineer
Design and program microprocessor-controlled test equipment. Develop and debug software for 8086 microprocessor. Design and test digital hardware. Write design specifications, test procedures and manuals. Requires experience in electronic design and microprocessor programming; familiarity with MIL environment test equipment requirements preferred. BSEE required.

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Assume lead role in development and integration of a mobile automatic calibration system for depot ATE. Defines calibration requirements, selects standards and develops procedures. Assist in the development & implementation of ATE calibration software. BSEE and at least 7 years' experience required.

Test Equipment Systems Engineer
Responsible for systems analyses, concept definitions, trade studies, system architectural designs, interface control documents, test equipment specifications, and system integration plans and procedures for systems test equipment. Will perform hardware/software tradeoffs and configure new test systems. Test equipment background and BSEE or BSCS required.

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Assume duties of a Senior Technical Staff Engineer in the area of Test Systems (ATE) serving as technical troubleshooter for senior management and providing the technical direction to other engineers in order to complete a project on schedule and within cost. Experience must include MTE/ATE detailed circuit design plus functional circuit analysis on complicated analog and digital system and subsystem units for test. Recent background required in the development of ATE station with multiple/compatible instruments controlled by HP 1000 or TEK 3260/3270 in BASIC or ATLAS. MSEE preferred.

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Design, code and integrate software modules relating to ATLAS compiler and test station operation system for automated test systems, working from new ATS requirements or change requests. Requires experience with HP 1000 automated test systems, HP RTE IVB, HPID and HP device subroutines, related software and ATLAS compilers. Fluent knowledge of FORTRAN IV required. BSEE, BSCS, MS/Math or equivalent experience required.

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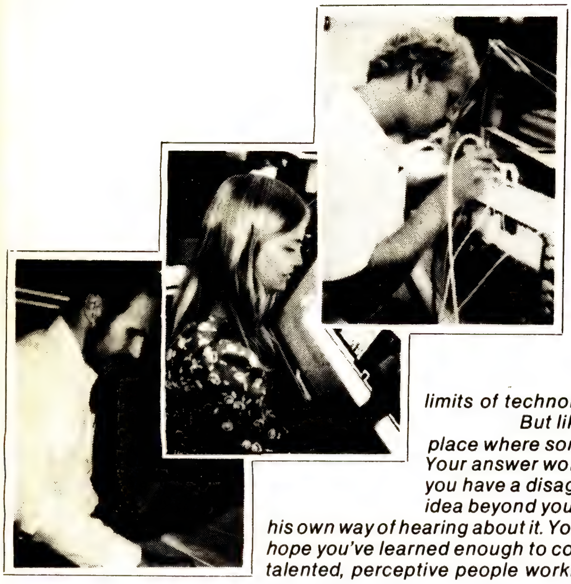

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Your involvement will consist of developing both real-time microprocessor control software for telecommunications equipment and related test instrumentation, and structured assembly language and PASCAL for C programs from design pseudocode (PDL), as well as testing/debugging programs with microprocessor hardware. A BSEE or CS is required, as are 1-3 years' experience, and a working knowledge of an assembly language and either C or PASCAL.

QUALITY ASSURANCE ENGINEER

Responsible for developing, implementing and maintaining QA/QC process, procedures and systems for processing materials into finished products. Also, involves evaluating components and material manufacturers to ensure sources of quality parts. Requires a BSEE degree with 2-5 years' experience in a quality assurance for control engineering or manufacturing environment.

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Boston	January 28-29
*Anaheim — AFCEA	January 29-30
St. Louis	February 11-12
Dallas/Fort Worth	February 25-26
Los Angeles	March 4-5
Minneapolis	March 11-12
Phoenix	March 18-19
Washington, D.C./Baltimore	March 25-26
Orlando	April 1-2
Long Island	April 15-16
Boston	April 22-23
San Jose	April 29-30
Chicago	May 6-7
Denver	May 13-14
Seattle	May 20-21
*Washington, D.C./Baltimore — AFCEA	June 5-6
Los Angeles/Irvine	June 10-11
Raleigh/Durham	July 15-16
Boston	July 29-30
Dallas/Fort Worth	August 5-6
Long Island	August 12-13
Phoenix	August 19-20
San Jose	August 26-27
Denver	September 9-10
Orlando	September 23-24
Minneapolis	Sept. 30-Oct. 1
Chicago	October 7-8
Los Angeles	October 21-22
Washington, D.C./Baltimore	October 28-29
San Jose	November 11-12
Boston	November 18-19

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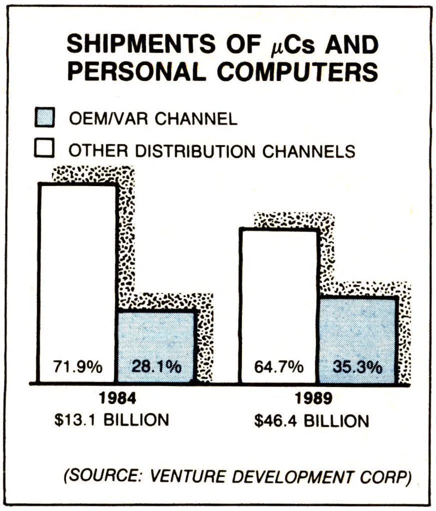


µC suppliers step up pursuit of OEMs and VARs

As the crowd of suppliers increases by crushing numbers in the µC and personal-computer market, vendors are pressing their efforts to establish modes of distribution other than retail sales. Led by IBM, supermicrocomputer and personal-computer vendors are increasing their sales to OEMs and value-added resellers (VARs), according to the market-research firm Venture Development Corp (Wellesley, MA).

VDC projects that shipments of personal computers and supermicrocomputers through value-added distribution channels will grow from 1984's $3.676 billion level to $16.367 billion in 1989. The general value-added market consists of software systems houses, OEMs, VARs, turnkey suppliers, and systems integrators. These companies tailor µCs and peripherals to specialized uses by adding hardware or software or both. They sell systems as solutions to specific problems, rather than as simple, generic hardware.

The consequent attempt to revise distribution channels is blurring traditional distinctions. Some systems integrators have blended with retail specialty stores to form a hybrid distribution channel. Some independent retail stores are forced to become, in effect, VARs. Traditional retail stores do not have trained sales people or experience in specialized markets for value-added products, so they must reorganize to offer their customers more sophisticated support and service.

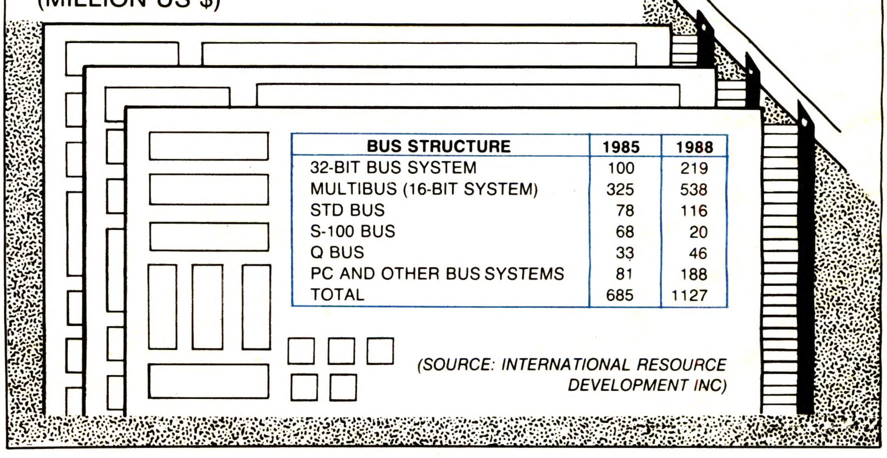
Programmable controllers give way to industrial µCs

As the process-control market becomes increasingly software intensive, users are tending to develop their own software, and this trend is inspiring the replacement of programmable controllers with industrial microcomputers. According to the market-research firm International Resource Development Inc (Norwalk, CT), the 1984 market for programmable controllers was projected to fall below $400 million, while the market for industrial µCs —particularly the 32-bit systems— was expected to push past the $250 million mark. Market shares for programmable controllers should continue to shrink for the remainder of the 1980s and into the 1990s, forecasts IRD.

The industrial-µC market is very crowded: There are more than 300 manufacturers and countless systems houses, and no one concern has more than a 5% market share. Companies like Honeywell, Foxboro ICT, and Fish Controls are making strong efforts to capture leads in the market, but hopes for such concentration are being frustrated by the users themselves. Users are becoming very sophisticated in the development of process-control systems, and they are taking a do-it-yourself approach to such development. Likely beneficiaries of this trend may be IBM, which has recently introduced a ruggedized version of its Personal Computer, and manufactuers of board-level analog-input and other control-related subsystems.

The increasing popularity of industrial µCs obviously redounds to the benefit of µC-bus manufacturers, but these vendors are not sharing the good times equally. IRD predicts that 1985 shipments of Multibus single-board systems will equal those of all other bus structures combined. This lead should continue at least through 1988. The 32-bit bus products are gaining popularity and STD Bus products will see some growth, but S-100 boards are apparently fading away. Approximately one-third of board-level-product sales will be on an OEM basis to industrial-µC and programmable-controller manufacturers, and two-thirds will be to end users through a variety of distribution channels.

SINGLE-BOARD SHIPMENTS BY BUS STRUCTURE (MILLION US $)



BUS STRUCTURE	1985	1988
32-BIT BUS SYSTEM	100	219
MULTIBUS (16-BIT SYSTEM)	325	538
STD BUS	78	116
S-100 BUS	68	20
Q BUS	33	46
PC AND OTHER BUS SYSTEMS	81	188
TOTAL	685	1127

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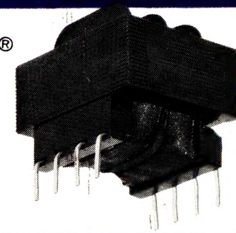

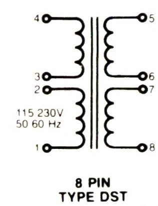

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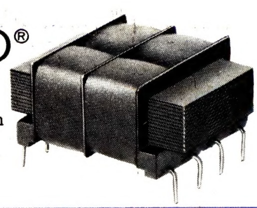

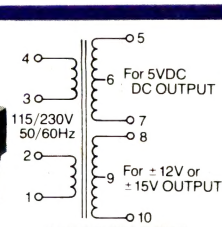

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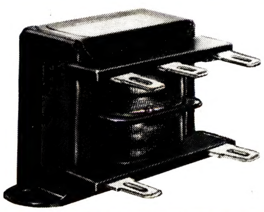

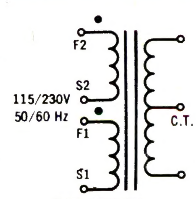

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